



FOD060L, FOD260L, FOD063L LVTT/LVCMOS 3.3V High Speed-10 MBit/s Logic Gate Optocouplers

Single Channel: FOD060L, FOD260L

Dual Channel: FOD063L

Features

- Compact SO8 package (except FOD260L – 8-pin DIP)
- Very high speed – 10 MBit/s
- Superior CMR — 50 kV/μs at 2,000V peak
- Fan-out of 8 over -40°C to +85°C
- Logic gate output
- Stroable output (single channel devices)
- Wired OR-open collector
- U.L. recognized (File # E90700) (pending)
- UDE approval pending

- Data multiplexing
- Switching power supplies
- Pulse transformer replacement
- Computer-peripheral interface

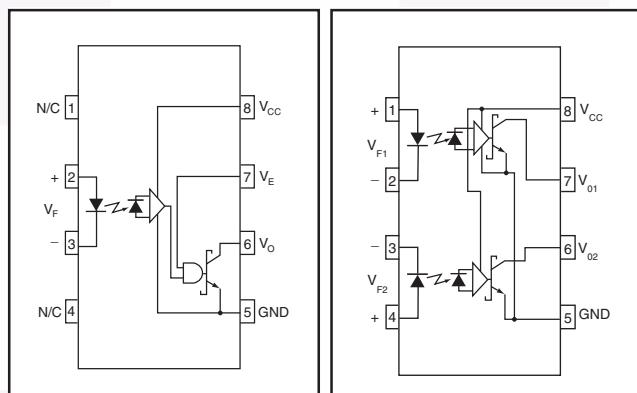
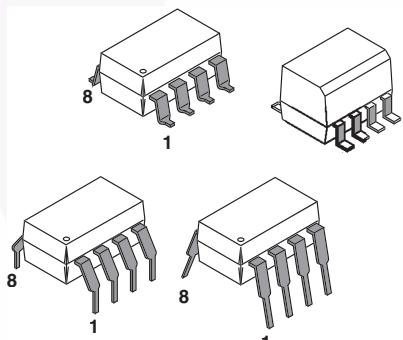
Description

These optocouplers consist of an AlGaAs LED, optically coupled to a very high speed integrated photo-detector logic gate. Single channel devices include a strovable output. This output features an open collector, thereby permitting wired OR outputs. The output consists of bipolar transistors in a Bi-CMOS process for reduced power consumption. The coupled parameters are guaranteed over the temperature range of -40°C to +85°C. A maximum input signal of 5 mA (3 mA for the FODX6XL versions) will provide a minimum output sink current of 13 mA (fan out of 8). An internal noise shield provides superior common mode rejection of typically 50 kV/μs at 2,000V common mode.

Applications

- Ground loop elimination
- LSTTL to TTL, LSTTL or 5-volt CMOS
- Line receiver, data transmission

Package



Single-channel circuit drawing
(FOD060L, FOD260L)

Dual-channel circuit drawing
(FOD063L)

Truth Table (Positive Logic)

| Input | Enable | Output |
|-------|--------|--------|
| H | H | L |
| L | H | H |
| H | L | H |
| L | L | H |
| H* | NC* | L* |
| L* | NC* | H* |

*Dual channel devices or single channel devices with pin 7 not connected.

A 0.1 μF bypass capacitor must be connected between pins 8 and 5. (See note 1)

Absolute Maximum Ratings (No derating required up to 85°C)

| Parameter | Symbol | Value | Units |
|---|------------------|-----------------------------------|------------|
| Storage Temperature | T _{STG} | -40 to +125 | °C |
| Operating Temperature | T _{OPR} | -40 to +85 | °C |
| EMITTER | I _F | 50 | mA |
| DC/Average Forward Input Current (each channel) | | | |
| Enable Input Voltage Not to exceed VCC by more than 500 mV | Single Channel | V _E | VCC + 0.5V |
| Reverse Input Voltage (each channel) | | V _R | 5.0 |
| Power Dissipation | Single Channel | P _I | 45 |
| | Dual Channel | | mW |
| DETECTOR | | | |
| Supply Voltage | | V _{CC} (1 minute max) | 7.0 |
| Output Current (each channel) | I _O | 50 | mA |
| Output Voltage (each channel) | V _O | 7.0 | V |
| Collector Output Power Dissipation | Single Channel | P _O | 85 |
| | Dual Channel | | mW |

Recommended Operating Conditions

| Parameter | Symbol | Min | Max | Units |
|---|-----------------|------|-----------------|-------|
| Input Current, Low Level | I _{FL} | 0 | 250 | µA |
| Input Current, High Level | I _{FH} | *6.3 | 15 | mA |
| Supply Voltage, Output | V _{CC} | 2.7 | 3.3 | V |
| Enable Voltage, Low Level (Single Channel) | V _{EL} | 0 | 0.8 | V |
| Enable Voltage, High Level (Single Channel) | V _{EH} | 2.0 | V _{CC} | V |
| Operating Temperature | T _A | -40 | +85 | °C |
| Fan Out (TTL load) | N | | 8 | |
| Output Pull-up Resistor | R _L | 330 | 4K | Ω |

*6.3 mA is a guard banded value which allows for at least 20% CTR degradation. Initial input current threshold value is 5.0 mA or less.

Electrical Characteristics ($T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ unless otherwise specified.)**Individual Component Characteristics**

| Parameter | Test Conditions | Symbol | Min | Typ** | Max | Unit |
|-------------------------------------|--|-------------------------|----------|-------|------|-------|
| EMITTER | ($I_F = 10 \text{ mA}$) | V_F | | | 1.8 | V |
| Input Forward Voltage | $T_A = 25^\circ\text{C}$ | | | | 1.75 | |
| Input Reverse Breakdown Voltage | ($I_R = 10 \mu\text{A}$) | B_{VR} | 5.0 | | | V |
| Input Capacitance | ($V_F = 0, f = 1 \text{ MHz}$) | C_{IN} | | | | pF |
| Input Diode Temperature Coefficient | ($I_F = 10 \text{ mA}$) | $\Delta V_F/\Delta T_A$ | | | | mV/°C |
| DETECTOR | ($V_E = 0.5 \text{ V}$) | I_{CCH} | | | 7 | mA |
| High Level Supply Current | ($I_F = 0 \text{ mA}, V_{CC} = 3.3 \text{ V}$) | | | | 10 | |
| Low Level Supply Current | ($V_E = 0.5 \text{ V}$) | I_{CCL} | | | 10 | mA |
| | ($I_F = 10 \text{ mA}, V_{CC} = 3.3 \text{ V}$) | | | | 15 | |
| Low Level Enable Current | ($V_{CC} = 3.3 \text{ V}, V_E = 0.5 \text{ V}$) | Single Channel | I_{EL} | | -1.6 | mA |
| High Level Enable Current | ($V_{CC} = 3.3 \text{ V}, V_E = 2.0 \text{ V}$) | Single Channel | I_{EH} | | -1.6 | mA |
| High Level Enable Voltage | ($V_{CC} = 3.3 \text{ V}, I_F = 10 \text{ mA}$) | Single Channel | V_{EH} | 2.0 | | V |
| Low Level Enable Voltage | ($V_{CC} = 3.3 \text{ V}, I_F = 10 \text{ mA}$) (Note 2) | Single Channel | V_{EL} | | 0.8 | V |

Switching Characteristics ($T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = 3.3 \text{ V}$, $I_F = 7.5 \text{ mA}$ unless otherwise specified.)

| AC Characteristics | Test Conditions | Device | Symbol | Min | Typ | Max | Unit |
|---|--|---------------------------|---------------------|-----------|--------|--------|------|
| Propagation Delay Time to Output High Level | (Note 3) ($R_L = 350\Omega, C_L = 15 \text{ pF}$) (Fig. 9) | All | T_{PLH} | | | 90 | ns |
| Propagation Delay Time to Output Low Level | (Note 4) ($R_L = 350\Omega, C_L = 15 \text{ pF}$) (Fig. 9) | All | T_{PHL} | | | 75 | ns |
| Pulse Width Distortion | ($R_L = 350\Omega, C_L = 15 \text{ pF}$) (Fig. 9) | All | $ T_{PHL}-T_{PLH} $ | | | 25 | ns |
| Propagation Delay Skew | ($R_L = 350\Omega, C_L = 15 \text{ pF}$) (Note 5) | All | t_{PSK} | | | 40 | ns |
| Output Rise Time (10-90%) | ($R_L = 350\Omega, C_L = 15 \text{ pF}$) (Note 6) (Fig. 9) | All | t_r | | | | ns |
| Output Fall Time (90-10%) | ($R_L = 350\Omega, C_L = 15 \text{ pF}$) (Note 7) (Fig. 12) | All | t_f | | | | ns |
| Enable Propagation Delay Time to Output High Level | ($V_{EH} = 3 \text{ V}, R_L = 350\Omega, C_L = 15 \text{ pF}$) (Note 8) (Fig. 10) | Single Channel | All | t_{ELH} | | | ns |
| Enable Propagation Delay Time to Output Low Level | ($V_{EH} = 3 \text{ V}, R_L = 350\Omega, C_L = 15 \text{ pF}$) (Note 9) (Fig. 10) | Single Channel | All | t_{EHL} | | | ns |
| Common Mode Transient Immunity (at Output High Level) | ($R_L = 350\Omega$) ($T_A = 25^\circ\text{C}$) ($I_F = 0 \text{ mA}, V_{OH} (\text{Min.}) = 2.0 \text{ V}$) (Note 10) (Fig. 11) | $ V_{CM} = 50 \text{ V}$ | All | $ ICM_H $ | 25,000 | 50,000 | V/μs |
| Common Mode Transient Immunity (at Output Low Level) | ($R_L = 350\Omega$) ($T_A = 25^\circ\text{C}$) ($I_F = 7.5 \text{ mA}, V_{OL} (\text{Max.}) = 0.8 \text{ V}$) (Note 11) (Fig. 11) | $ V_{CM} = 50 \text{ V}$ | All | $ ICM_L $ | 25,000 | 50,000 | V/μs |

Transfer Characteristics ($T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ Unless otherwise specified.)

| DC Characteristics | Test Conditions | Symbol | Min | Typ** | Max | Unit |
|---|---|----------|-----|-------|-----|---------------|
| High Level Output Current (Note 2) $V_E = 2.0 \text{ V}$ | $(I_F = 250 \mu\text{A}, V_{CC} = 3.3 \text{ V}, V_O = 3.3 \text{ V})$ | I_{OH} | | | 50 | μA |
| | Single Channel | | | | | |
| Low Level Output Voltage (Note 2) $V_E = 2.0 \text{ V}$ | $(V_{CC} = 3.3 \text{ V}, I_F = 5 \text{ mA}, I_{OL} = 13 \text{ mA})$ | V_{OL} | | | 0.6 | V |
| | Single Channel | | | | | |
| Input Threshold Current (Note 2) $V_E = 2.0 \text{ V}$ | $(V_{CC} = 3.3 \text{ V}, V_O = 0.6 \text{ V}, I_{OL} = 13 \text{ mA})$ | I_{FT} | | | 5 | mA |
| | Single Channel | | | | | |

Isolation Characteristics ($T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ Unless otherwise specified.)

| Characteristics | Test Conditions | Device | Symbol | Min | Typ** | Max | Unit |
|--|--|-------------------------------|-----------|------|-----------|------|---------------|
| Input-Output Insulation Leakage Current | (Relative humidity = 45%) ($T_A = 25^\circ\text{C}$, $t = 5 \text{ s}$) ($V_{I-O} = 3000 \text{ VDC}$) (Note 12) | | I_{I-O} | | | 1.0* | μA |
| Withstand Insulation Test Voltage | $I_{IO} \leq 2 \mu\text{A}$, $R_H < 50\%$, $T_A = 25^\circ\text{C}$ (Note 12) ($t = 1 \text{ min.}$) | FOD060L FOD063L FOD260L | V_{ISO} | 3750 | | | V_{RMS} |
| | | | | 5000 | | | |
| Resistance (Input to Output) | $(V_{I-O} = 500 \text{ V})$ (Note 12) | | R_{I-O} | | 10^{12} | | Ω |
| Capacitance (Input to Output) | $(f = 1 \text{ MHz})$ (Note 12) | | C_{I-O} | | 0.6 | | pF |

** All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^\circ\text{C}$

Notes

1. The V_{CC} supply to each optoisolator must be bypassed by a $0.1\mu\text{F}$ capacitor or larger. This can be either a ceramic or solid tantalum capacitor with good high frequency characteristic and should be connected as close as possible to the package V_{CC} and GND pins of each device.
2. Enable Input – No pull up resistor required as the device has an internal pull up resistor.
3. t_{PLH} – Propagation delay is measured from the 3.75 mA level on the HIGH to LOW transition of the input current pulse to the 1.5V level on the LOW to HIGH transition of the output voltage pulse.
4. t_{PHL} – Propagation delay is measured from the 3.75 mA level on the LOW to HIGH transition of the input current pulse to the 1.5V level on the HIGH to LOW transition of the output voltage pulse.
5. t_{PSK} is the worst case difference between t_{PHL} and t_{PLH} for any devices at the stated test conditions.
6. t_r – Rise time is measured from the 90% to the 10% levels on the LOW to HIGH transition of the output pulse.
7. t_f – Fall time is measured from the 10% to the 90% levels on the HIGH to LOW transition of the output pulse.
8. t_{ELH} – Enable input propagation delay is measured from the 1.5V level on the HIGH to LOW transition of the input voltage pulse to the 1.5V level on the LOW to HIGH transition of the output voltage pulse.
9. t_{EHL} – Enable input propagation delay is measured from the 1.5V level on the LOW to HIGH transition of the input voltage pulse to the 1.5V level on the HIGH to LOW transition of the output voltage pulse.
10. CM_H – The maximum tolerable rate of rise of the common mode voltage to ensure the output will remain in the high state (i.e., $V_{OUT} > 2.0 \text{ V}$). Measured in volts per microsecond ($\text{V}/\mu\text{s}$).
11. CM_L – The maximum tolerable rate of fall of the common mode voltage to ensure the output will remain in the low output state (i.e., $V_{OUT} < 0.8 \text{ V}$). Measured in volts per microsecond ($\text{V}/\mu\text{s}$).
12. Device considered a two-terminal device: Pins 1,2,3 and 4 shorted together, and Pins 5,6,7 and 8 shorted together.

Typical Performance Curves

Fig. 1 Input Forward Current vs. Forward Voltage

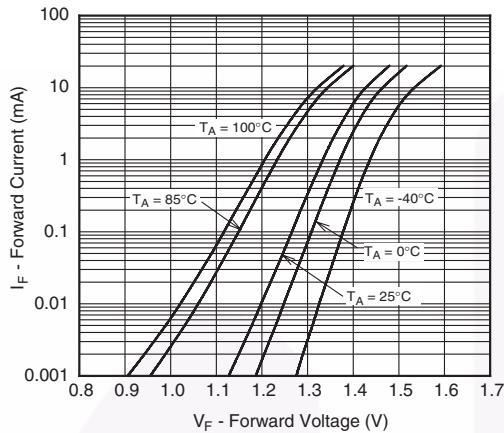


Fig. 2 Input Threshold Current vs. Ambient Temperature

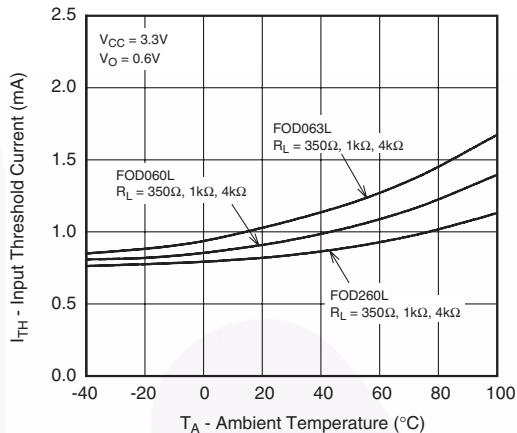


Fig. 3 Low Level Output Voltage vs. Ambient Temperature

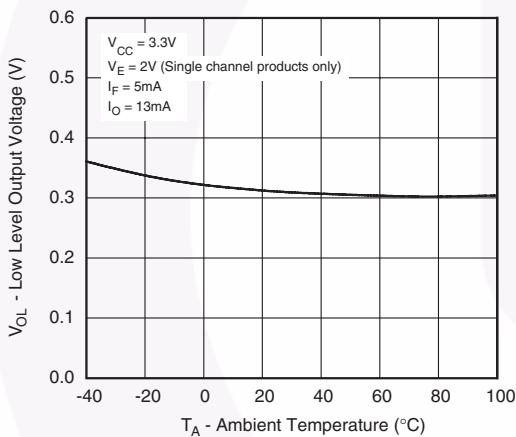


Fig. 4 High Level Output Current vs. Ambient Temperature

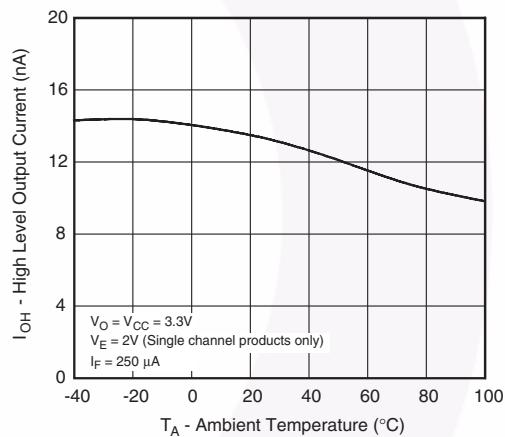


Fig. 5 Low Level Output Current vs. Ambient Temperature

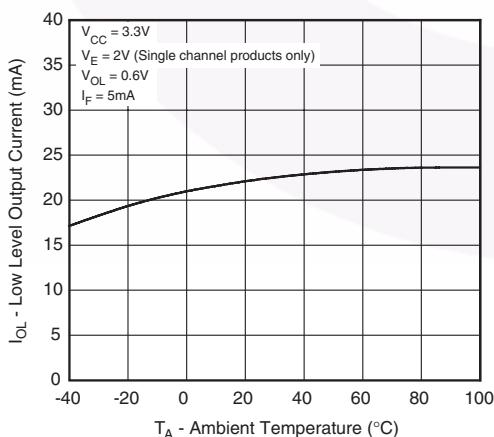
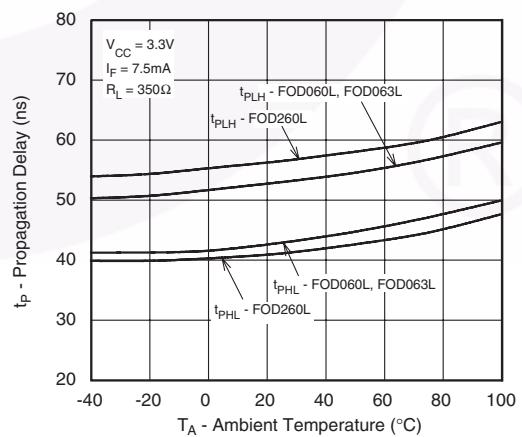


Fig. 6 Propagation Delay vs. Ambient Temperature



Typical Performance Curves

Fig. 7 Rise and Fall Times vs. Ambient Temperature

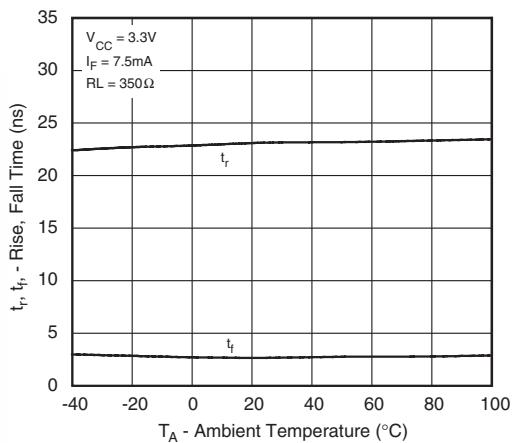
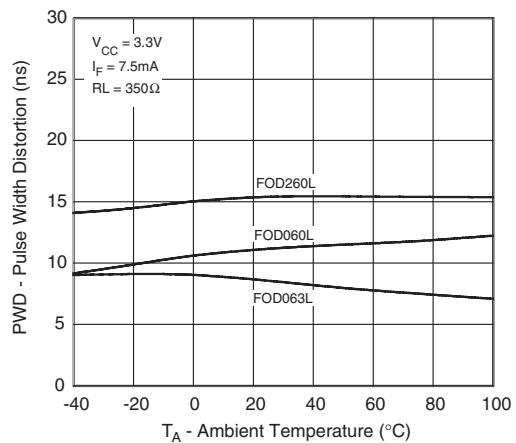


Fig. 8 Pulse Width Distortion vs. Ambient Temperature



FOD060L, FOD260L, FOD063L — LVTT/LVCMOS 3.3V High Speed-10 MBit/s Logic Gate Optocouplers

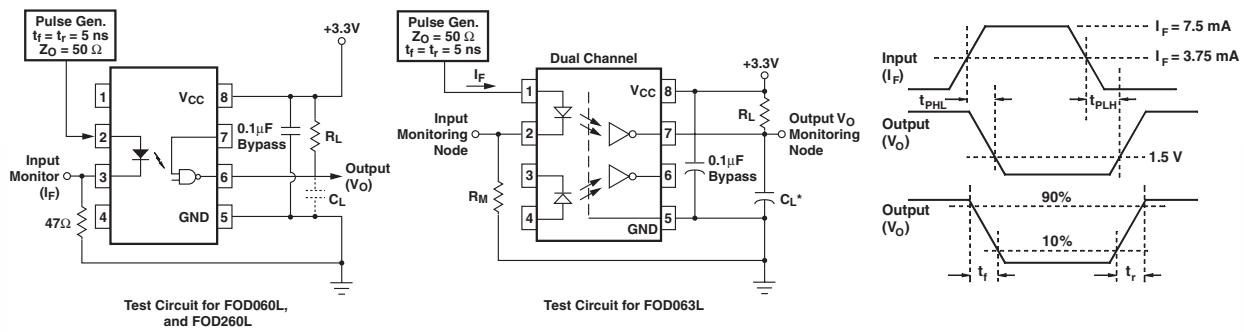


Fig. 9 Test Circuit and Waveforms for t_{PLH} , t_{PHL} , t_r and t_f .

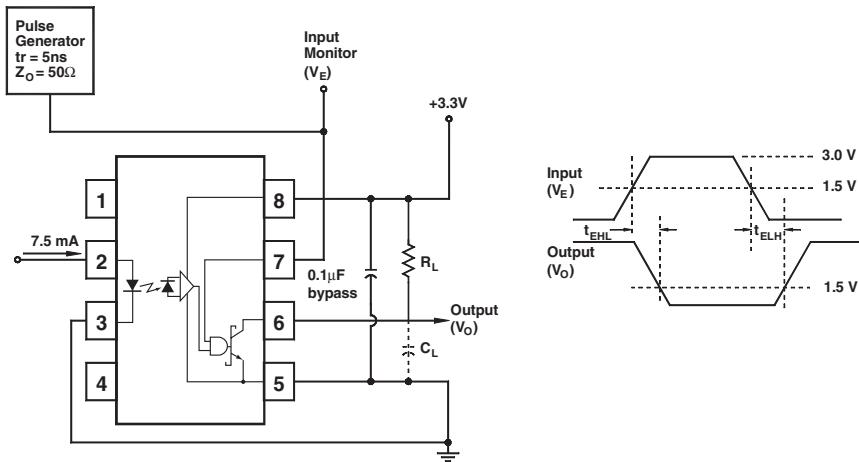


Fig. 10 Test Circuit t_{EHL} and t_{ELH} .

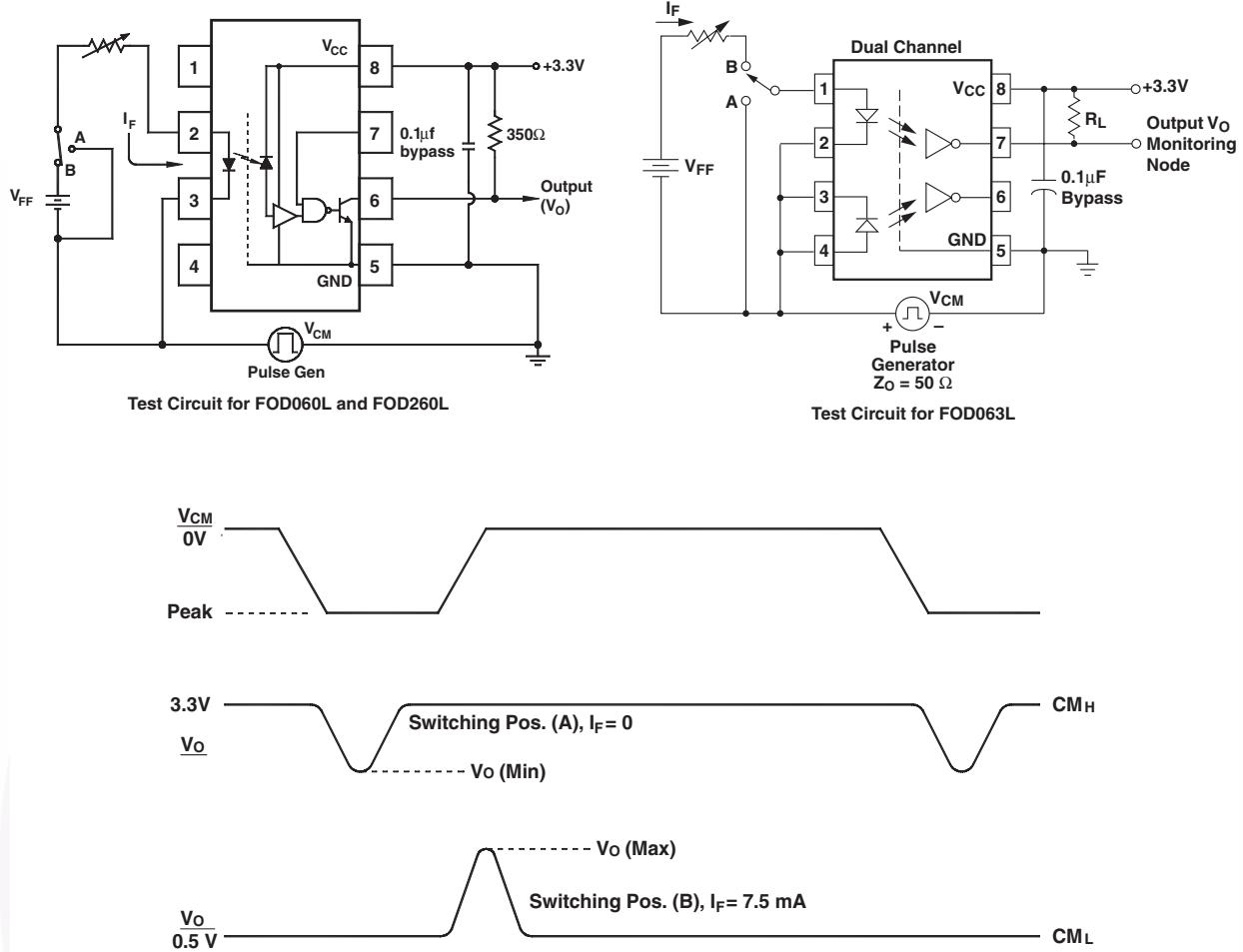
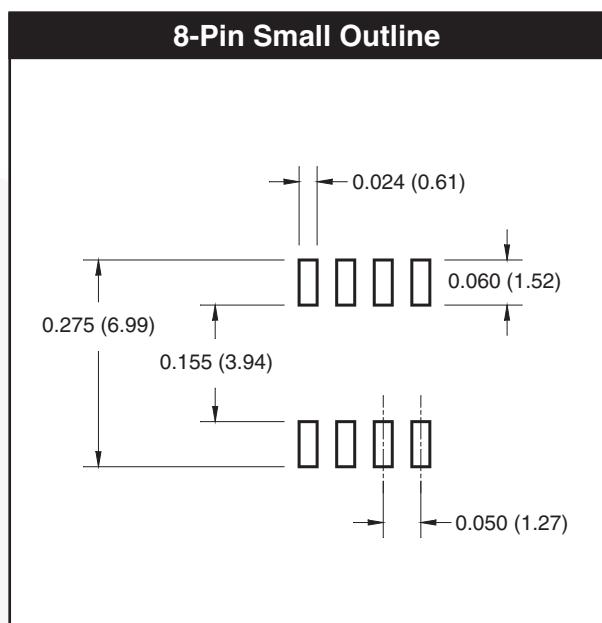
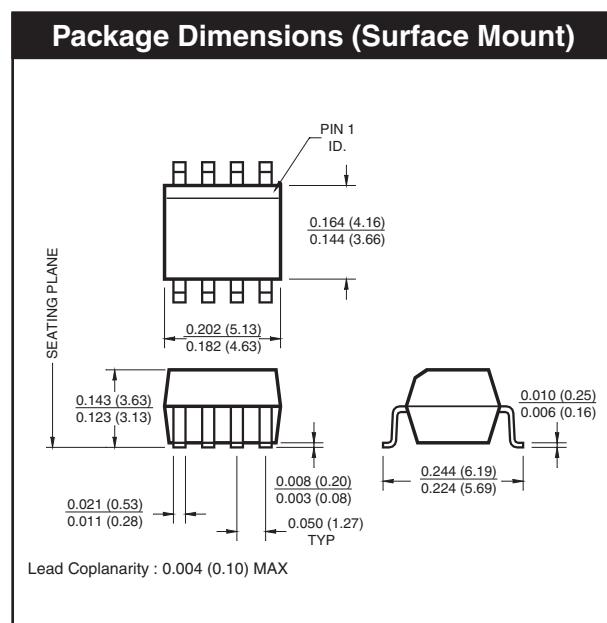


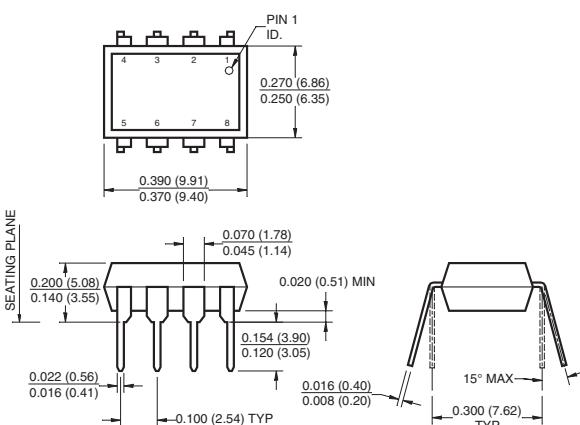
Fig. 11 Test Circuit Common Mode Transient Immunity

8-Pin SOIC

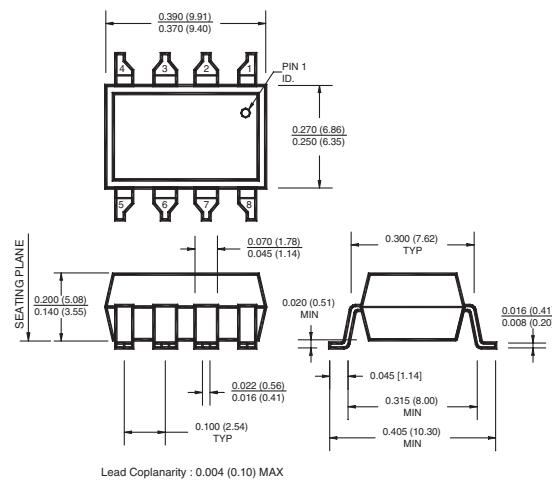


8-Pin DIP

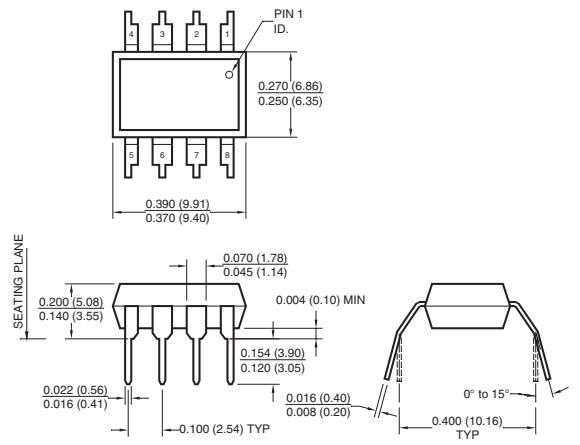
Package Dimensions (Through Hole)



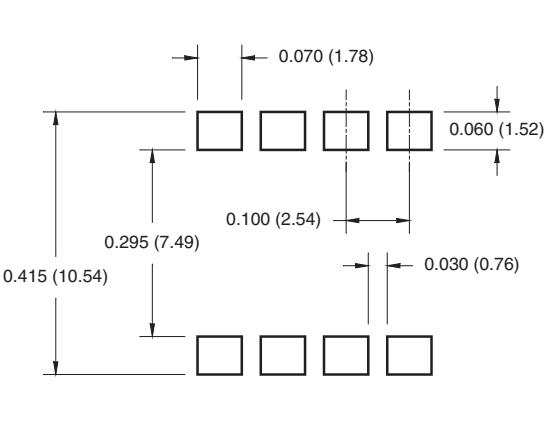
Package Dimensions (Surface Mount)



Package Dimensions (0.4" Lead Spacing)



8-Pin DIP



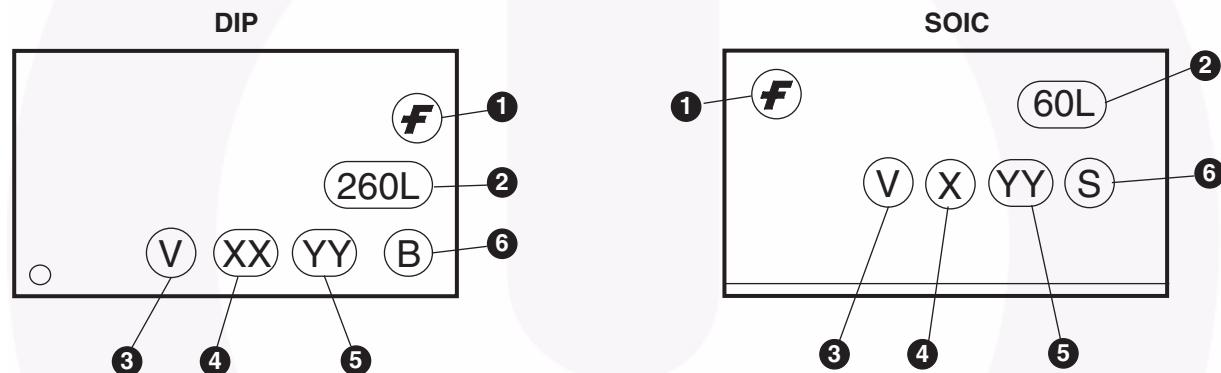
NOTE

All dimensions are in inches (millimeters)

Ordering Information

| Option | Order Entry Identifier | Description |
|-----------|------------------------|--|
| No Suffix | FOD260L | Through Hole (DIP package only) |
| | FOD060L | Surface Mount Lead Form (SOIC-8 package only) |
| S | FOD260LS | Surface Mount Lead Bend (DIP package only) |
| SD | FOD260LSD | Surface Mount; Tape and reel (DIP package only) |
| SV | Pending Approval | Surface Mount; VDE0884 (DIP package only) |
| SDV | Pending Approval | Surface Mount; Tape and reel, VDE0884 (1000 units per reel) (DIP package only) |
| T | FOD260LT | 0.4" Lead Spacing (DIP package only) |
| TV | Pending Approval | 0.4" Lead Spacing, VDE0884 (DIP package only) |
| R1 | FOD060LR1 | Tape and Reel (500 units per reel) (SOIC-8 package only) |
| R1V | Pending Approval | VDE, Tape and Reel (500 units per reel) (SOIC-8 package only) |
| R2 | FOD060LR2 | Tape and Reel (2500 units per reel) (SOIC-8 package only) |
| R2V | Pending Approval | VDE, Tape and Reel (2500 units per reel) (SOIC-8 package only) |
| V | Pending Approval | VDE (SOIC-8 package only) |

Marking Information

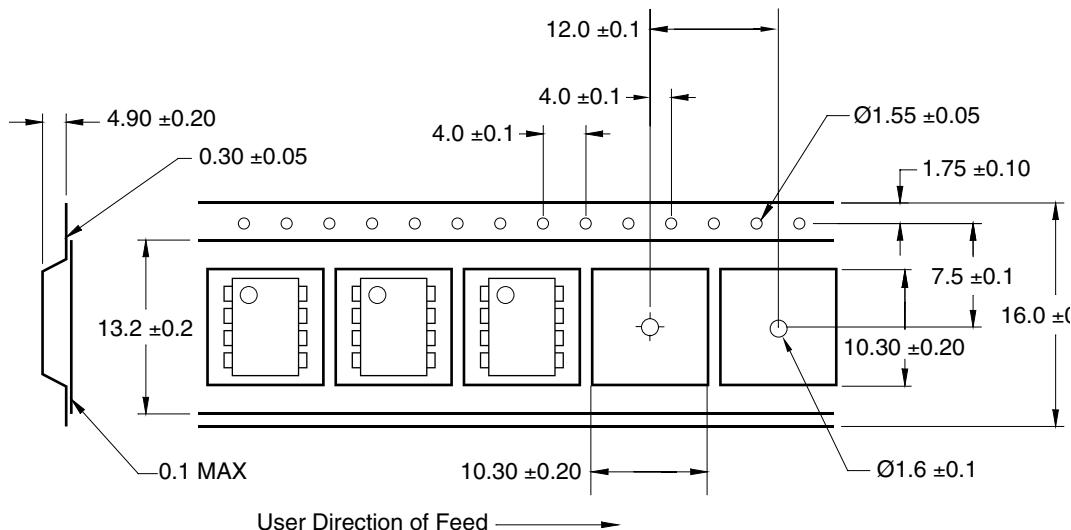


Definitions

| | |
|----------|--|
| 1 | Fairchild logo |
| 2 | Device number |
| 3 | VDE mark (Note: Only appears on parts ordered with VDE option – See order entry table) |
| 4 (DIP) | Two digit year code, e.g., '03' |
| 4 (SOIC) | One digit year code, e.g., '3' |
| 5 | Two digit work week ranging from '01' to '53' |
| 6 | Assembly package code |

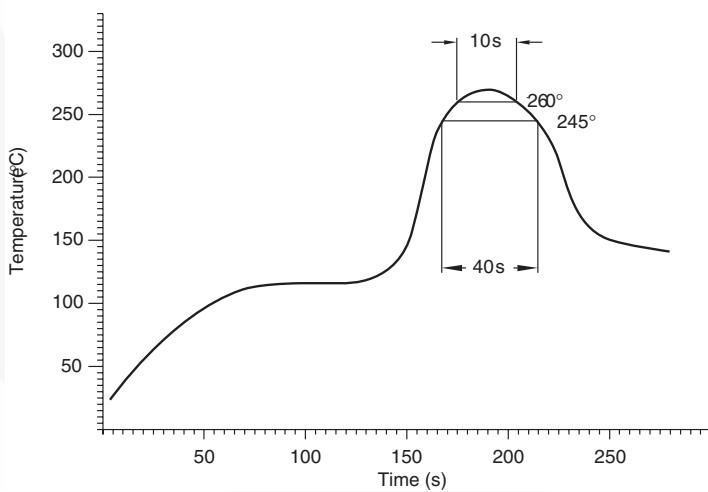
8-Pin DIP

Carrier Tape Specifications (FOD260L)

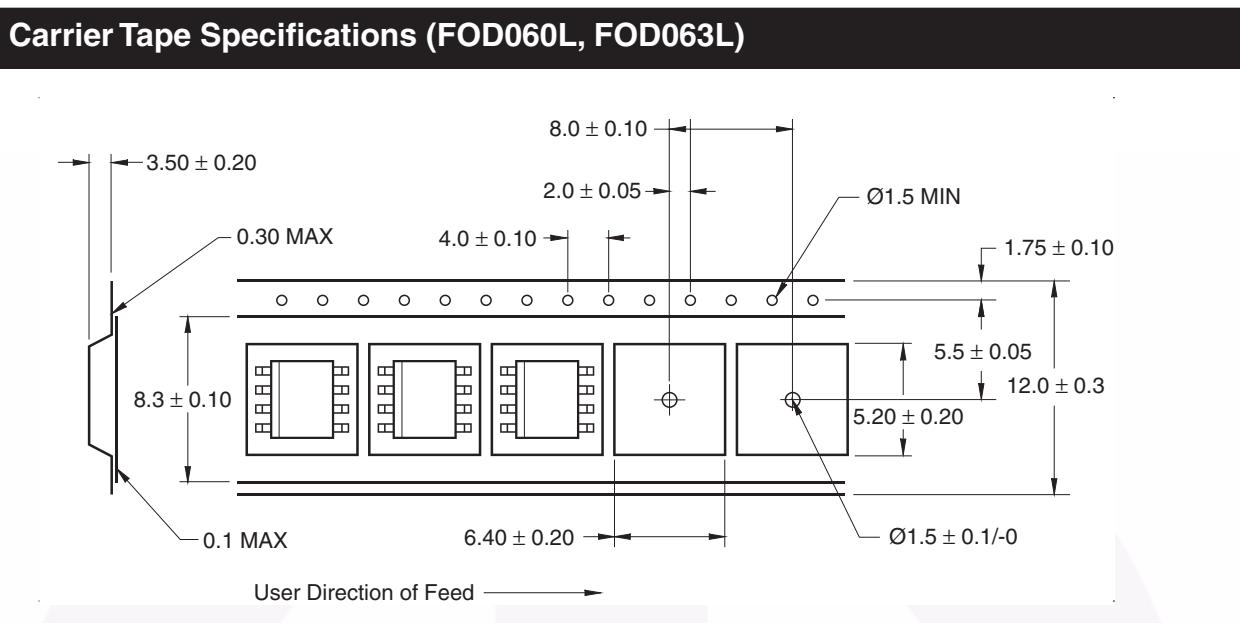


Reflow Profile (FOD260L)

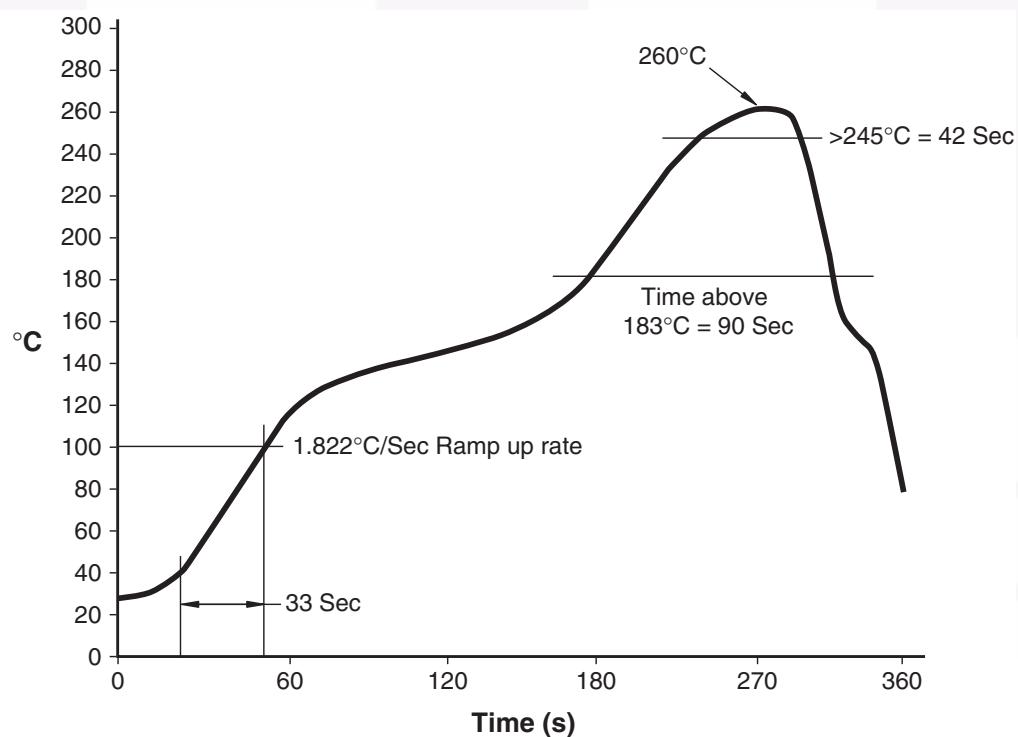
- Peak reflow temperature 260°C (package surface temperature)
- Time of temperature higher than 245°C 40 seconds or less
- Number of reflows Three



8-Pin SOIC



Reflow Profile (FOD060L, FOD063L)





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| Datasheet Identification | Product Status | Definition |
|--------------------------|-----------------------|---|
| Advance Information | Formative / In Design | Datasheet contains the design specifications for product development. Specifications may change in any manner without notice. |
| Preliminary | First Production | Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design. |
| No Identification Needed | Full Production | Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design. |
| Obsolete | Not In Production | Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only. |

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