

Narrowband FM Receiver

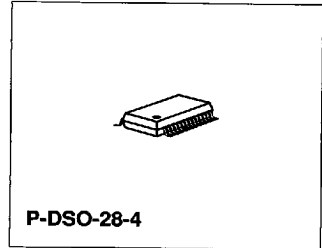
PMB 2430

Preliminary Data

Bipolar IC

Features

- Double conversion heterodyne receiver with limiter/demodulator
- Low current consumption
- Reduced external components
- Low-noise temperature compensated internal reference voltages
- First mixer operating frequencies up to 1500 MHz
- First mixer conversion power gain of 10 dB
- Optional use of first mixer with/without external bias resistor at M1E
- External adjustment of first mixer current for mixer performance improvement
- First mixer stage with high dynamic range and low spurious signals
- Optimum decoupling of first mixer signal input frequency to first LO input frequency
- High decoupling of first mixer output to second mixer signal input
- Second mixer stage with high dynamic range and low spurious signals
- 90-dB IF-limiter gain
- RSSI output with 90-dB RSSI-dynamic range and high linear slope
- Low impedance audio output



P-DSO-28-4

Type	Ordering Code	Package
PMB 2430S	Q67000-A6046	P-DSO-28-4 (Shrink) (SMD)
PMB 2430S	Q67006-A6046	P-DSO-28-4 (Shrink, SMD, Tape & Reel)

Functional Description and Application

The PMB 2430 is a single-chip double conversion heterodyne FM receiver with a limiter and demodulator circuitry. It is designed for input frequencies up to 1500 MHz and for a first intermediate frequency up to 120 MHz. For using the first mixer and to adjust the mixer current, an external resistor has to be connected. The circuit can be used as a narrowband FM receiver for all analog mobile systems.

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First Mixer

The first mixer is a single balanced mixer with a balanced local oscillator input and a balanced open collector output. Via an external bias resistor at M11E the mixer can be connected to ground and the mixer current can be adjusted.

A RF-signal and an external first local oscillator signal enter the chip (M11E or M11B and LO1/ $\overline{\text{LO1}}$) and are mixed down to a first intermediate frequency (IF).

A differential current generated at the balanced mixer output MO1/ $\overline{\text{MO1}}$ is filtered with a resonant circuit and/or a crystal filter. The resonant circuit also connects the open collector output to the supply voltage.

Second Mixer

Through M12E or M12B the filtered first IF-signal reenters the chip.

A second external local oscillator signal is connected to the isolation amplifier at LO2/ $\overline{\text{LO2}}$.

Both signals are mixed down in a single balanced mixer with an unbalanced open collector output to a second IF at pin MO2. This pin is connected to the supply voltage via an external 1.5 k Ω resistor.

Limiter and Demodulator Circuit

The second IF is additionally filtered and fed either into the limiter input LI or into $\overline{\text{LI}}$, where the signal is amplified.

The field strength of the second IF at the limiter input is measured by the RSSI-circuit, which delivers an equivalent DC-voltage at the pin RSSI.

At the limiter output LAO/ $\overline{\text{LAO}}$ the amplified signal drives an external L/C quadrature tank circuit and is phase shifted. This phase shifted signal reenters the chip at the demodulator input QDI/ $\overline{\text{QDI}}$.

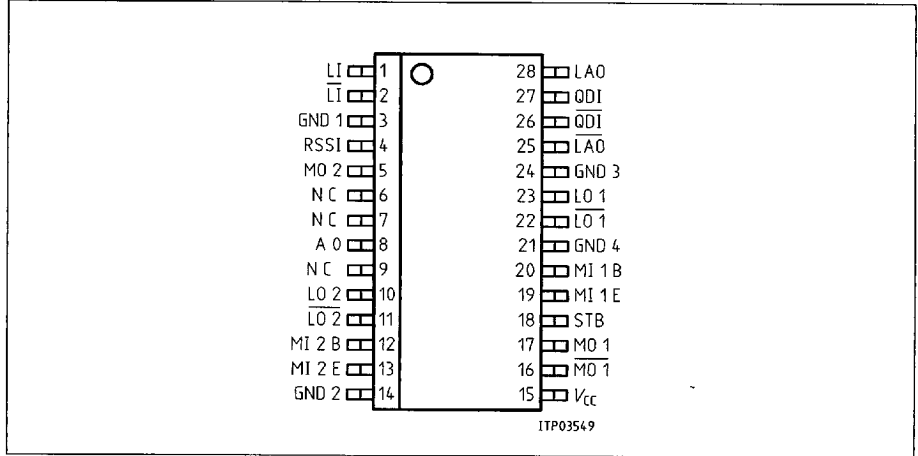
The demodulator mixes the limited signal with the phase shifted signal by means of the quadrature demodulation.

At the pin audio output AO the demodulated output signal can be used directly.

Additional Circuitry and Information

Differential signals and symmetrical circuitries are used all over the IC for high frequency parts, except at the 450 kHz and the audio signal output. For optimum decoupling separate ground rails are provided for the circuitry before and after the first IF-channel filter. A bias driver generates internal temperature and supply voltage compensated reference voltages and currents required for the different circuit blocks. All pins with the exception of the pins connected to the first mixer and the second mixer output pin are ESD protected up to 1kVolt to ground.

Pin Configuration
(top view)



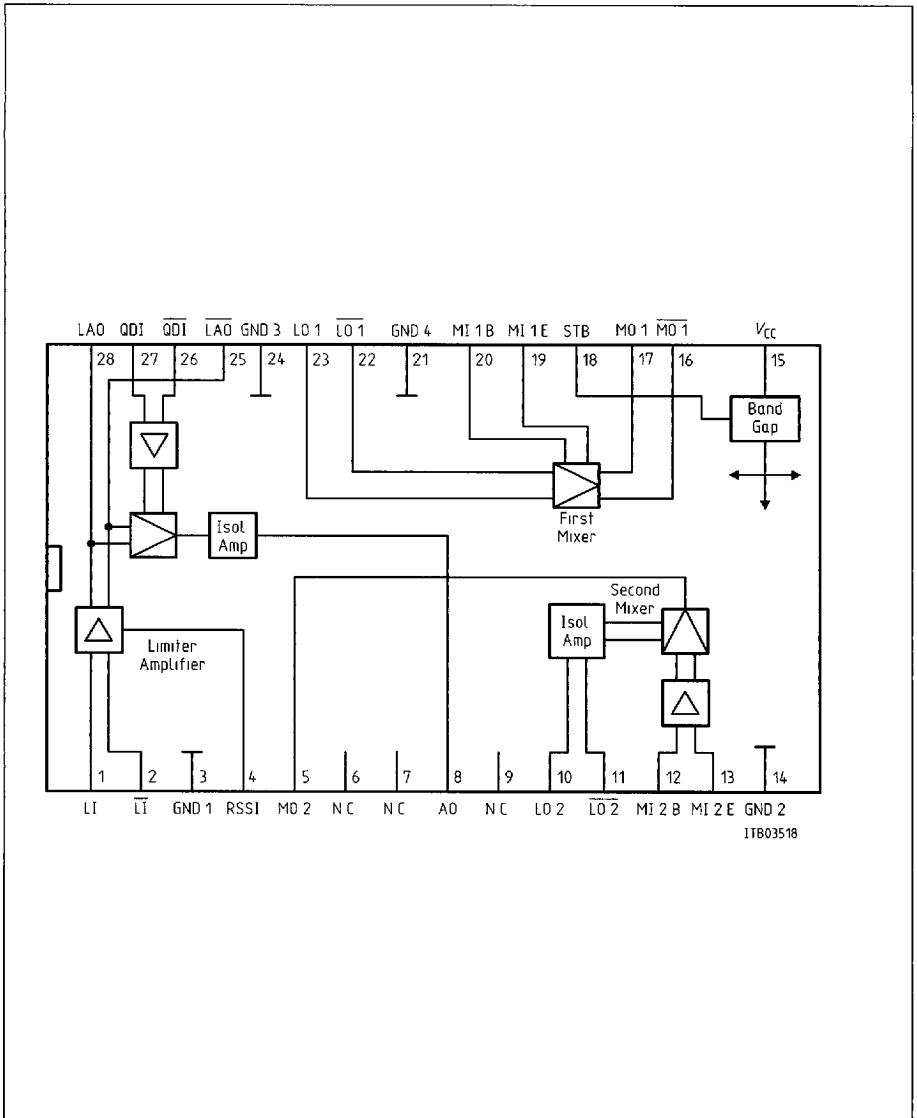
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Pin Definitions and Functions

Pin No.	Symbol	Function
1	LI	Limiter input
2	$\overline{\text{LI}}$	Limiter input
3	GND1	Chip grounding
4	RSSI	Field strength output
5	MO2	Mixer 2 open collector output
6	n.c.	Not connected
7	n.c.	Not connected
8	AO	Audio output
9	n.c.	Not connected
10	LO2	Isolation amplifier mixer 2 input
11	$\overline{\text{LO2}}$	Isolation amplifier mixer 2 input
12	MI2B	Mixer 2 base input
13	MI2E	Mixer 2 emitter input
14	GND2	Chip grounding
15	V_{CC}	Chip supply voltage
16	$\overline{\text{MO1}}$	Mixer 1 open collector output
17	MO1	Mixer 1 open collector output
18	STB	Chip stand-by input
19	MI1E	RF-mixer 1 emitter input, current adjust via external resistor
20	MI1B	RF-mixer 1 base input
21	GND4	Chip grounding
22	$\overline{\text{LO1}}$	Local oscillator mixer 1 input
23	LO1	Local oscillator mixer 1 input
24	GND3	Chip grounding
25	$\overline{\text{LAO}}$	Limiter amplifier output
26	$\overline{\text{QDI}}$	Quadrature detector input
27	QDI	Quadrature detector input
28	LAO	Limiter amplifier output

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Block Diagram

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Electrical Characteristics

Absolute Maximum Ratings

$T_A = -40$ to 85 °C

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Supply voltage	V_{15}	- 0.5	7	V	
Voltage at demodulator	$V_{25, 28}$	- 1	1	V	V_S not supplied
Open collector output voltage (MO1, MO1, MO2)	$V_{5,16,17}$	- 0.5	$V_S + 2.5$	V	$V_S \leq 5.5$ V
Differential input voltage	$V_{1,2,10,11,12,13,19,20,22,23}$	- 1	1	V	
Junction temperature	T_j		+ 125	°C	
Storage temperature	T_{stg}	- 65	+ 150	°C	
Thermal resistance (junction to ambient)	$R_{th JA}$		110	°C/W	

Operational Range

Ambient temperature	T_A	- 40	+ 85	°C	
Supply voltage	V_{15}	4.5	5.5	V	
MI1E/B input level	$P_{MI1E/B}$		- 5	dBm	
MI1E/B input frequency	$f_{MI1E/B}$	50	1500	MHz	
LO1/LO1 input level	$P_{LO1/LO1}$	- 20	+ 3	dBm	
LO1/LO1 input frequency	f_{IF1}	100	1500	MHz	
Intermediate frequency	$f_{MI2E/B}$	40	120	MHz	
MI2E/B input level	$P_{MI2E/B}$		0	dBm	
AO output frequency; 3 dB roll off	f_{AO}	0	20	kHz	
I_{STB} current: high	I_{STB}		200	µA	$V_{STB} = V_S$
V_{STB} voltage: high	V_{STP}	3.0	V_S	V	
I_{STB} current: low	I_{STB}		- 50	µA	$V_{STB} = 0$ V
V_{STB} voltage: low	V_{STP}	0	0.8	V	
RSSI output voltage	V_{RSSI}	0	3.6	V	
LO2/LO2 isolation amplifier frequency range	$f_{LO2/LO2}$	40	120	MHz	

Note: Power levels are referred to an impedance of 50 Ω.

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AC/DC Characteristics $T_A = 25\text{ }^\circ\text{C}$; $V_S = 4.75\text{ to }5.25\text{ V}$

Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			
Supply current	I_{15+5}	2.0	3.1	4.5	mA	$V_{STB} = V_{CC} = \text{high}$	1
RF-supply current	I_{16+17}		2.0	2.6	mA	$V_{STB} = V_{CC} = \text{high}$	1 ¹⁾
Supply current	I_{15+5}		0.5		mA	$V_{STB} = 0\text{ V} = \text{low}$	1
RF-supply current	I_{16+17}			0.1	mA	$V_{STB} = 0\text{ V} = \text{low}$	1 ¹⁾

Signal Input MI1E/B of Single Balanced Mixer (base pin 20 AC grounded)

Input resistance	$R_{MI1E/B}$		50		Ω	base AC grounded	3
Input inductance	$L_{MI1E/B}$		20		nH	in series to $R_{MI1E/B}$	3
Max. input level	P_{MI1max}	-9	-5		dBm	3 dB compression at MO1/ MO1 referenced to MI1E/B input; $f_C = 900\text{ MHz}$	1
Intercept point	P_{IP}	-6	-2		dBm	referenced to MI1E/B input; IP carrier frequency distance = 60 kHz; $f_C = 900\text{ MHz}$	1
Blocking level	P_B	-16	-12		dBm	3 dB attenuation of wanted signal at MO1/MO1 referenced to MI1E/B input; MI1E/B input level = -30 dBm; $f_C = 900\text{ MHz}$	1
Input interference level at $f = f_{int}$	P_{int}	-90	-94		dBm	signal level at f_{IF2IN} with $P_{int} < -44\text{ dBm}$	6
Input frequency	$f_{MI1E/B}$	50		1500	MHz	optimum matched input circuit	1
Noise figure	$F_{MI1E/B}$		8	10	dB	$f_C = 900\text{ MHz}$; DSB noise	1
Noise figure	$F_{MI1E/B}$			10	dB	$f_C = 900\text{ MHz}$; SSB noise, including optimum noise matching	2

¹⁾ With external resistor at pin 19 according test circuit 1

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AC/DC Characteristics (cont'd)

$T_A = 25\text{ }^\circ\text{C}$; $V_S = 4.75\text{ to }5.25\text{ V}$

Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			

Input for First Local Oscillator LO1/ $\overline{\text{LO1}}$

Input resistance	$R_{\text{LO1}/\overline{\text{LO1}}}$		250		Ω	balanced	3
Input capacitance	$C_{\text{LO1}/\overline{\text{LO1}}}$		2.5		pF	in parallel to $R_{\text{LO1}/\overline{\text{LO1}}}$	3
Input level	$P_{\text{LO1}/\overline{\text{LO1}}}$	-6	-3	0	dBm		1
Input frequency	$f_{\text{LO1}/\overline{\text{LO1}}}$	50		1500	MHz	optimum matched input circuit	1

Output of First Mixer (IF driver input) MO1/ $\overline{\text{MO1}}$ (open collector)

Resistance	$R_{\text{MO1}/\overline{\text{MO1}}}$		37		$\text{k}\Omega$		4
Capacitance	$C_{\text{MO1}/\overline{\text{MO1}}}$		1.8		pF	in parallel to $R_{\text{MO1}/\overline{\text{MO1}}}$	4
Power gain from signal input	G_{MO1}	6	10	14	dB		1
Intermediate frequency	f_{IF}	40		120	MHz	optimum matched output circuit	1

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AC/DC Characteristics (cont'd)

 $T_A = 25\text{ }^\circ\text{C}$; $V_S = 4.75$ to 5.25 V

Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			

Signal Input MI2E/B of Single Balanced Mixer, Emitter Pin 13 AC Grounded
(no input matching network used)

Input resistance	$R_{MI2E/B}$		2.7		k Ω	emitter AC grounded	3
Input capacitance	$C_{MI2E/B}$		4.8		pF	in parallel to $R_{MI2E/B}$	3
Max. input level	P_{MI2max}	-20	-15		dBm	3-dB compression at MO2 referenced to MI2 input	1
Intercept point	P_{IP}	-18	-13		dBm	referenced to MI2 input; IP carrier frequency distance = 20 kHz; $f_C = 44.55\text{ MHz}$	1
Blocking level	P_B	-23	-18		dBm	3-dB attenuation of wanted signal at MO2 referenced to MI2 input; frequency distance = 60 kHz; $f_C = 44.55\text{ MHz}$	1
Input frequency	$f_{MI1E/B}$	40		200	MHz		1
Noise figure	F_{MI2}			10	dB	$f = 45\text{ MHz}$, DSB; $f_{MO2} = 10\text{ MHz}$, noise matching at second mixer input	2
Cross talk attenuation Emitter grounded and cross talk parasites not tuned out	a_{MO1}		87		dB	MO1/X to MI2E/B; $f = 45\text{ MHz}$	5

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AC/DC Characteristics (cont'd)

$T_A = 25\text{ }^\circ\text{C}$; $V_S = 4.75$ to 5.25 V

Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			

Isolation Amplifier LO2/ $\overline{\text{LO2}}$ (no input matching network used)

Input resistance	$R_{\text{LO2}/\overline{\text{LO2}}}$		5.5		k Ω		3
Input capacitance	$C_{\text{LO2}/\overline{\text{LO2}}}$		3.0		pF	in parallel to $R_{\text{LO2}/\overline{\text{LO2}}}$	3
Max input level	P_{LO2max}		- 17	- 10	dBm		1
Frequency range	f_{LO2}	40		120	MHz	with other external circuitry, than test figure 1 and 2	
Second LO first harmonic spurious response suppression below wanted LO at MO2	P_{SPBLO}	20			dB		

Output of Second Mixer MO2 (open collector) with External Pull-up Resistor of 1.5 k Ω

Voltage gain from signal input	G_{MO2}	19	24	29	dB	external $R_L = 1.5\text{ k}\Omega$	1
Intermediate frequency	f_{MO2}	0.30	0.45	1	MHz		1

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AC/DC Characteristics (cont'd)

$T_A = 25\text{ }^\circ\text{C}$; $V_S = 4.75\text{ to }5.25\text{ V}$

Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			

IF Limiter and Demodulator

$\Delta f = \pm 14\text{ kHz}$; $f_i = 450\text{ kHz}$; $Q = 8$; $V_{IF} = 10\text{ mVrms}$; $f_{AO} = 1\text{ kHz}$

Max. input level	$P_{L\text{max}}$			10	dBm		1
IF-limiter gain	G_{MO2}		90		dB	LI to LAO balanced	1
Cross talk attenuation	a_{LI}		90		dB	MO2 to LI; design hint	5
Limiter bandwidth	f_{LI}		500		kHz	$V_{LAO} = -3\text{ dB}$, design hint	1
Limiting threshold	V_{LI}	-92			dBm	$V_{AO} = -3\text{ dB}$; CCITT filter used	2
AM-suppression	a_{AM}	40	45		dB	$m = 0.3$; CCITT filter used	1
Ratio signal to noise	a_{SN}		80		dB	CCITT filter used	1
Noise and hum	a_{NH}			-53	dB	1-kHz tone, $\Delta f = \pm 10\text{ kHz}$	1
Noise and hum	a_{NH}			-33	dB	1-kHz tone, $\Delta f = \pm 10\text{ kHz}$, no CCITT filter	1
Ultimate SINAD		35			dB	CCITT filter used	1

Field Strength Output RSSI ($R_L \geq 100\text{ k}\Omega$, $C_L \leq 50\text{ pF}$)

Output resistance	R_{RSSI}		65		k Ω		1
Field strength factor	F_{RSSI}	36	38	40	mV/ dB		1
RSSI-dynamic range	ΔV_{RSSI}	86	90		dB		1
RSSI intercept with noise floor	IC_{RSSI}		-86		dBm	according diagram	1

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AC/DC Characteristics (cont'd)
 $T_A = 25\text{ °C}; V_S = 4.75\text{ to }5.25\text{ V}$

Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			

Signal Outputs AO ($R_L \geq 50\text{ k}\Omega$, $C_L \leq 10\text{ pF}$)

Audio bandwidth	BW_{AO}		20		kHz	3 dB roll-off value $\Delta f_{FM} = \pm 10\text{ kHz}$; HPF = 300 Hz; LPF = 200 kHz	1
Audio output voltage according CCITT	V_{AO}		390		mVr ms	LC tank circuit; Q = 8; $\Delta f_{FM} = \pm 10\text{ kHz}$ fixed $T_A = 25\text{ °C}$,	1
Audio output voltage according CCITT	V_{AO}		390		mVr ms	LC tank circuit; Q = 8; $\Delta f_{FM} = \pm 10\text{ kHz}$ $T_A = -25...+80\text{ °C}$	1
Distortion factor	THD		1.3	2.2	%	$\Delta f_{FM} = \pm 10\text{ kHz}$; HPF = 300 Hz, LPF = 20 Hz, $f_{AO} = 1\text{ kHz}$	1
Output resistance	R_{AO}		1	2	k Ω	design hint	
DC output level	V_{AO}		2.3		V	depend on LC tank circuit; design hint	1

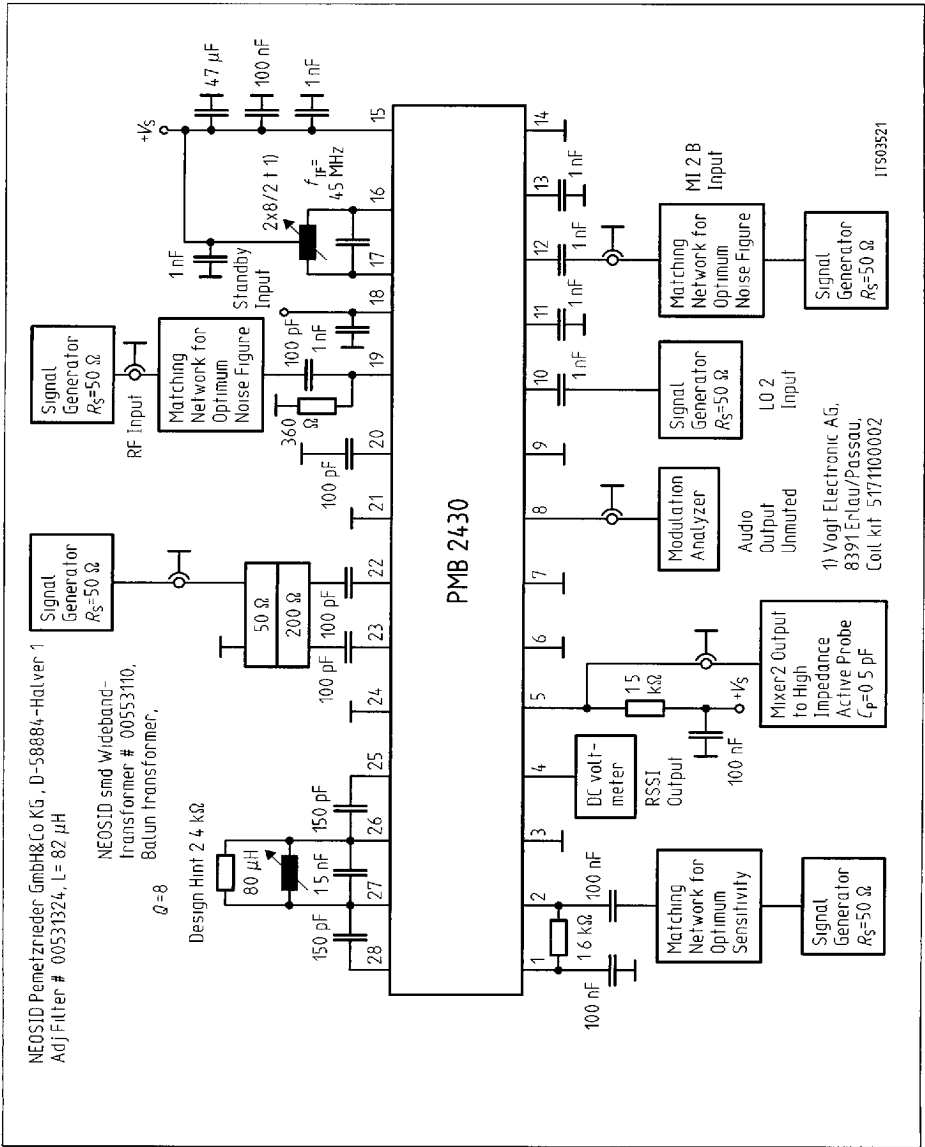
Stand-by Switch

Low-input voltage	V_{STB}	0		0.8	V		1
Low-input current	I_{STB}			- 50	μA		1
High-input voltage	V_{STB}	3		V_S	V		1
High-input current	I_{STB}			200	μA		1

Notes

- Parameters for balanced inputs and outputs refer to the differential mode signal
- Input and output impedances (design hints) are modelled as a resistor in parallel with a capacitor or in series to an inductor. Measurements have been done with Siemens test boards.

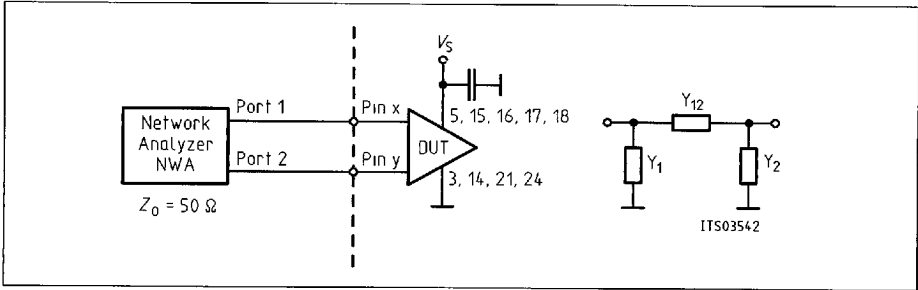
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Test Circuit 2

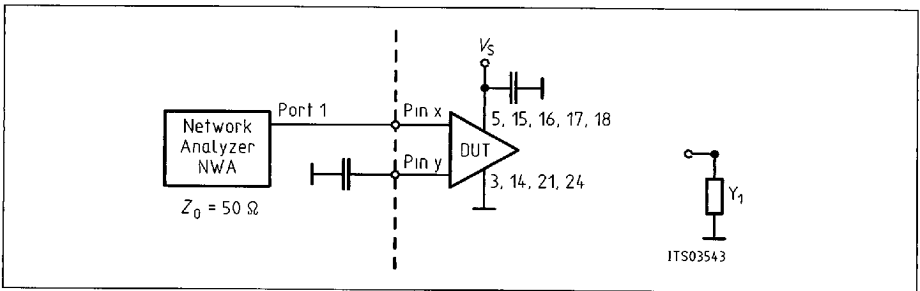
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Test Circuit 3a

The S parameters are tested at the indicated frequency and the equivalent parallel or series circuit is calculated on this base.



Test Circuit 3b

* Capacitor used for Mixer 1 measurement only

The S parameters are tested at the indicated frequency and the equivalent parallel or series circuit is calculated on this base.

Test Point	T.C.	Test Frequency/MHz	Pin x	Pin y
LO1-input impedance	3a	900	22	23
Mixer 1-input impedance	3b	945	19	20
LO2-input impedance	3b	45	10	11
Mixer 2-input impedance	3b	45	12	13

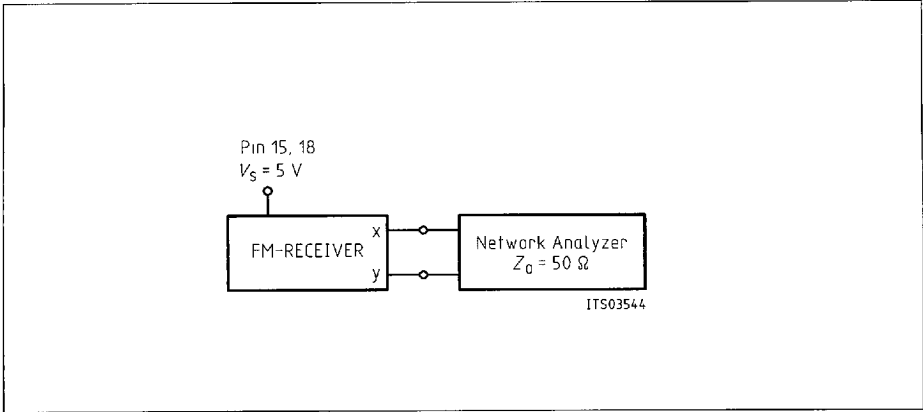
Network Analyzer output level: - 3 dBm for LO1 measurement

Measurement circuitry according test circuit 1: - 30 dB else

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Open collector pins are connected to $V_S = 5\text{ V}$ via the network analyzer;
 Other test circuitry according test circuit 1.

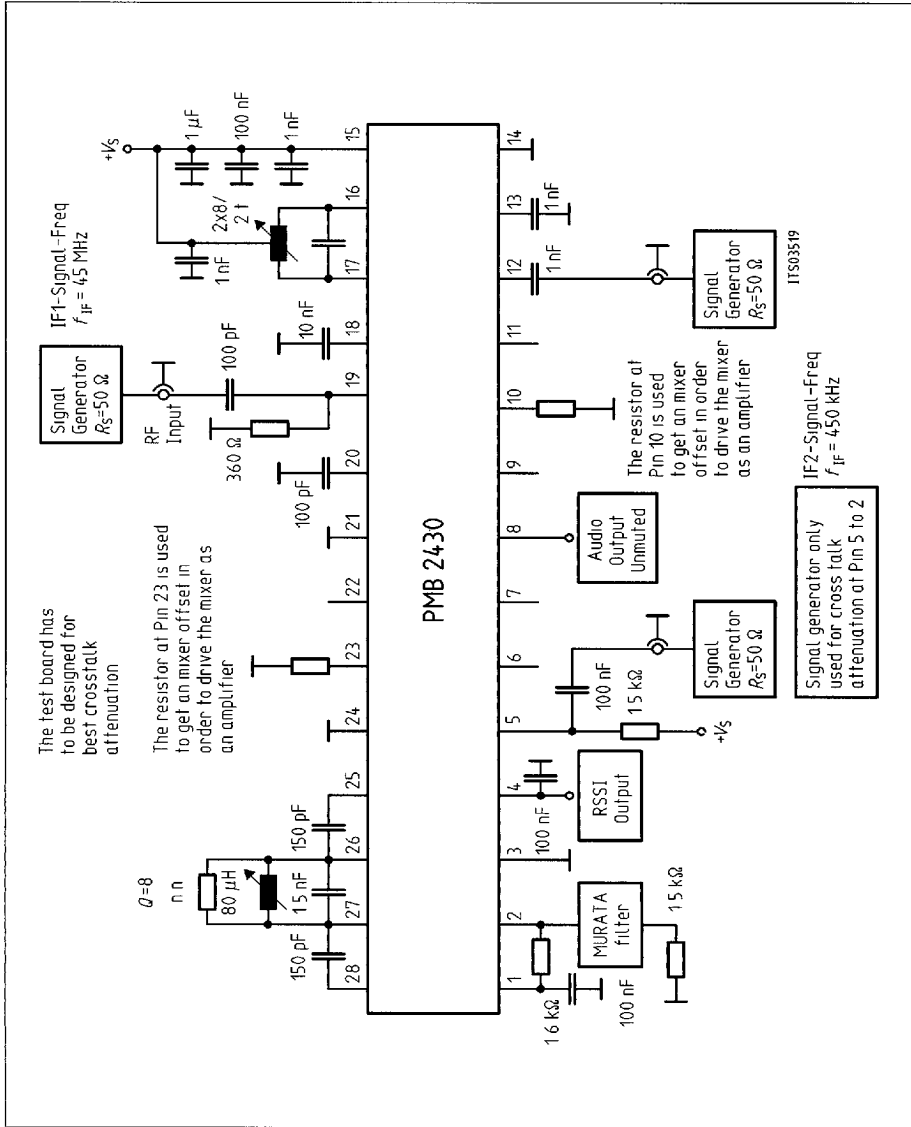


Test Circuit 4

The S parameters are tested at the indicated frequency and the equivalent parallel or series circuit is calculated on this base. The network analyzer output level for this measurement should be -14dB.

Test Point	Test Frequency/MHz	Pin x	Pin y
MO1 mixer 1 output impedance	45	16	17

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Test Circuit 5

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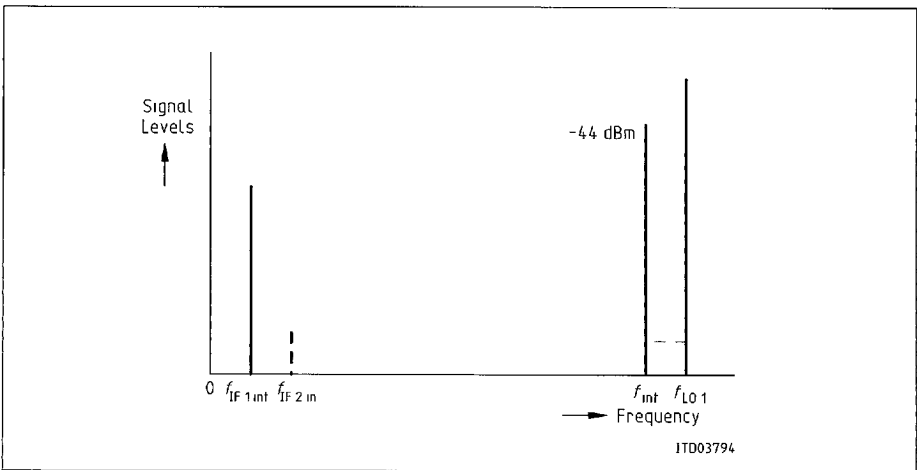
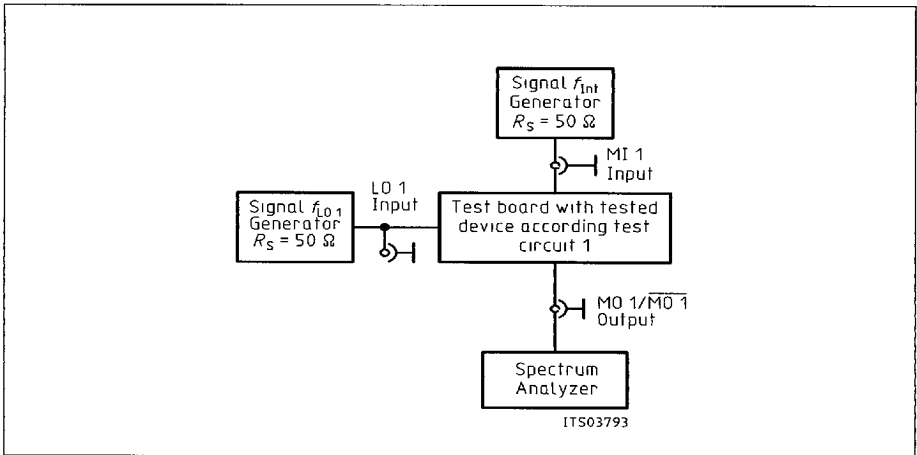
Test procedure for cross talk attenuation at pin 5 to 2:

1. Apply a signal as specified at pin 5 and measure RSSI voltage.
2. Compare RSSI DC-level with an earlier measurement with an 450-kHz signal direct capacitively applied to pin 2 according test circuit 1.
3. Calculate cross talk value out of this results.

Test procedure for cross talk attenuation at pin 16, 17 to 12:

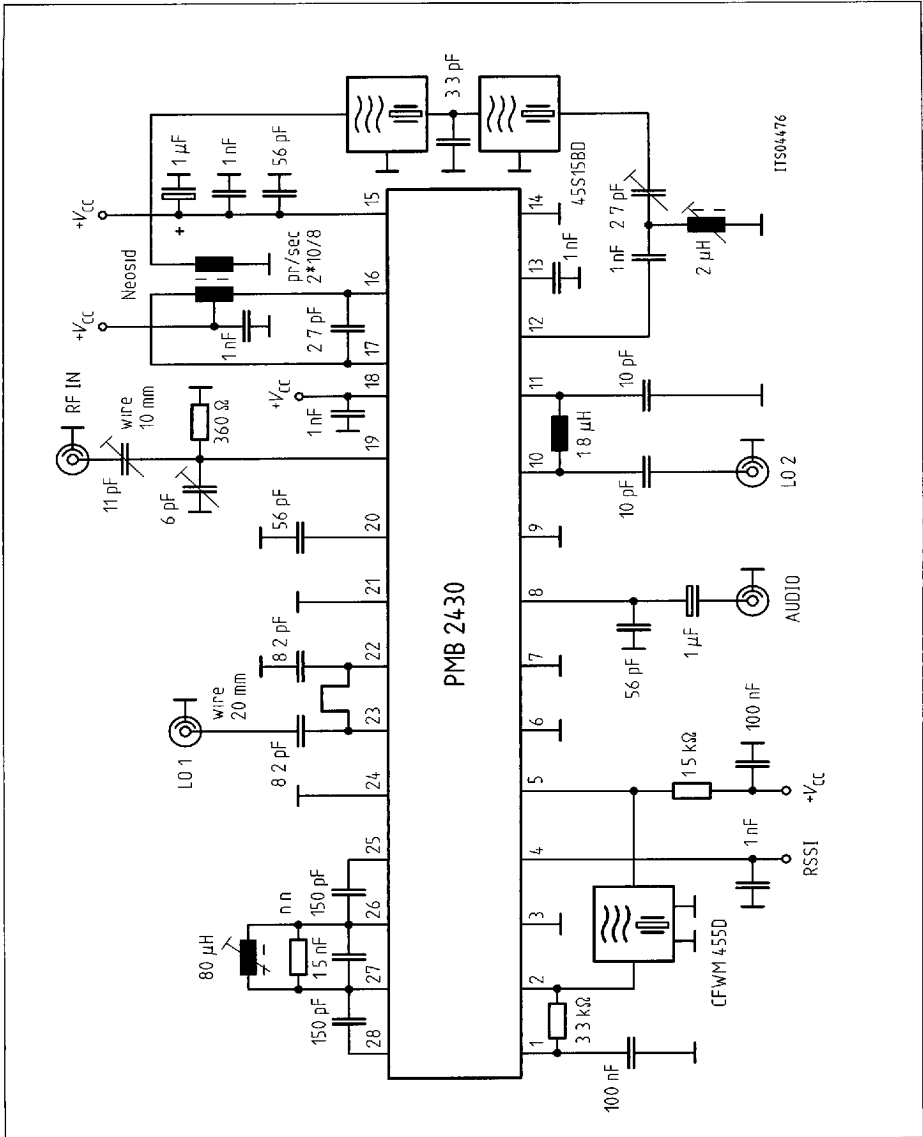
1. Apply a signal at pin 12 and measure with high impedance probe level at pin 5.
2. Apply a signal at pin 19 and measure with high impedance probe level at pin 5. Increase level to achieve the same output level as at point 1.
3. Measure with high impedance probe balanced level at pin 16, 17.
4. Calculate cross talk attenuation out of level differences.

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Test Circuit 6

- f_{int} = unwanted interfering signal within band: $f_{int} = f_{LO1} - f_{IF2}$
- f_{LO1} = local oscillator signal
- f_{IFint} = unwanted IF/2 signal from interfering channel: $f_{IFint} = f_{LO1} - f_{int}$
- f_{IF2n} = unwanted harmonic signal of f_{IFint} : $f_{IF2n} = 2 \times f_{IFint}$



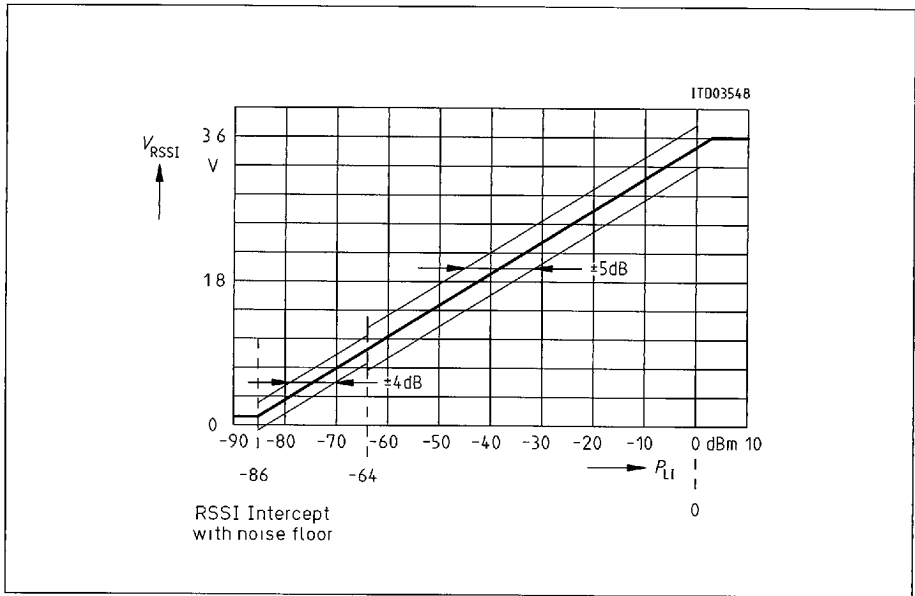
Application Circuit

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Diagram

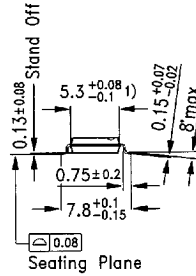
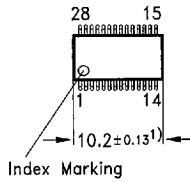
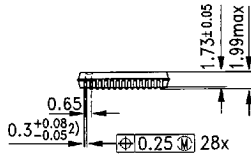


RSSI-Response

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Plastic-Package, P-DSO-28-4 (Shrink) (SMD)
 (Dual-Small-Outlines)



- 1) Does not include plastic or metal protrusions of 0.15 max per side
- 2) Does not include dambar protrusion of 0.08 max per side

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Sorts of Packing

Package outlines for tubes, trays etc. are contained in our Data Book "Package Information"

SMD = Surface Mounted Device

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Dimensions in mm

B111-H6712-
G2-X-7600