8-Channel Programmable, Parallelable 1A Buck DC/DCs

FEATURES

- **8-Channel Independent Step-Down DC/DCs**
- **Master-Slave Configurable for Up to 4A Per Output Channel with a Single Inductor**
- **Independent V_{IN} Supply for Each DC/DC (2.25V to 5.5V)**
- **All DC/DCs Have 0.425V to V_{IN} Output Voltage Range**
- **Precision Enable Pin Thresholds for Autonomous Sequencing (or I²C Control)**
- 1MHz to 3MHz Programmable/Synchronizable Oscillator Frequency (2MHz Default)
- I²C Selectable Phasing (90° Steps) Per Channel
- Programmable Power-On Reset/Watch Dog/ Pushbutton Timing
- Die Temperature Monitor Output
- 48-Lead (7mm × 7mm) QFN Package

APPLICATIONS

- General Purpose Multichannel Power Supplies
- Industrial/Automotive/Communications

DESCRIPTION

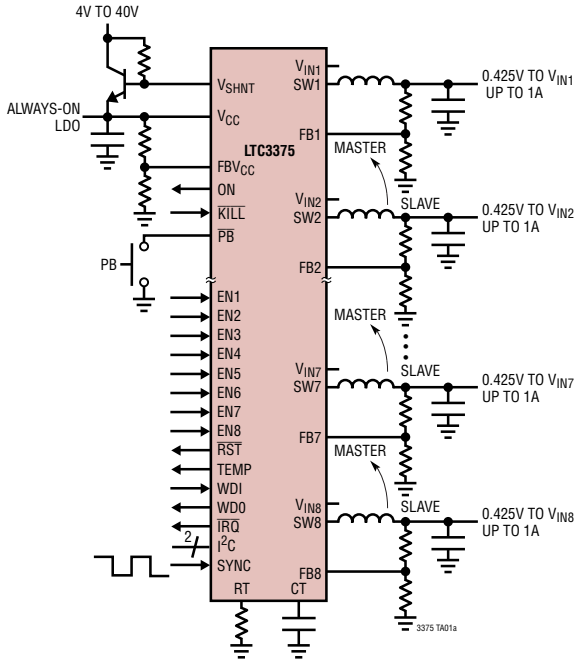
The LTC®3375 is a digitally programmable high efficiency multioutput power supply IC. The DC/DCs consist of eight synchronous buck converters (I_{OUT} up to 1A each) all powered from independent 2.25V to 5.5V input supplies.

DC/DC enables, output voltages, operating modes, and phasing may all be independently programmed over I²C or used in standalone mode via simple I/O with power-up defaults. The DC/DCs may be used independently or in parallel to achieve higher output currents of up to 4A per output with a shared inductor. Alarm levels for high die temperature may also be programmed via I²C with a maskable $\overline{IRQ}$ output for monitoring DC/DC and system faults.

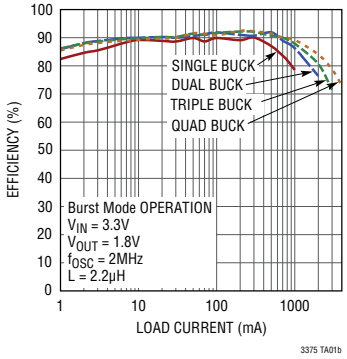
Pushbutton ON/OFF/RESET control, power-on reset, and a watchdog timer provide flexible and reliable power-up sequencing and system monitoring. The LTC3375 is available in a low profile 48-lead 7mm × 7mm QFN package.

TYPICAL APPLICATION

8-Channel 1A Multioutput Buck Regulator



Buck Efficiency vs Load



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ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN1-8}, FB1-8, EN1-8, V_{CC}, V_{SHNT}, FBV_{CC}, CT, ON, $\overline{KILL}$, $\overline{IRQ}$, $\overline{RST}$, $\overline{PB}$, WDI, WDO, SYNC, RT, SDA, SCL ..... –0.3V to 6V

TEMP .....–0.3V to Lesser of (V_{CC} + 0.3V) or 6V

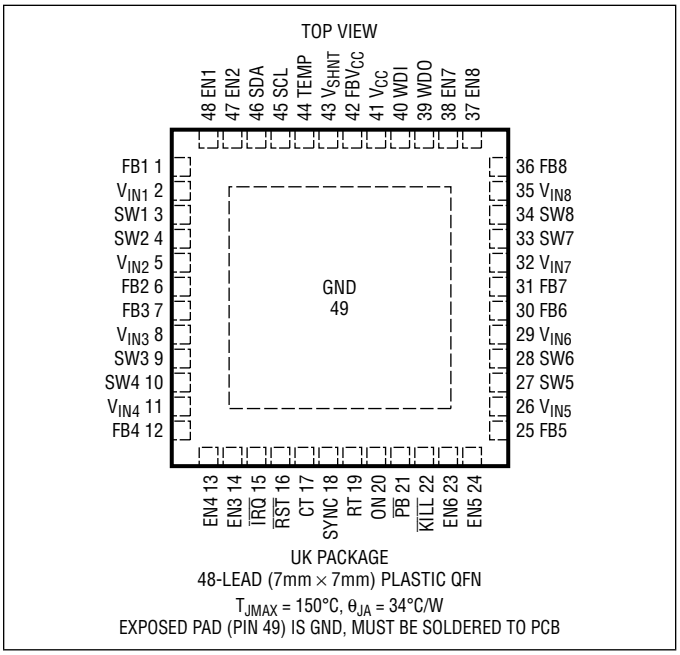
$I_{\overline{IRQ}}$, $I_{\overline{RST}}$, I_{WDO}, I_{ON} 5mA

I_{VSHNT} 3mA

Operating Junction Temperature Range (Notes 2, 3) ..... –40°C to 150°C

Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



UK PACKAGE
48-LEAD (7mm × 7mm) PLASTIC QFN

T_{JMAX} = 150°C, θ_{JA} = 34°C/W

EXPOSED PAD (PIN 49) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3375EUK#PBF	LTC3375EUK#TRPBF	LTC3375UK	48-Lead (7mm × 7mm) Plastic QFN	–40°C to 125°C
LTC3375IUK#PBF	LTC3375IUK#TRPBF	LTC3375UK	48-Lead (7mm × 7mm) Plastic QFN	–40°C to 125°C
LTC3375HUK#PBF	LTC3375HUK#TRPBF	LTC3375UK	48-Lead (7mm × 7mm) Plastic QFN	–40°C to 150°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{CC} = V_{IN1-8} = 3.3V, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{VCC}	V_{CC} Voltage Range		●	2.7		5.5	V
V_{VCC_UVLO}	Undervoltage Threshold on V_{CC}	V_{CC} Voltage Falling V_{CC} Voltage Rising	● ●	2.35 2.45	2.45 2.55	2.55 2.65	V V
I_{VCC_ALLOFF}	V_{CC} Input Supply Current	All Switching Regulators in Shutdown, $\overline{PB}$ = HIGH			11	25	µA
I_{VCC}	V_{CC} Input Supply Current	At Least 1 Buck Active, SYNC = 0V, R_T = 400k, V_{FB_BUCK} = 0.85V At Least 1 Buck Active, SYNC = 2MHz			50 200	85 325	µA µA
f_{OSC}	Internal Oscillator Frequency	V_{RT} = V_{CC}, SYNC = 0V V_{RT} = V_{CC}, SYNC = 0V R_{RT} = 400k, SYNC = 0V	 ● ●	1.8 1.75 1.8	2 2 2	2.2 2.25 2.2	MHz MHz MHz
f_{SYNC}	Synchronization Frequency	t_{LOW}, t_{HIGH} > 40ns		1		3	MHz
V_{SYNC}	SYNC Level High SYNC Level Low		● ●	1.2		 0.4	V V
V_{RT}	RT Servo Voltage	R_{RT} = 400k	●	780	800	820	mV
Temperature Monitor							
$V_{TEMP(ROOM)}$	TEMP Voltage at 25°C				150		mV
ΔV_{TEMP}/°C	V_{TEMP} Slope		●		6.75		mV/°C
OT	Overtemperature Shutdown	Temperature Rising			165		°C
OT_HYST	Overtemperature Hysteresis				10		°C
DT_WARN	Die Temperature Warning Threshold (Die Temperature that Causes $\overline{IRQ}$ = 0)	DT[1], DT[0] = 00 DT[1], DT[0] = 01 DT[1], DT[0] = 10 DT[1], DT[0] = 11			Inactive 140 125 110		 °C °C °C
1A Buck Regulators							
V_{BUCK}	Buck Input Voltage Range		●	2.25		5.5	V
V_{OUT}			●	V_{FB}		V_{IN}	V
V_{IN_UVLO}	Undervoltage Threshold on V_{IN}	V_{IN} Voltage Falling V_{IN} Voltage Rising	● ●	1.95 2.05	2.05 2.15	2.15 2.25	V V
I_{VIN_BUCK}	Burst Mode® Operation Forced Continuous Mode Operation Shutdown Input Current Shutdown Input Current	V_{FB_BUCK} = 0.85V (Note 4) I_{SW_BUCK} = 0µA, V_{FB_BUCK} = 0V All Switching Regulators in Shutdown At Least One Other Buck Active			18 400 0 1	50 550 1 2	µA µA µA µA
I_{FWD}	PMOS Current Limit	(Note 5)		2.0	2.3	2.7	A
V_{FB} (Default)	Feedback Regulation Voltage	Forced Continuous Mode Default (1, 1, 0, 0)	●	705	725	745	mV
V_{FB} (High)	Feedback Regulation Voltage	Forced Continuous Mode Full Scale (1, 1, 1, 1)	●	780	800	820	mV
V_{FB} (Low)	Feedback Regulation Voltage	Forced Continuous Mode Zero Scale (0, 0, 0, 0)	●	405	425	445	mV
V_{LSB}	V_{FB} Servo Voltage Step Size				25		mV
I_{FB}	Feedback Leakage Current	V_{FB_BUCK} = 0.85V		–50		50	nA
DMAX	Maximum Duty Cycle	V_{FB_BUCK} = 0V	●	100			%
R_{PMOS}	PMOS On-Resistance	I_{SW_BUCK} = 100mA			265		mΩ
R_{NMOS}	NMOS On-Resistance	I_{SW_BUCK} = –100mA			280		mΩ
I_{LEAKP}	PMOS Leakage Current	EN_BUCK = 0		–2		2	µA
I_{LEAKN}	NMOS Leakage Current	EN_BUCK = 0		–2		2	µA
R_{SWPD}	Output Pull-Down Resistance in Shutdown	EN_BUCK = 0 (I^2C Bit Set)			1		kΩ
t_{SS}	Soft-Start Time	Default (1, 1, 0, 0) Reference Voltage			1		ms

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{CC} = V_{IN1-8} = 3.3V, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{PGOOD(FALL)}$	Falling PGOOD Threshold Voltage	Full-Scale (1, 1, 1, 1) Reference Voltage			92.5		%
$V_{PGOOD(HYS)}$	PGOOD Hysteresis				1		%
Buck Regulators Combined							
I_{FWD2}	PMOS Current Limit	2 Buck Converters Combined (Note 5)			4.6		A
I_{FWD3}	PMOS Current Limit	3 Buck Converters Combined (Note 5)			6.9		A
I_{FWD4}	PMOS Current Limit	4 Buck Converters Combined (Note 5)			9.2		A
V_{CC} Regulator							
V_{FBVCC}	FBV_{CC} Regulation Voltage			1.17	1.2	1.23	V
R_{REG}	Pull-Down Resistance for V_{CC} (Regulator)				200		Ω
V_{VSHNT_MAX}	V_{SHNT} Clamp Voltage	I_{SHNT} = 2mA, FBV_{CC} = 0V			6.1		V
R_{CLAMP}	Pull-Down Resistance for V_{SHNT} (Clamp)				200		Ω
I^2C Port							
ADDRESS	I^2C Address		●		0110100[R/WB]		
V_{IH}	Input High Voltage	SDA/SCL	●	1.2			V
V_{IL}	Input Low Voltage	SDA/SCL	●			0.4	V
I_{IH}	Input High Current	SDA/SCL				50	nA
I_{IL}	Input Low Current	SDA/SCL				50	nA
V_{OL_SDA}	SDA Output Low Voltage	I_{SDA} = 3mA				0.4	V
f_{SCL}	Clock Operating Frequency					400	kHz
t_{BUF}	Bus Free Time Between Stop and Start Condition			1.3			µs
t_{HD_SDA}	Hold Time After Repeated Start Condition			0.6			µs
t_{SU_STA}	Repeated Start Condition Set-Up Time			0.6			µs
t_{SU_STO}	Stop Condition Set-Up Time			0.6			µs
$t_{HD\_DAT(O)}$	Data Hold Time Output			0		900	ns
$t_{HD\_DAT(I)}$	Data Hold Time Input			0			ns
t_{SU_DAT}	Data Set-Up Time			250			ns
t_{LOW}	SCL Clock Low Period			1.3			µs
t_{HIGH}	SCL Clock High Period			0.6			µs
t_f	Clock/Data Fall Time	C_B = Capacitance of One Bus Line (pF)		$20+0.1C_B$		300	ns
t_r	Clock/Data Rise Time	C_B = Capacitance of One Bus Line (pF)		$20+0.1C_B$		300	ns
Interface Logic Pins (ON, $\overline{KILL}$, $\overline{RST}$, $\overline{IRQ}$, $\overline{PB}$, WDI, WDO)							
I_{OH}	Output High Leakage Current	ON, $\overline{RST}$, $\overline{IRQ}$, WDO 5.5V at Pin		-1		1	µA
V_{OL}	Output Low Voltage	ON, $\overline{RST}$, $\overline{IRQ}$, WDO 3mA Into Pin			0.1	0.4	V
V_{IH}	Input High Threshold	$\overline{KILL}$, $\overline{PB}$, WDI	●	1.2			V
V_{IL}	Input Low Threshold	$\overline{KILL}$, $\overline{PB}$, WDI	●			0.4	mV
t_{WDI}	Time From Last WDI				1.5		sec
t_{WDO}	WDO Low Time Absent a Transition at WDI				200		ms
$t_{WDRESET}$	Time From a WDI Transition Until the WD Timer Is Reset					2	µs

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{CC} = V_{IN1-8} = 3.3V, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Interface Logic Pins (EN1, EN2, EN3, EN4, EN5, EN6, EN7, EN8)							
V_{HI_ALLOFF}	Enable Rising Threshold	All Regulators Disabled	●	400	730	1200	mV
V_{EN_HYS}	Enable Hysteresis				60		mV
V_{HI}	Enable Rising Threshold	At Least One Regulator Enabled	●	380	400	420	mV
I_{EN}	Enable Pin Leakage Current	EN = V_{CC} = V_{IN} = 5.5V		–1		1	µA
Pushbutton Parameters, C_T = 0.01µF							
$t_{\overline{PB}\_LO}$	$\overline{PB}$ Low Time to $\overline{IRQ}$ Low	ON High		28	50	72	ms
$t_{\overline{PB}\_ON}$	$\overline{PB}$ Low Time to ON High			140	200	260	ms
$t_{\overline{PB}\_OFF}$	$\overline{PB}$ Low to ON Forced Low			7	10	13	sec
t_{HR}	Time for Which All Enabled Regulators Are Disabled After $\overline{KILL}$ is Asserted High	ON High		0.7	1	1.3	sec
$t_{\overline{IRQ}\_PW}$	$\overline{IRQ}$ Minimum Pulse Width	ON High		28	50	72	ms
$t_{\overline{KILL}H}$	Time in Which $\overline{KILL}$ Must Be Asserted High	After ON Rising Edge		7	10	13	sec
$t_{\overline{KILL}L}$	$\overline{KILL}$ Low Time to ON Low	ON High		28	50	72	ms
$t_{\overline{RST}}$	$\overline{RST}$ Assertion Delay			160	230	300	ms

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3375 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3375E is guaranteed to meet specifications from 0°C to 85°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3375I is guaranteed over the –40°C to 125°C operating junction temperature range. The LTC3375H is guaranteed over the –40°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes; operating lifetime is derated for junction temperatures greater than 125°C. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors. The junction temperature (T_J in °C) is calculated from the ambient temperature (T_A in °C) and power dissipation (P_D in Watts) according to the formula:

$$T_J = T_A + (P_D \bullet \theta_{JA})$$

where θ_{JA} (in °C/W) is the package thermal impedance.

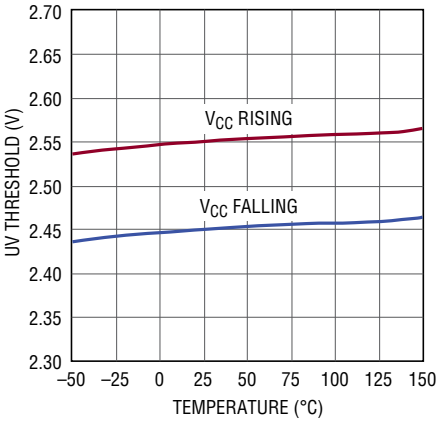
Note 3: The LTC3375 includes overtemperature protection which protects the device during momentary overload conditions. Junction temperatures will exceed 150°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 4: Static current, switches not switching. Actual current may be higher due to gate charge losses at the switching frequency.

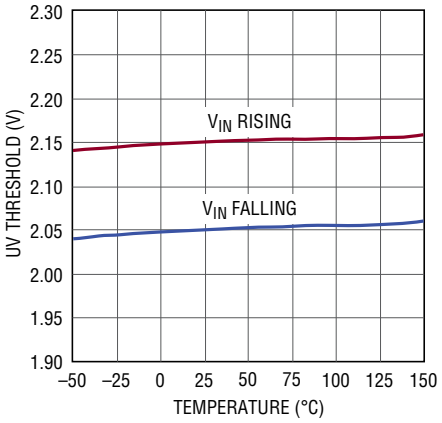
Note 5: The current limit features of this part are intended to protect the IC from short term or intermittent fault conditions. Continuous operation above the maximum specified pin current rating may result in device degradation over time.

TYPICAL PERFORMANCE CHARACTERISTICS

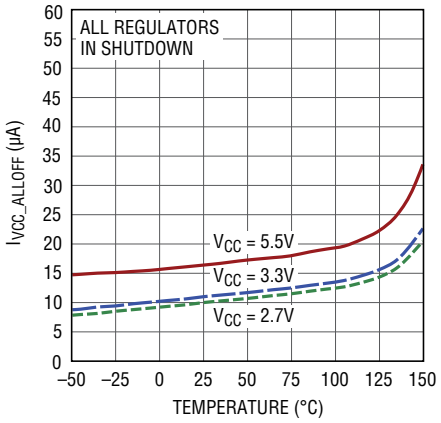
V_{CC} Undervoltage Threshold vs Temperature



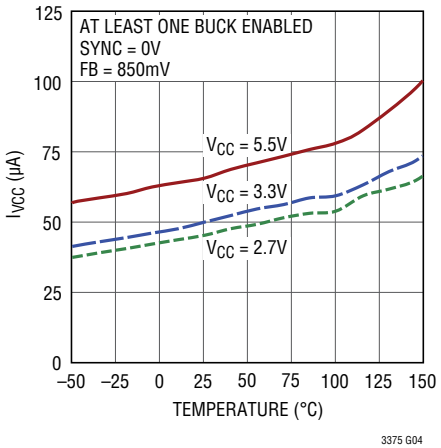
Buck V_{IN} Undervoltage Threshold vs Temperature



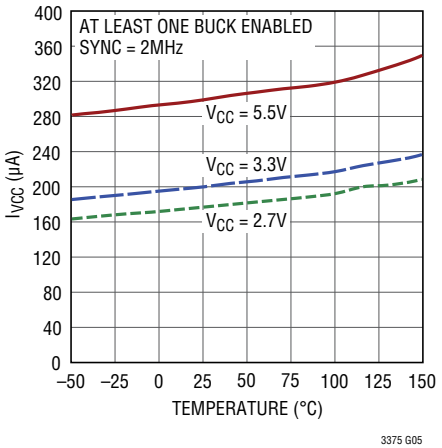
V_{CC} Supply Current vs Temperature



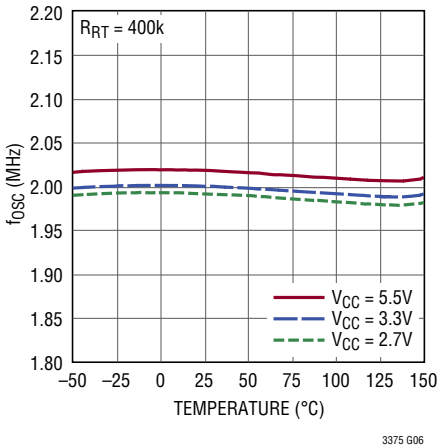
V_{CC} Supply Current vs Temperature



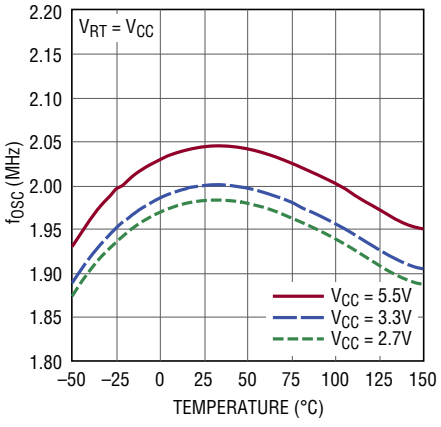
V_{CC} Supply Current vs Temperature



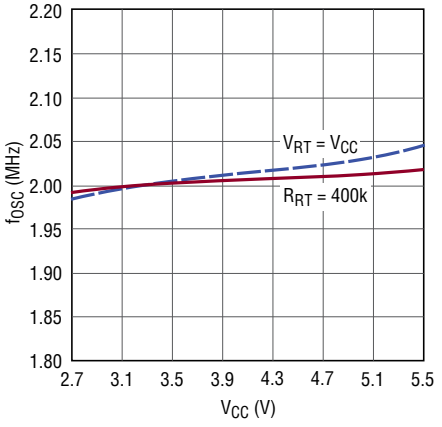
RT Programmed Oscillator Frequency vs Temperature



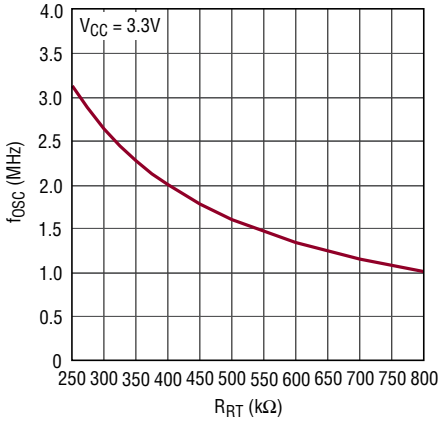
Default Oscillator Frequency vs Temperature



Oscillator Frequency vs V_{CC}

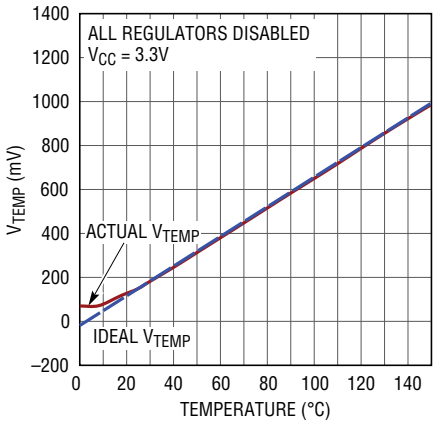


Oscillator Frequency vs R_T



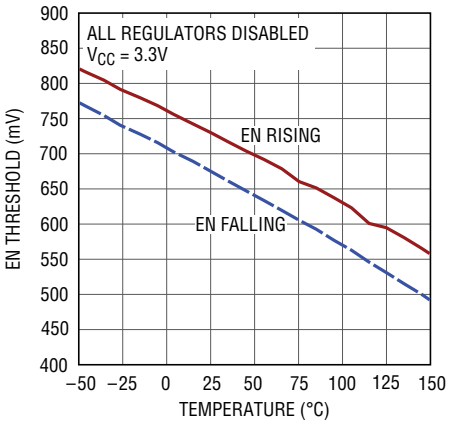
TYPICAL PERFORMANCE CHARACTERISTICS

V_{TEMP} vs Temperature



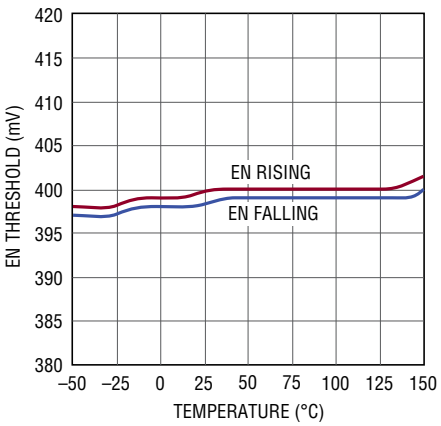
3375 G10

Enable Threshold vs Temperature



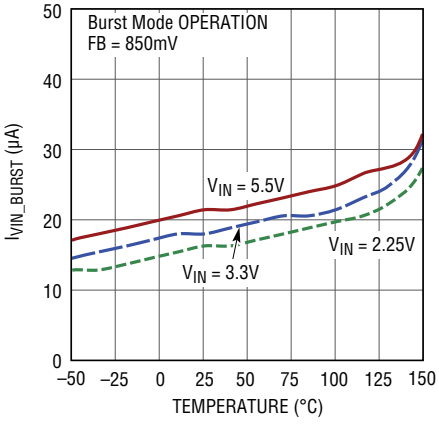
3375 G11

Enable Pin Precision Threshold vs Temperature



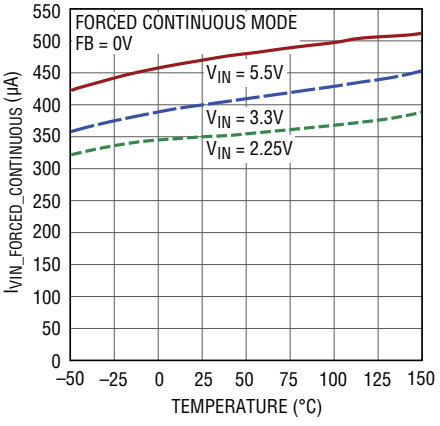
3375 G12

Buck V_{IN} Supply Current vs Temperature



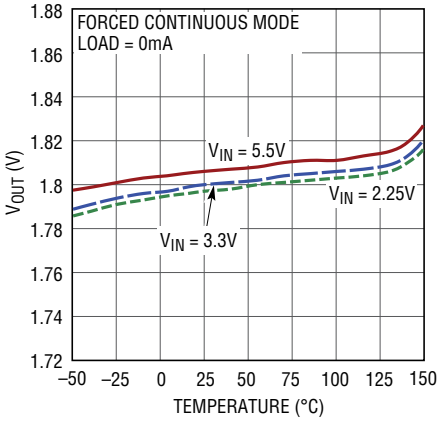
3375 G13

Buck V_{IN} Supply Current vs Temperature



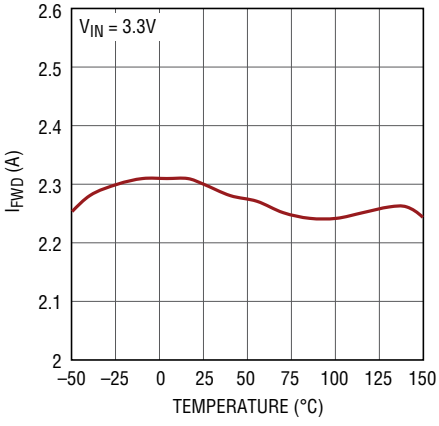
3375 G14

V_{OUT} vs Temperature



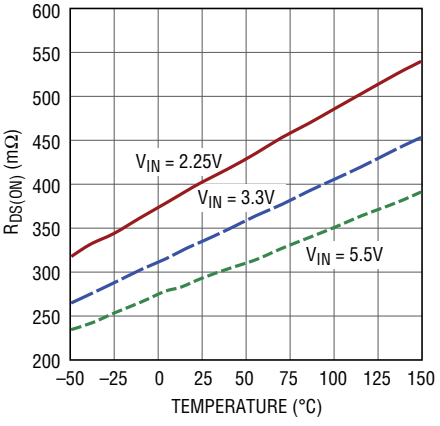
3375 G15

PMOS Current Limit vs Temperature



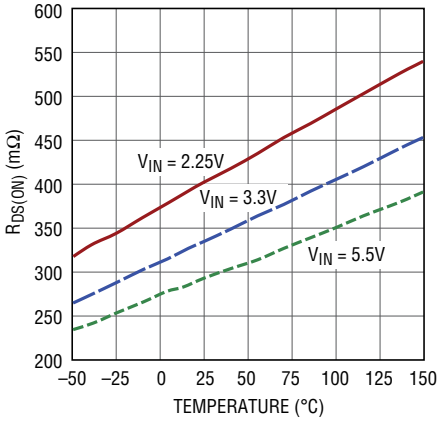
3375 G16

PMOS $R_{DS(ON)}$ vs Temperature



3375 G17

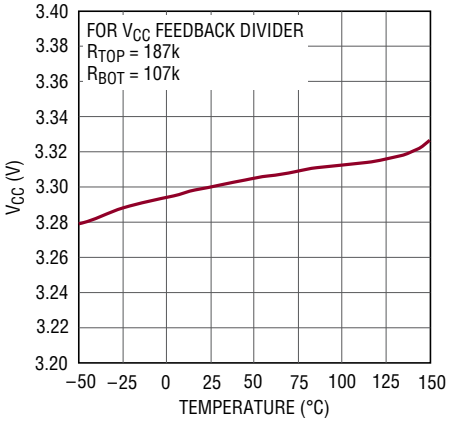
NMOS $R_{DS(ON)}$ vs Temperature



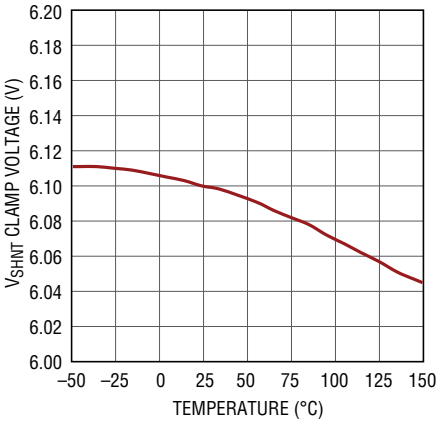
3375 G18

TYPICAL PERFORMANCE CHARACTERISTICS

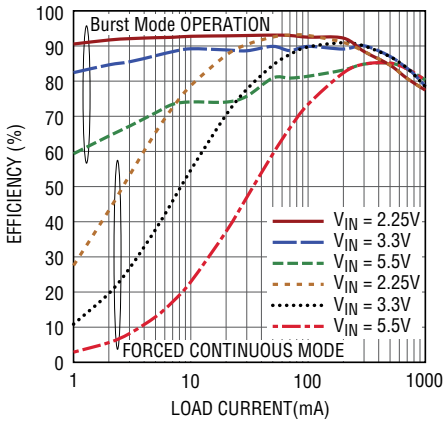
V_{CC} vs Temperature



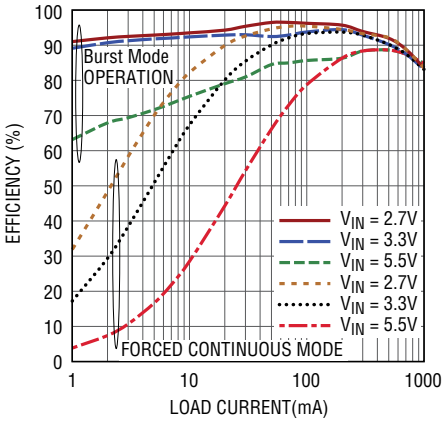
V_{SHNT} Clamp Voltage vs Temperature



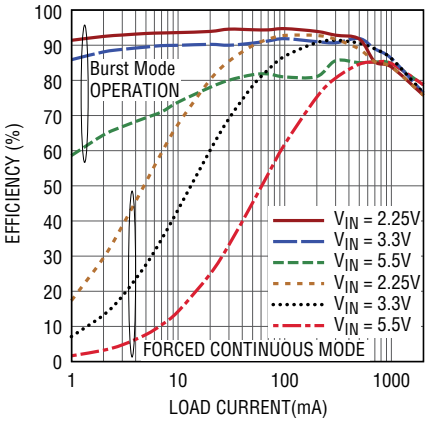
1A Buck Efficiency vs I_{LOAD}



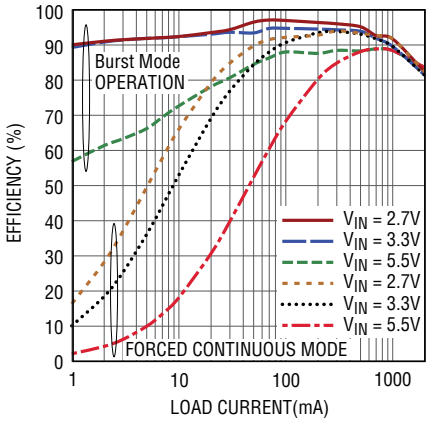
1A Buck Efficiency vs I_{LOAD}



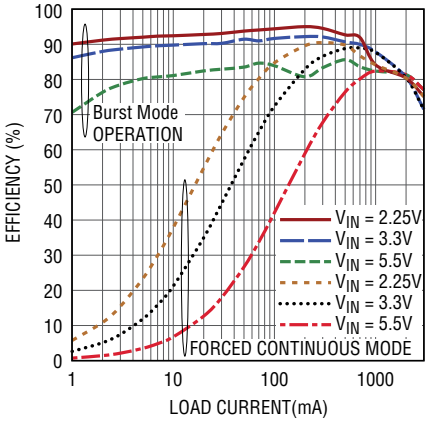
2A Buck Efficiency vs I_{LOAD}



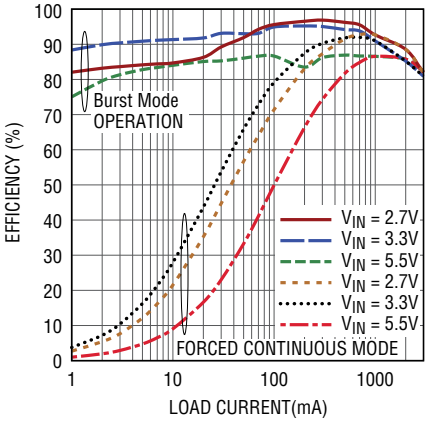
2A Buck Efficiency vs I_{LOAD}



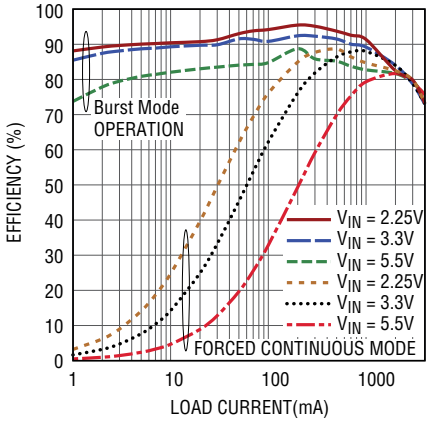
3A Buck Efficiency vs I_{LOAD}



3A Buck Efficiency vs I_{LOAD}

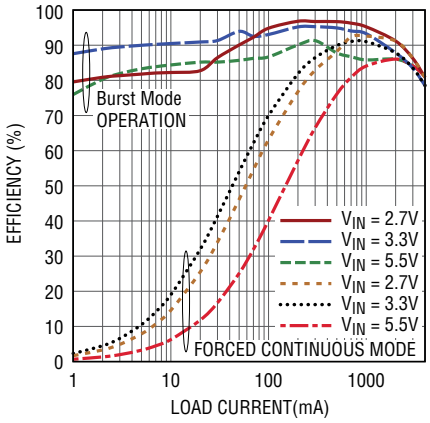


4A Buck Efficiency vs I_{LOAD}

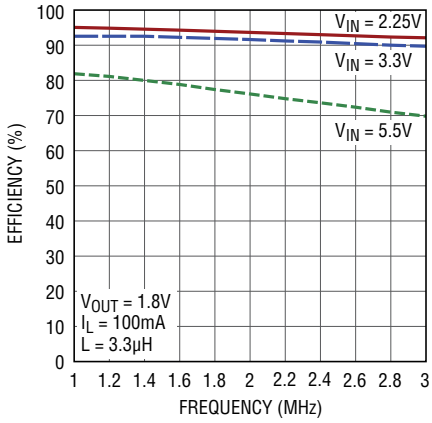


TYPICAL PERFORMANCE CHARACTERISTICS

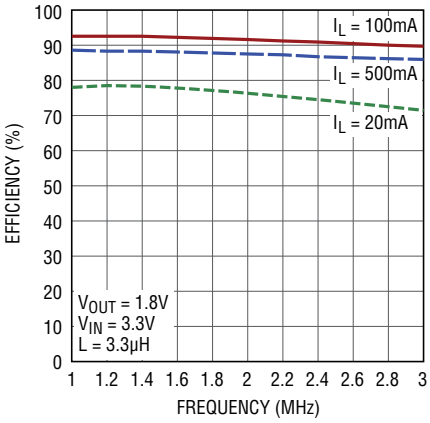
4A Buck Efficiency vs I_{LOAD}



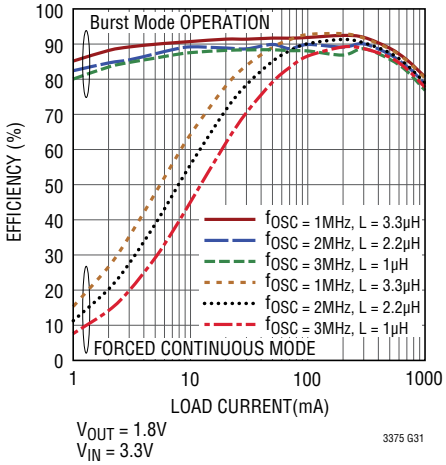
1A Buck Efficiency vs Frequency (Forced Continuous Mode)



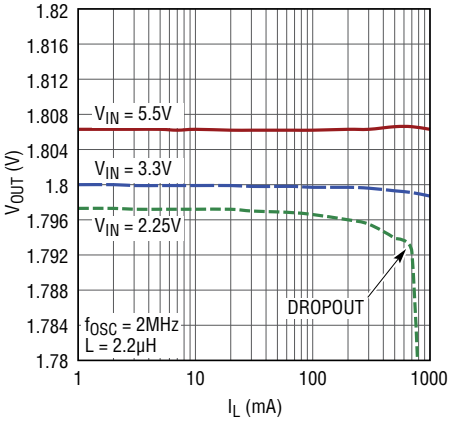
1A Buck Efficiency vs Frequency (Forced Continuous Mode)



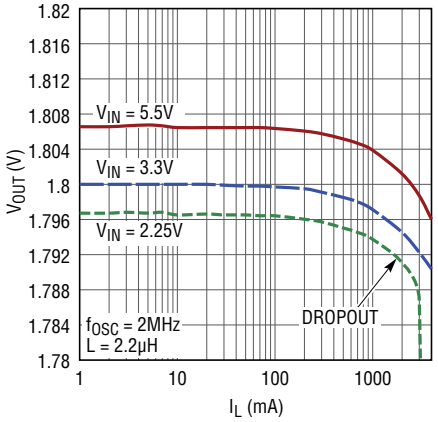
1A Buck Efficiency vs I_{LOAD} (Across Operating Frequency)



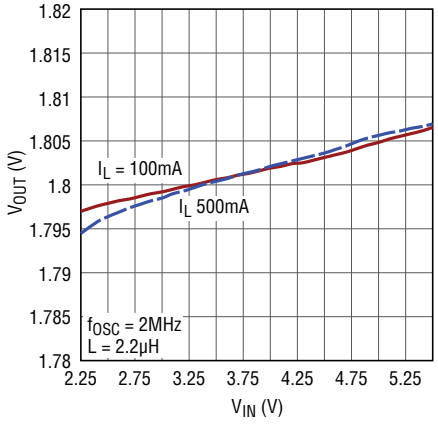
1A Buck Regulator Load Regulation (Forced Continuous Mode)



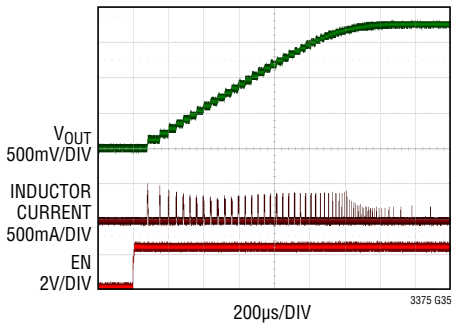
4A Buck Regulator Load Regulation (Forced Continuous Mode)



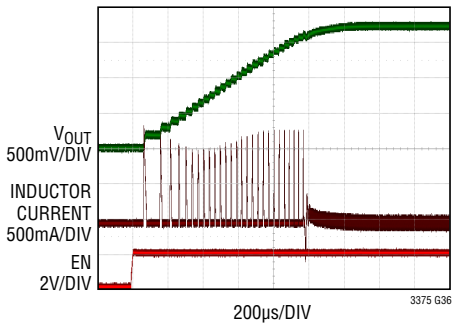
1A Buck Regulator Line Regulation (Forced Continuous Mode)



1A Buck Regulator No Load Startup Transient (Burst Mode)

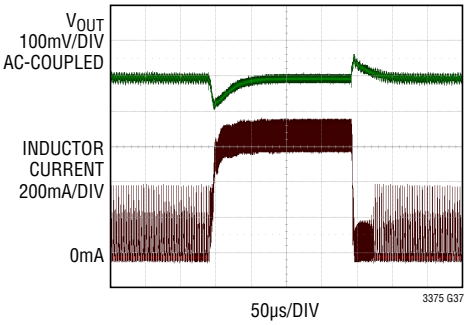


4A Buck Regulator No Load Startup Transient (Forced Continuous Mode)



TYPICAL PERFORMANCE CHARACTERISTICS

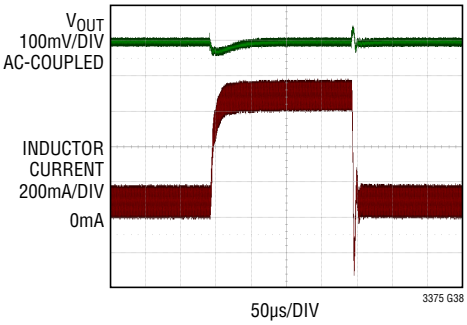
1A Buck Regulator, Transient Response (Burst Mode)



50µs/DIV

LOAD STEP = 100mA TO 700mA
V_{IN} = 3.3V, V_{OUT} = 1.8V

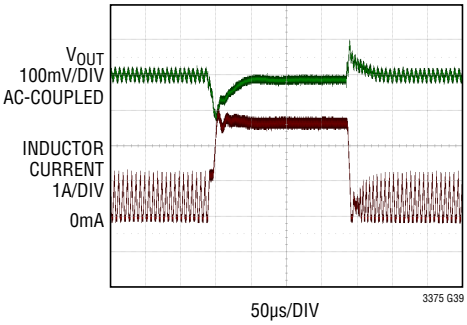
1A Buck Regulator, Transient Response (Forced Continuous Mode)



50µs/DIV

LOAD STEP = 100mA TO 700mA
V_{IN} = 3.3V, V_{OUT} = 1.8V

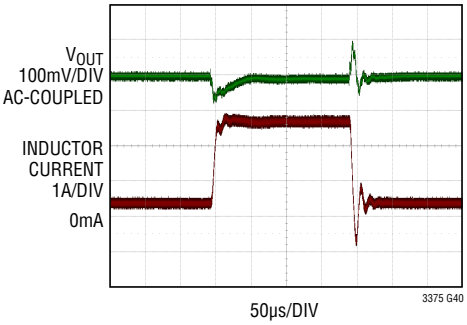
4A Buck Regulator, Transient Response (Burst Mode)



50µs/DIV

LOAD STEP = 100mA TO 2.8A
V_{IN} = 3.3V, V_{OUT} = 1.8V

4A Buck Regulator, Transient Response (Forced Continuous Mode)



50µs/DIV

LOAD STEP = 400mA TO 2.8A
V_{IN} = 3.3V, V_{OUT} = 1.8V

PIN FUNCTIONS

FB1 (Pin 1): Buck Regulator 1 Feedback Pin. Receives feedback by a resistor divider connected across the output.

V_{IN1} (Pin 2): Buck Regulator 1 Input Supply. Bypass to GND with a 10µF or larger ceramic capacitor.

SW1 (Pin 3): Buck Regulator 1 Switch Node. External inductor connects to this pin.

SW2 (Pin 4): Buck Regulator 2 Switch Node. External inductor connects to this pin.

V_{IN2} (Pin 5): Buck Regulator 2 Input Supply. Bypass to GND with a 10µF or larger ceramic capacitor. May be driven by an independent supply or must be shorted to V_{IN1} when buck regulator 2 is combined with buck regulator 1 for higher current.

FB2 (Pin 6): Buck Regulator 2 Feedback Pin. Receives feedback by a resistor divider connected across the output. Connecting FB2 to V_{IN2} combines buck regulator 2 with buck regulator 1 for higher current. Up to 4 converters may be combined in this way.

FB3 (Pin 7): Buck Regulator 3 Feedback Pin. Receives feedback by a resistor divider connected across the output. Connecting FB3 to V_{IN3} combines buck regulator 3 with buck regulator 2 for higher current. Up to 4 converters may be combined in this way.

V_{IN3} (Pin 8): Buck Regulator 3 Input Supply. Bypass to GND with a 10µF or larger ceramic capacitor. May be driven by an independent supply or must be shorted to V_{IN2} when buck regulator 3 is combined with buck regulator 2 for higher current.

SW3 (Pin 9): Buck Regulator 3 Switch Node. External inductor connects to this pin.

SW4 (Pin 10): Buck Regulator 4 Switch Node. External inductor connects to this pin.

V_{IN4} (Pin 11): Buck Regulator 4 Input Supply. Bypass to GND with a 10µF or larger ceramic capacitor. May be driven by an independent supply or must be shorted to V_{IN3} when buck regulator 4 is combined with buck regulator 3 for higher current.

FB4 (Pin 12): Buck Regulator 4 Feedback Pin. Receives feedback by a resistor divider connected across the output. Connecting FB4 to V_{IN4} combines buck regulator 4 with buck regulator 3 for higher current. Up to 4 converters may be combined in this way.

EN4 (Pin 13): Buck Regulator 4 Enable Input. Active high.

EN3 (Pin 14): Buck Regulator 3 Enable Input. Active high.

$\overline{IRQ}$ (Pin 15): Interrupt Pin (Active Low). Open-drain output. When an undervoltage, die temperature, or unmasked error condition is detected, this pin is driven LOW.

$\overline{RST}$ (Pin 16): Reset Pin (Active Low). Open-drain output. When the regulated output voltage of any unmasked enabled switching regulator is more than 7.5% below its programmed level, this pin is driven LOW. Assertion delay is scaled by the C_T capacitor. When all buck regulators are disabled $\overline{RST}$ is driven LOW.

CT (Pin 17): Timing Capacitor Pin. A capacitor connected to GND sets a time constant which is scaled for use by the ON, $\overline{KILL}$, $\overline{PB}$, $\overline{RST}$ and $\overline{IRQ}$ pins.

SYNC (Pin 18): Oscillator Synchronization Pin. Driving SYNC with an external clock signal will synchronize all switchers to the applied frequency. The slope compensation is automatically adapted to the external clock frequency. The absence of an external clock signal will enable the frequency programmed by the RT pin. Do not float.

RT (Pin 19): Oscillator Frequency Pin. This pin provides two modes of setting the switching frequency. Connecting a resistor from RT to ground will set the switching frequency based on the resistor value. If RT is tied to V_{CC} the default

PIN FUNCTIONS

internal 2MHz oscillator will be used. Do not float.

ON (Pin 20): Open-Drain Output. When the $\overline{PB}$ pin is pressed and released, the signal is debounced and the ON signal is held HIGH for a minimum time period that is scaled by the C_T capacitor. ON is forced low if: a) $\overline{KILL}$ is not driven high (by µP) within 10 seconds of the initial valid $\overline{PB}$ power turn-on event, b) $\overline{KILL}$ is driven low during normal operation, c) $\overline{PB}$ is pressed and held low for 10 seconds during normal operation, d) a RESET_ALL I^2C command is written. This pin can connect directly to a DC/DC converter enable pin that provides an internal pull-up. Otherwise a pull-up resistor to an external supply is required. All associated times are scaled by the C_T capacitor.

$\overline{PB}$ (Pin 21): Pushbutton Input. Active low. $\overline{PB}$ is internally pulled to V_{CC} through a 420k (typical) resistor.

$\overline{KILL}$ (Pin 22): Kill Input Pin. Forcing $\overline{KILL}$ low releases the ON output which in turn is forced low. While $\overline{KILL}$ is low, the buck converters will be forced to power down and will remain powered down for 1 second (scaled by the C_T capacitor) after $\overline{KILL}$ returns high. During system turn-on, this pin is blanked by a 10 second (scaled by the C_T capacitor) ($t_{\overline{KILL}H}$) to allow the system to pull $\overline{KILL}$ high. If unused, connect to V_{CC}.

EN6 (Pin 23): Buck Regulator 6 Enable Input. Active high.

EN5 (Pin 24): Buck Regulator 5 Enable Input. Active high.

FB5 (Pin 25): Buck Regulator 5 Feedback Pin. Receives feedback by a resistor divider connected across the output. Connecting FB5 to V_{IN5} combines buck regulator 5 with buck regulator 4 for higher current. Up to 4 converters may be combined in this way.

V_{IN5} (Pin 26): Buck Regulator 5 Input Supply. Bypass to GND with a 10µF or larger ceramic capacitor. May be driven by an independent supply or must be shorted to V_{IN4} when buck regulator 5 is combined with buck regulator 4 for higher current.

SW5 (Pin 27): Buck Regulator 5 Switch Node. External inductor connects to this pin.

SW6 (Pin 28): Buck Regulator 6 Switch Node. External inductor connects to this pin.

V_{IN6} (Pin 29): Buck Regulator 6 Input Supply. Bypass to GND with a 10µF or larger ceramic capacitor. May be driven by an independent supply or must be shorted to V_{IN5} when buck regulator 6 is combined with buck regulator 5 for higher current.

FB6 (Pin 30): Buck Regulator 6 Feedback Pin. Receives feedback by a resistor divider connected across the output. Connecting FB6 to V_{IN6} combines buck regulator 6 with buck regulator 5 for higher current. Up to 4 converters may be combined in this way.

FB7 (Pin 31): Buck Regulator 7 Feedback Pin. Receives feedback by a resistor divider connected across the output. Connecting FB7 to V_{IN7} combines buck regulator 7 with buck regulator 6 for higher current. Up to 4 converters may be combined in this way.

V_{IN7} (Pin 32): Buck Regulator 7 Input Supply. Bypass to GND with a 10µF or larger ceramic capacitor. May be driven by an independent supply or must be shorted to V_{IN6} when buck regulator 7 is combined with buck regulator 6 for higher current.

SW7 (Pin 33): Buck Regulator 7 Switch Node. External inductor connects to this pin.

SW8 (Pin 34): Buck Regulator 8 Switch Node. External inductor connects to this pin.

V_{IN8} (Pin 35): Buck Regulator 8 Input Supply. Bypass to GND with a 10µF or larger ceramic capacitor. May be driven by an independent supply or must be shorted to V_{IN7} when buck regulator 8 is combined with buck regulator 7 for higher current.

FB8 (Pin 36): Buck Regulator 8 Feedback Pin. Receives feedback by a resistor divider connected across the output. Connecting FB8 to V_{IN8} combines buck regulator 8 with buck regulator 7 for higher current. Up to 4 converters may be combined in this way.

PIN FUNCTIONS

EN8 (Pin 37): Buck Regulator 8 Enable Input. Active high.

EN7 (Pin 38): Buck Regulator 7 Enable Input. Active high.

WDO (Pin 39): Watchdog Timer Output. Open-drain output. WDO is pulled low for 200ms during a watchdog timer failure.

WDI (Pin 40): Watchdog Timer Input. The WDI pin must be toggled either low to high or high to low every 1.5 seconds. Failure to toggle WDI results in the WDO pin being pulled low for 200ms.

V_{CC} (Pin 41): Always-On LDO Output Voltage/Internal Bias Supply. When used as a regulator, V_{CC} should be connected to the emitter/source of the external LDO NPN/NFET transistor. V_{CC} serves as a low voltage rail that may be used to provide power to external circuitry, and is also used to power the internal top level circuitry of the LTC3375. Alternatively the V_{CC} pin may be connected to a 2.7V to 5.5V external power supply. In this case FBV_{CC} and V_{SHNT} should be tied to ground.

FBV_{CC} (Pin 42): Always-On LDO Feedback Pin. Receives feedback by a resistor divider connected across V_{CC}.

V_{SHNT} (Pin 43): Shunt Regulator Base Control Voltage. V_{SHNT} should be connected to the base/gate of an external high voltage NPN/NFET transistor and to its collector/drain through a resistor.

TEMP (Pin 44): Temperature Indication Pin. TEMP outputs a voltage of 150mV (typical) at room temperature. The TEMP voltage will change by 6.75mV/°C (typical) giving an external indication of the LTC3375 internal die temperature.

SCL (Pin 45): Serial Clock Line for I^2C Port.

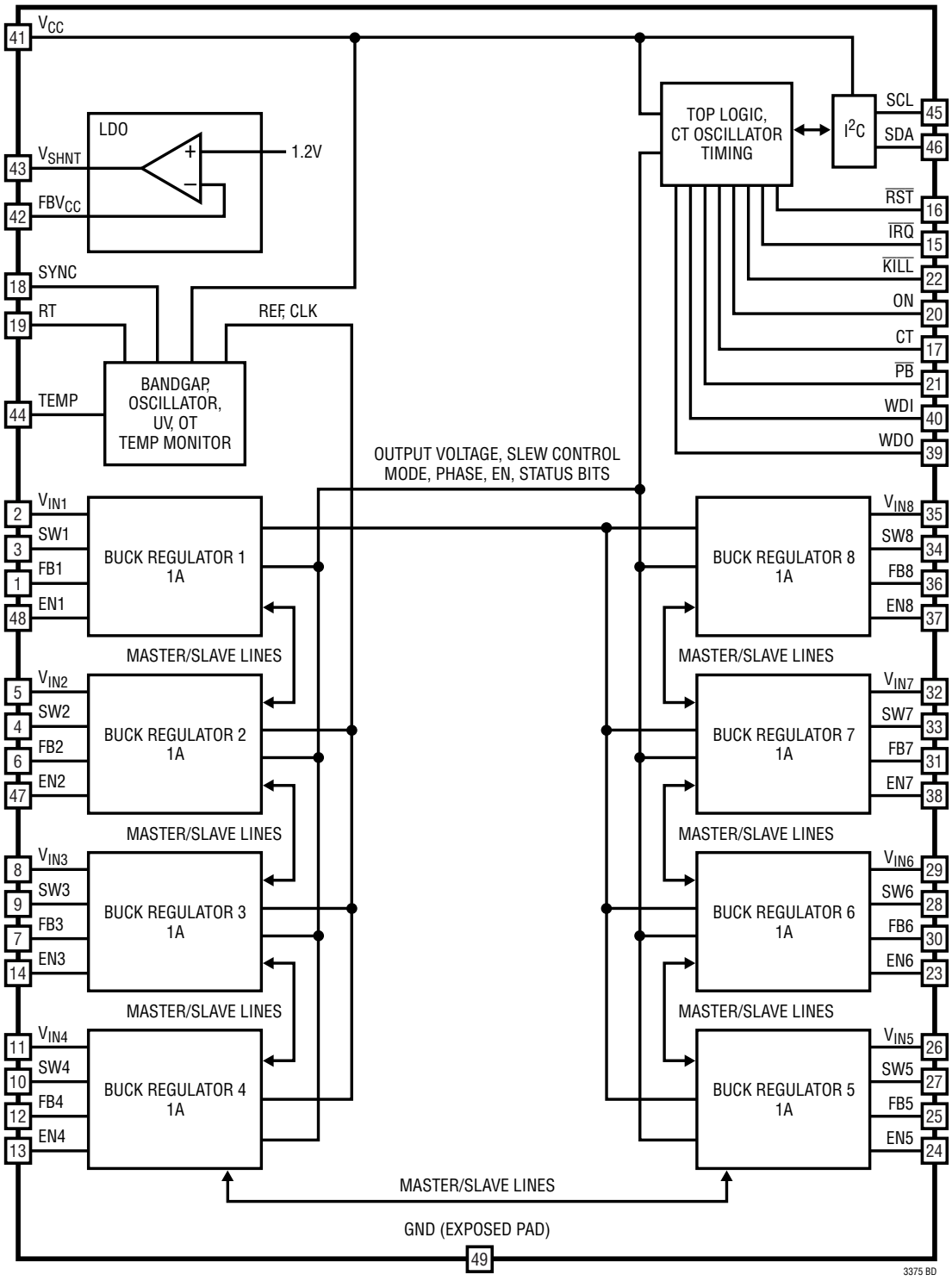
SDA (Pin 46): Serial Data Line for I^2C Port. Open-drain output during read back.

EN2 (Pin 47): Buck Regulator 2 Enable Input. Active high.

EN1 (Pin 48): Buck Regulator 1 Enable Input. Active high.

GND (Exposed Pad Pin 49): Ground. The exposed pad must be connected to a continuous ground plane on the printed circuit board directly under the LTC3375 for electrical contact and rated thermal performance.

BLOCK DIAGRAM



OPERATION

Buck Switching Regulators

The LTC3375 contains eight monolithic 1A synchronous buck switching regulators. All of the switching regulators are internally compensated and need only external feedback resistors to set the output voltage. The switching regulators offer two operating modes: Burst Mode operation (power-up default mode) for higher efficiency at light loads and forced continuous PWM mode for lower noise at light loads. In Burst Mode operation at light loads, the output capacitor is charged to a voltage slightly higher than its regulation point. The regulator then goes into sleep mode, during which time the output capacitor provides the load current. In sleep most of the regulator's circuitry is powered down, helping conserve input power. When the output capacitor droops below its programmed value, the circuitry is powered on and another burst cycle begins. The sleep time decreases as load current increases. In Burst Mode operation, the regulator will burst at light loads whereas at higher loads it will operate at constant frequency PWM mode operation. In forced continuous mode (selectable via I^2C command), the oscillator runs continuously and the buck switch currents are allowed to reverse under very light load conditions to maintain regulation. This mode allows the buck to run at a fixed frequency with minimal output ripple.

Each buck switching regulator has its own V_{IN}, SW, FB and EN pin to maximize flexibility. The enable pins have two different enable threshold voltages that depend on the operating state of the LTC3375. With all regulators disabled, the enable pin threshold is set to 730mV (typical). Once any regulator is enabled, the enable pin thresholds of the remaining regulators are set to a bandgap-based 400mV and the EN pins are each monitored by a precision comparator. This precision EN threshold may be used to provide event-based sequencing via feedback from other previously enabled regulators. All buck regulators have forward and reverse-current limiting, soft-start to limit inrush current during start-up, and short-circuit protection.

Each buck can operate in standalone mode using the EN pin in its default MODE and FB reference settings, or be fully controlled using the I^2C port. I^2C commands may be used to independently program each buck regulators' operating mode, oscillator phase, and reference voltage in addition to simple ON/OFF control. Each buck may have its phase programmed in 90° phase steps via I^2C. The phase step command programs the fixed edge of the switching sequence, which is when the PMOS turns on. The PMOS off (NMOS on) phase is subject to the duty cycle demanded by the regulator. Bucks 1 and 2 default to 0°, bucks 3 and 4 default to 90°, bucks 5 and 6 default to 180°, and bucks 7 and 8 default to 270°. Each buck can have its feedback voltage independently programmed in 25mV increments from 425mV to 800mV. All regulators' feedback voltages default to 725mV at initial power-up. In cases where power stages are combined, the register content of the master program the combined buck regulator's behavior and the register contents of the slave are ignored.

Two additional I^2C commands act on all the buck switching regulators together. In shutdown, an I^2C control bit keeps all the SW nodes in a high impedance state (default) or forces all the SW nodes to decay to GND through 1k (typical) resistors. Also, the slew rate of the SW nodes may be switched from the default value to a lower value for reduced radiated EMI at the cost of a small drop in efficiency.

Each buck regulator may be enabled via its enable pin or I^2C. The buck regulator enable pins may be tied to V_{OUT} voltages, through a resistor divider, to program power-up sequencing. If a different power-down sequence is required, the enables can be redundantly written via I^2C. The EN pins can then be ignored via an I^2C command, and the switching regulators may be powered down via I^2C while the EN pins remain tied to the output voltages of other regulators.

In addition to many programming options, there are also 17 bits of data that may be read back to report fault conditions on the LTC3375, and all I^2C commands can be read back prior to executing.

Buck Regulators with Combined Power Stages

Up to four adjacent buck regulators may be combined in a master-slave configuration by connecting their SW pins together, connecting their V_{IN} pins together, and connecting the higher numbered bucks' FB pin(s) to the input supply. The lowest numbered buck is always the master. In Figure 1, buck regulator 1 is the master. The

OPERATION

feedback network connected to the FB1 pin programs the output voltage to 1.2V. The FB2 pin is tied to $V_{IN1/2}$, which configures buck regulator 2 as the slave. The SW1 and SW2 pins must be tied together, as must the V_{IN1} and V_{IN2} pins. The register contents of the master program, the combined buck regulator's behavior, and the register contents of the slave are ignored. The slave buck control circuitry draws no current. The enable of the master buck (EN1) controls the operation of the combined bucks; the enable of the slave regulator (EN2) must be tied to ground.

Any combination of 2, 3, or 4 adjacent buck regulators may be combined to provide either 2A, 3A, or 4A of average output load current. For example, buck regulator 1 and buck regulator 2 may run independently, while buck regulators 3 and 4 may be combined to provide 2A, while buck regulators 5 through 8 may be combined to provide 4A. Buck regulator 1 is never a slave, and buck regulator 8 is never a master. 15 unique output power stage configurations are possible to maximize application flexibility.

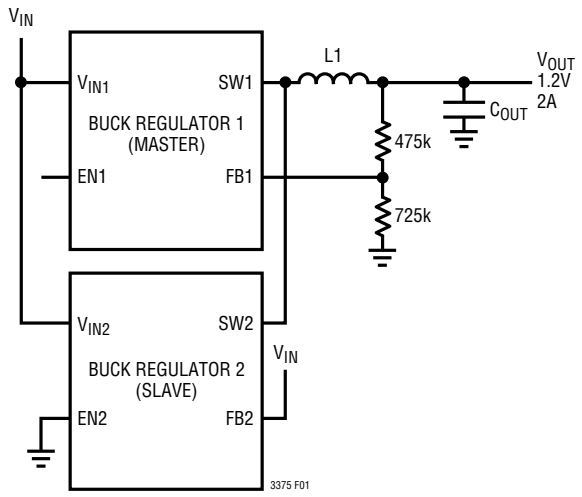


Figure 1. Buck Regulators Configured as Master-Slave

Pushbutton Interface

The LTC3375 includes a pushbutton interface which can be used to provide power-up or power-down control for either the part or the application. The $\overline{PB}$, $\overline{KILL}$, and ON pins provide the user with flexibility to power-up or power-down the part in addition to having I^2C control. All $\overline{PB}$ timing parameters are scaled using the CT pin. Times described below apply to a nominal C_T capacitor of 0.01µF.

The LTC3375 is in an off state when it is powered up with all regulators in shutdown. The ON pin is LOW in the off state. The ON pin will go HIGH if $\overline{PB}$ is pulled LOW for 200ms. The ON pin stays in its HIGH state for 10 seconds and then returns LOW unless $\overline{KILL}$ is asserted HIGH in this time in which case ON will remain HIGH. If $\overline{KILL}$ goes LOW, for longer than a 50ms debounce time, while ON is HIGH after the 10 second time has expired, ON will again go to its LOW state. $\overline{PB}$ being held low causes the $\overline{KILL}$ pin to be ignored.

Once in the "on" state (ON pin is HIGH), the LTC3375 can be powered down in one of three ways that allow for flexibility between hardware and software system resets. First, if $\overline{PB}$ is held LOW for at least 10 seconds, then ON will be driven LOW. This will not force a hard reset on any of the buck switching regulators. The ON pin, however, may be used to either drive the EN pin of the first sequenced buck converter or that of an upstream high voltage buck switching regulator. In this case the $\overline{IRQ}$ pin is latched to its LOW state to indicate a $\overline{PB}$ induced reset. Second, if the $\overline{PB}$ pin is driven LOW for longer than 50ms but less than 10 seconds, the $\overline{IRQ}$ pin will be pulled LOW for as long as the $\overline{PB}$ pin remains LOW. If a microcontroller sees a transient $\overline{IRQ}$ LOW signal, then this should signal that the user has pressed the $\overline{PB}$. A software power-down may then be initiated if so desired. Finally, if the $\overline{KILL}$ input is driven LOW for longer than 50ms, then a hard reset will be initiated. All enabled buck switching regulators will be turned off while $\overline{KILL}$ is low and will remain powered down for 1 second after $\overline{KILL}$ returns high. $\overline{KILL}$ being low also forces a hard reset while the pushbutton is in the "off" state. A hard reset may also be generated by using the RESET_ALL I^2C command that will last for 1 second. The pushbutton will return to the "off" state. $\overline{KILL}$ must be high to power-up using EN pins or I^2C. In any hard reset event all buck regulator I^2C bits are set low.

Power-Up and Power-Down Via Pushbutton

The LTC3375 may be turned on and off using the $\overline{PB}$, $\overline{KILL}$, and ON pins as shown in Figures 2a and 2b. In Figures 2a and 2b, pressing $\overline{PB}$ LOW at time t_1, causes the ON pin to go HIGH at time t_2 and stay HIGH for at least 10 seconds after which ON will go LOW unless $\overline{KILL}$ has been asserted high. ON can be connected to the EN pin

OPERATION

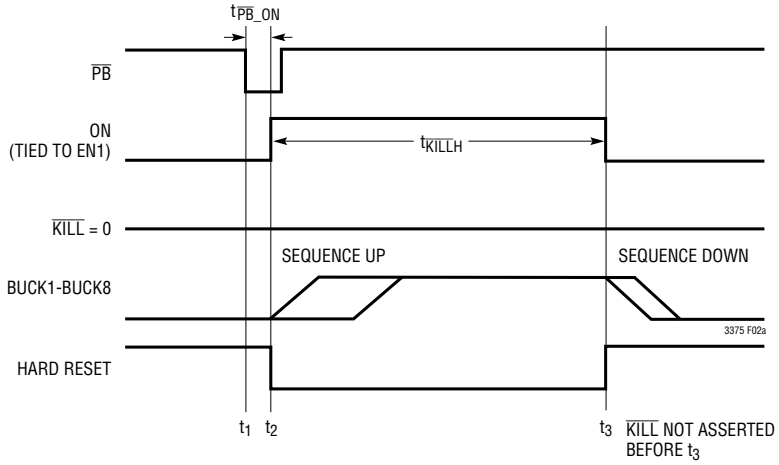


Figure 2a. Power-Up Using $\overline{PB}$ (Sequenced Power-Up, Figure 8)

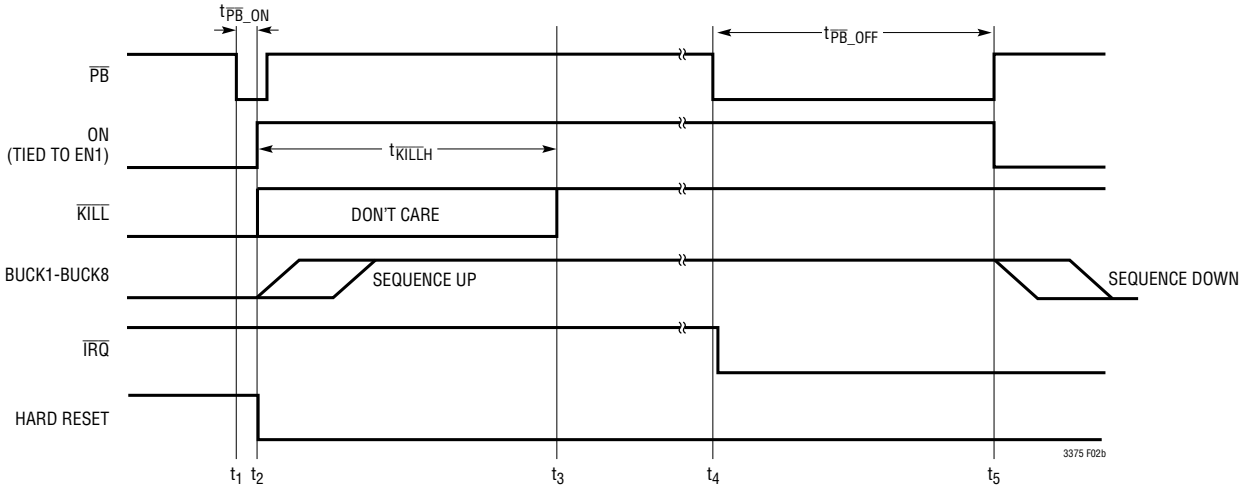


Figure 2b. Power-Up and Power-Down Using $\overline{PB}$ (Sequenced Power-Up, Figure 8)

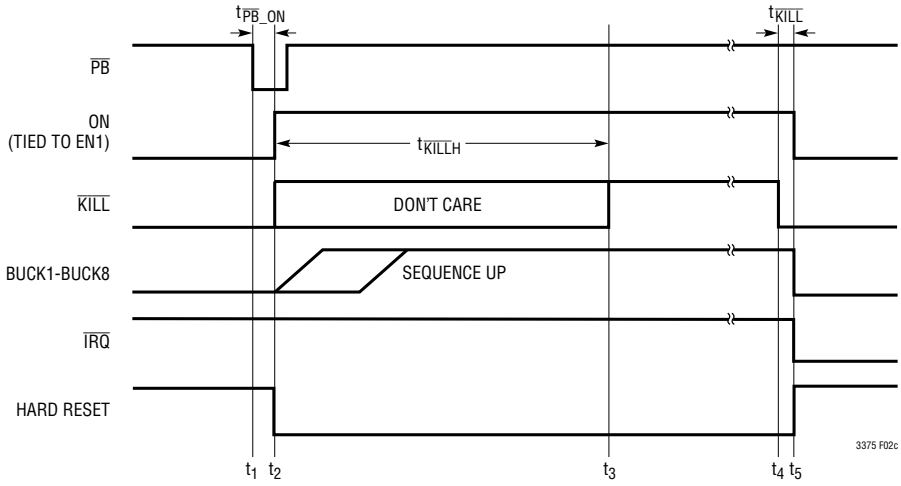


Figure 2c. Power-Up Using $\overline{PB}$ and Power-Down Using $\overline{KILL}$

OPERATION

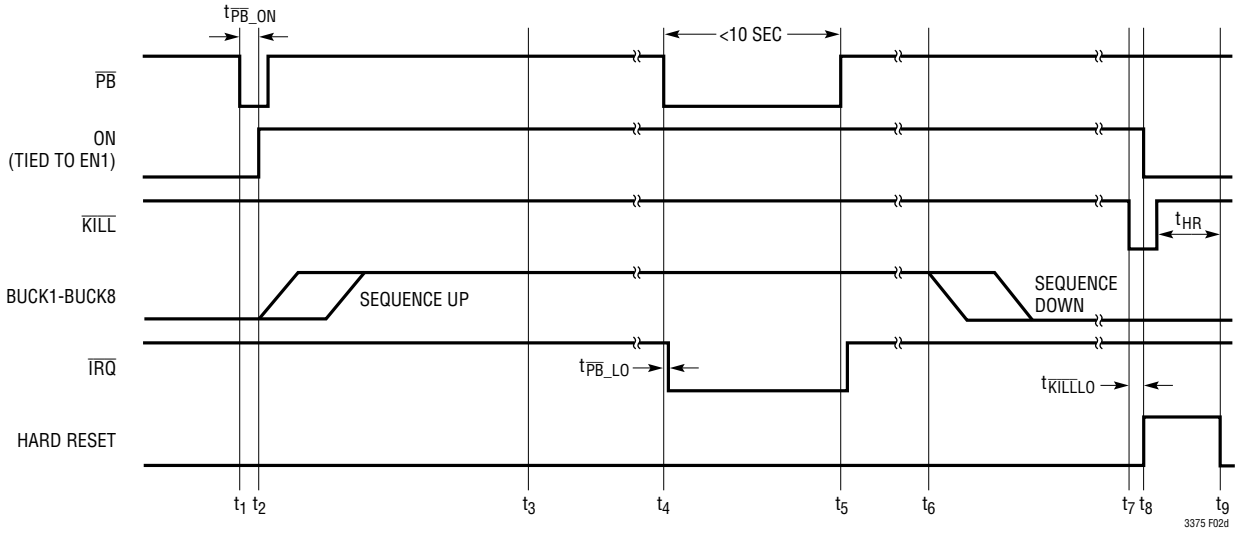


Figure 2d. Power-Up Using $\overline{PB}$ and Power-Down Using a "Soft" Reset

of either an upstream high voltage buck regulator, or any EN pin causing its associated buck switching regulator to power-up, which can sequentially power-up the other buck regulators. The $\overline{RST}$ pin gets pulled HIGH 230ms after the last enabled buck is in its PGOOD state. An application showing sequential regulator start-up is shown in the Typical Applications section (Figure 8).

In Figure 2b, $\overline{PB}$ is held LOW at instant t_4 for 10 seconds. This causes ON to return to a LOW state, which can sequence a power-down by either shutting down an upstream high voltage buck, or by shutting down one of the internal buck switching regulators.

In Figure 2c, $\overline{KILL}$ is pulled LOW while the pushbutton is in the "on" state. This causes a hard reset to be generated at t_4, all regulators are powered down 50ms later at time t_5. An I^2C signaled reset will have the same effect as pulling $\overline{KILL}$ low momentarily.

In Figure 2d, $\overline{PB}$ is held LOW at instant t_4 for a time greater than 50ms but less than 10 seconds. This causes a transient $\overline{IRQ}$ signal. This unlatched interrupt can be used to signal a user pushbutton request. In this case a software reset may be initiated if so desired. In Figure 2d, the microprocessor initiates the power-down sequencing after the user pushbutton signal at time t_6. At time t_7, once all the converters are powered down, the micro brings $\overline{KILL}$ LOW. 50ms later at time t_8 ON goes LOW. In this case, a hard reset is issued until 1 second after $\overline{KILL}$ returns high at t_9.

None of the pushbutton based $\overline{IRQ}$ signals are reported in an I^2C register. As such, any $\overline{IRQ}$ signals that are not revealed by polling the I^2C read back may be interpreted as caused by the pushbutton.

Power-Up and Power-Down Via Enable Pin or I^2C

All regulators can be enabled either via its enable pin or I^2C. If the use of the pushbutton interface is not desired $\overline{PB}$ and $\overline{KILL}$ should be tied to V_{CC}, and the user may simply enable any of the buck switching regulators by asserting a HIGH signal on any of the EN pins or by writing a buck switching regulator EN command to the I^2C. If no I^2C enable has been written, the buck switching regulator may be powered down by simply returning its EN pin to a LOW state. If it is wished to power-down the converters via I^2C, an IGNORE_EN command may be written causing the LTC3375 to treat the state of the EN pin as LOW regardless of its input. Then, the buck switching converters can be powered down via I^2C regardless of their associated EN pin. Alternatively a RESET_ALL command may be written that will force all the buck switching regulators to power-down and remain powered down for a minimum of one second before they are allowed to be re-enabled.

OPERATION

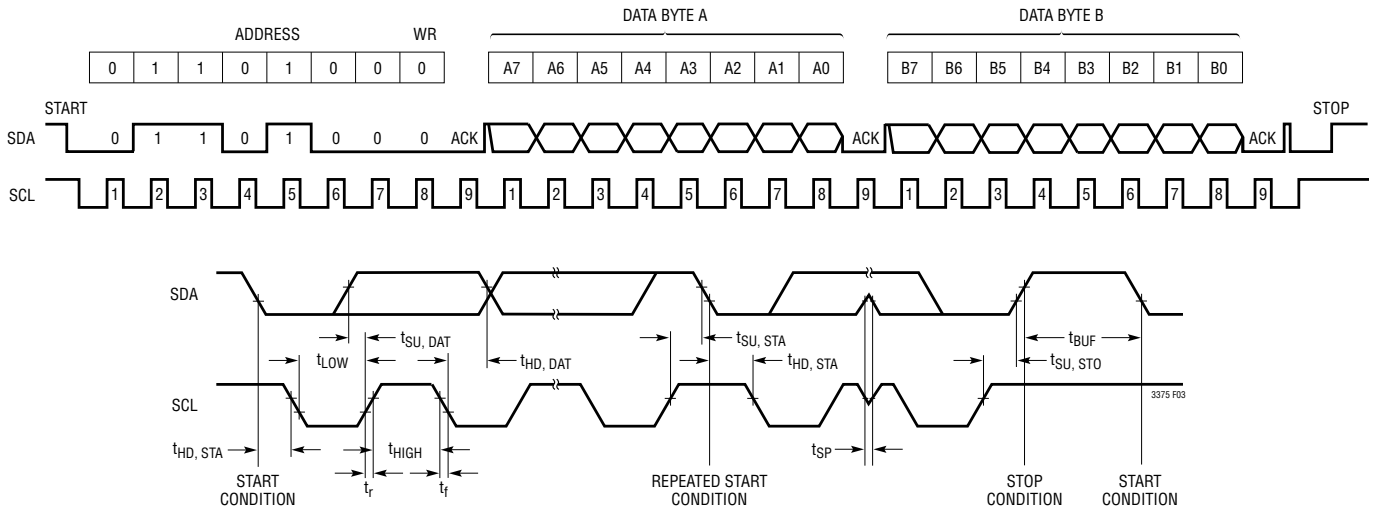


Figure 3. I²C Bus Operation

I²C Interface

The LTC3375 may communicate with a bus master using the standard I²C 2-wire interface. The timing diagram (Figure 3) shows the relationship of the signals on the bus. The two bus lines, SDA and SCL, must be high when the bus is not in use. External pull-up resistors or current sources, such as the LTC1694 SMBus accelerator, are required on these lines. The LTC3375 is both a slave receiver and slave transmitter. The I²C control signals, SDA and SCL are scaled internally to the V_{CC} supply.

The I²C port has an undervoltage lockout on the V_{CC} pin. When V_{CC} is below 1.8V, the I²C serial port is cleared and the LTC3375 registers are set to their default configurations.

I²C Bus Speed

The I²C port is designed to be operated at speeds of up to 400kHz. It has built-in timing delays to ensure correct operation when addressed from the I²C compatible master device.

I²C Start and Stop Conditions

A bus master signals the beginning of communications by transmitting a START condition. A START condition is generated by transitioning SDA from HIGH to LOW while SCL is HIGH. The master may transmit either the slave write or the slave read address. Once data is written to the LTC3375, the master may transmit a STOP condition which commands the LTC3375 to act upon its new command set. A STOP condition is sent by the master by transitioning SDA from LOW to HIGH while SCL is HIGH. The bus is then free for communication with another I²C device.

I²C Byte Format

Each byte sent to or received from the LTC3375 must be 8 bits long followed by an extra clock cycle for the acknowledge bit. The data should be sent to the LTC3375 most significant bit (MSB) first.

I²C Acknowledge

The acknowledge signal is used for handshaking between the master and the slave. When the LTC3375 is written to (write address), it acknowledges its write address as well as the subsequent two data bytes. When it is read from (read address), the LTC3375 acknowledges its read address only. The bus master should acknowledge receipt of information from the LTC3375.

An acknowledge (active LOW) generated by the LTC3375 lets the master know that the latest byte of information was received. The acknowledge related clock pulse is generated by the master. The master releases the SDA line (HIGH) during the acknowledge clock cycle. The LTC3375 pulls down the SDA line during the write acknowledge clock pulse so that it is a stable LOW during the HIGH period of this clock pulse.

OPERATION

Table 1. Summary of I²C Sub-Addresses and Byte Formats. Bits A7, A6, A5, A4 of Sub-Address Need to be 0 to Access Registers

SUB-ADDRESS A7A6A5A4A3A2A1A0	OPERATION	ACTION	BYTE FORMAT D7D6D5D4D3D2D1D0	DEFAULT D7D6D5D4D3D2D1D0	COMMENTS
0000 0000 (00h)	Read/Write	Global Logic	RESET_ALL, DT[1], DT[0], IGNORE_EN, 1KPD, SLOW, RD_TEMP, Unused	0000 0000	Bits either act at top level or on all buck switching regulators at once
0000 0001 (01h)	Read/Write	Buck1 Register	ENABLE, MODE, PHASE[1], PHASE[0], DAC[3], DAC[2]. DAC[1], DAC[0]	0000 1100	
0000 0010 (02h)	Read/Write	Buck2 Register	ENABLE, MODE, PHASE[1], PHASE[0], DAC[3], DAC[2]. DAC[1], DAC[0]	0000 1100	
0000 0011 (03h)	Read/Write	Buck3 Register	ENABLE, MODE, PHASE[1], PHASE[0], DAC[3], DAC[2]. DAC[1], DAC[0]	0001 1100	
0000 0100 (04h)	Read/Write	Buck4 Register	ENABLE, MODE, PHASE[1], PHASE[0], DAC[3], DAC[2]. DAC[1], DAC[0]	0001 1100	
0000 0101 (05h)	Read/Write	Buck5 Register	ENABLE, MODE, PHASE[1], PHASE[0], DAC[3], DAC[2]. DAC[1], DAC[0]	0010 1100	
0000 0110 (06h)	Read/Write	Buck6 Register	ENABLE, MODE, PHASE[1], PHASE[0], DAC[3], DAC[2]. DAC[1], DAC[0]	0010 1100	
0000 0111 (07h)	Read/Write	Buck7 Register	ENABLE, MODE, PHASE[1], PHASE[0], DAC[3], DAC[2]. DAC[1], DAC[0]	0011 1100	
0000 1000 (08h)	Read/Write	Buck8 Register	ENABLE, MODE, PHASE[1], PHASE[0], DAC[3], DAC[2]. DAC[1], DAC[0]	0011 1100	
0000 1001 (09h)	Read/Write	$\overline{\text{RST}}$ Mask	PGOOD[8], PGOOD[7], PGOOD[6], PGOOD[5], PGOOD[4], PGOOD[3], PGOOD[2], PGOOD[1]	1111 1111	Fault will pull $\overline{\text{RST}}$ low if the corresponding bit is '1'
0000 1010 (0Ah)	Read/Write	$\overline{\text{IRQ}}$ PGOOD Mask	PGOOD[8], PGOOD[7], PGOOD[6], PGOOD[5], PGOOD[4], PGOOD[3], PGOOD[2], PGOOD[1]	0000 0000	Fault will pull $\overline{\text{IRQ}}$ low if the corresponding bit is '1'
0000 1011 (0Bh)	Read/Write	$\overline{\text{IRQ}}$ UVLO Mask	UVLO[8], UVLO[7], UVLO[6], UVLO[5], UVLO[4], UVLO[3], UVLO[2], UVLO[1]	0000 0000	Fault will pull $\overline{\text{IRQ}}$ low if the corresponding bit is '1'
0000 1100 (0Ch)	Read	PGOOD Status Register (Latched at $\overline{\text{IRQ}}$ fault)	PGOOD[8], PGOOD[7], PGOOD[6], PGOOD[5], PGOOD[4], PGOOD[3], PGOOD[2], PGOOD[1]		Read back of PGOOD based faults. If the corresponding mask bit is '0', then bit can be used to read back real time data
0000 1101 (0Dh)	Read	UVLO Status Register (Latched at $\overline{\text{IRQ}}$ fault)	UVLO[8], UVLO[7], UVLO[6], UVLO[5], UVLO[4], UVLO[3], UVLO[2], UVLO[1]		Read back of UVLO based faults. If the corresponding mask bit is '0', then bit can be used to read back real time data
0000 1110 (0Eh)	Read	Temp Monitor	DT_WARN, TEMP[6], TEMP[5], TEMP[4], TEMP[3], TEMP[2], TEMP[1], TEMP[0]		TEMP bits read back the TEMP digital code. DT_WARN bit latches high if an $\overline{\text{IRQ}}$ fault has been caused due to a DT Warning
0000 1111 (0Fh)	Write	Clear Interrupt		NA	Clears the Interrupt Bit, Status Latches are Unlatched

When the LTC3375 is read from, it releases the SDA line so that the master may acknowledge receipt of the data. Since the LTC3375 only transmits one byte of data during a read cycle, a master not acknowledging the data sent by the LTC3375 has no I²C specific consequence on the operation of the I²C port.

I²C Slave Address

The LTC3375 responds to a 7-bit address which has been factory programmed to b'0110100[R/WB]'. The LSB of the address byte, known as the read/write bit, should be 0 when writing to the LTC3375 and 1 when reading data from it. Considering the address as an 8-bit word,

OPERATION

the write address is 68h and the read address is 69h. The LTC3375 will acknowledge both its read and write address.

I²C Sub-Addressed Writing

The LTC3375 has 13 command registers for control input. They are accessed by the I²C port via a sub-addressed writing system.

A single write cycle of the LTC3375 consists of exactly three bytes except when a clear interrupt command is written. The first byte is always the LTC3375's write address. The second byte represents the LTC3375's sub-address. The sub-address is a pointer which directs the subsequent data byte within the LTC3375. The third byte consists of the data to be written to the location pointed to by the sub-address. The LTC3375 contains 12 control registers which can be written to.

I²C Bus Write Operation

The master initiates communication with the LTC3375 with a START condition and the LTC3375's write address. If the address matches that of the LTC3375, the LTC3375 returns an acknowledge. The master should then deliver the sub-address. Again the LTC3375 acknowledges and the cycle is repeated for the data byte. The data byte is transferred to an internal holding latch upon the return of its acknowledge by the LTC3375. This procedure must be repeated for each sub-address that requires new data. After one or more cycles of [ADDRESS][SUB-ADDRESS][DATA], the master may terminate the communication with a STOP condition. Multiple sub-addresses may be written to with a single address command using a [ADDRESS][SUB-ADDRESS][DATA][SUB-ADDRESS][DATA] sequence. Alternatively, a REPEAT-START condition can be initiated by the master and another chip on the I²C bus can be addressed. This cycle can continue indefinitely and the LTC3375 will remember the last input valid data that it received. Once all chips on the bus have been addressed and sent valid data, a global STOP can be sent and the LTC3375 will update its command latches with the data that it had received.

It is important to understand that until a STOP signal is transmitted, data written to the LTC3375 command registers is not acted on by the LTC3375. Only once a STOP signal is issued is the data transferred to the command latch and acted on.

I²C Bus Read Operation

The LTC3375 has 13 command registers and three status registers. The contents of any of these registers, except for the Clear Interrupt (0Fh) register, may be read back via I²C.

To read the data of a register, that register's sub-address must be provided to the LTC3375. The bus master reads the status of the LTC3375 with a START condition followed by the LTC3375 write address followed by the first data byte (the sub-address of the register whose data needs to be read) which is acknowledged by the LTC3375. After receiving the acknowledge signal from the LTC3375 the bus master initiates a new START condition followed by the LTC3375 read address. The LTC3375 acknowledges the read address and then returns a byte of read back data from the selected register. A STOP command is not required for the bus read operation.

Immediately after writing data to a register, the contents of that register may be read back if the bus master issues a START condition followed by the LTC3375 read address.

Error Condition Reporting Via $\overline{\text{RST}}$ and $\overline{\text{IRQ}}$ Pins

Error conditions are reported back via the $\overline{\text{IRQ}}$ and $\overline{\text{RST}}$ pins. After an error condition is detected, status data can be read back to a microprocessor via I²C to determine the exact nature of the error condition.

Figure 4 is a simplified schematic showing the signal path for reporting errors via the $\overline{\text{RST}}$ and $\overline{\text{IRQ}}$ pins.

All buck switching regulators have an internal power good (PGOOD) signal. When the regulated output voltage of an enabled switcher rises above 93.5% of its programmed value, the PGOOD signal will transition high. When the regulated output voltage falls below 92.5% of its programmed value, the PGOOD signal is pulled low. If any internal PGOOD signal is not masked and stays low for greater than 50µs, then the $\overline{\text{RST}}$ and $\overline{\text{IRQ}}$ pins are pulled low, indicating to a microprocessor that an error condition has occurred. The 50µs filter time prevents the pins from being pulled low due to a transient.

OPERATION

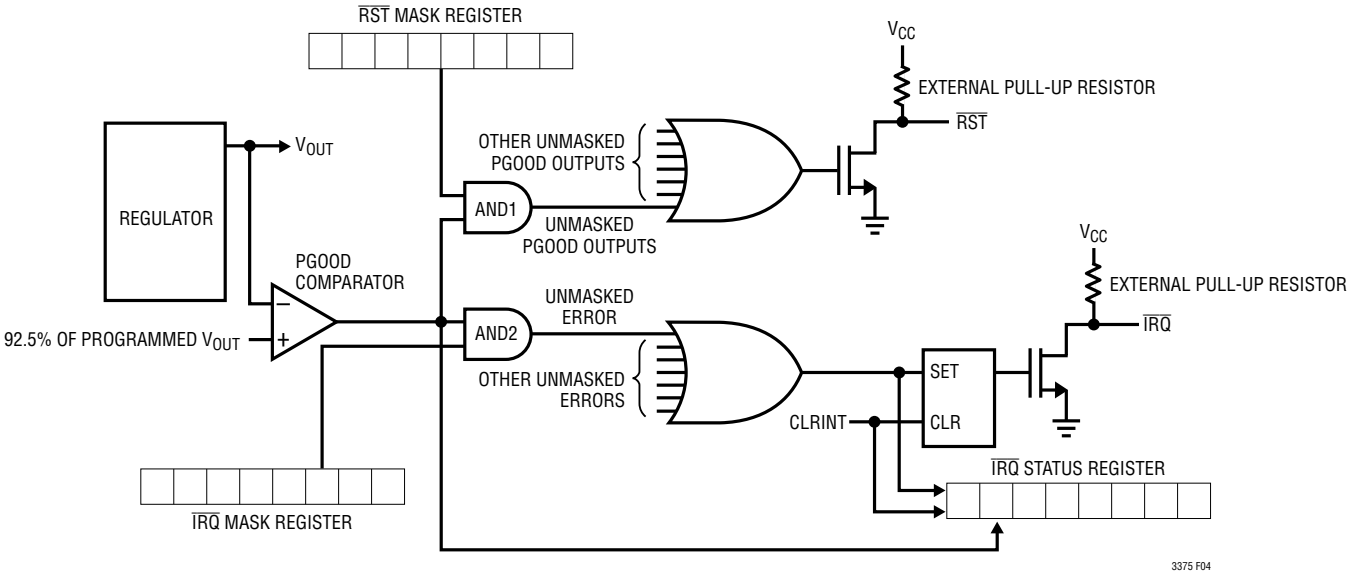


Figure 4. Simplified Schematic $\overline{RST}$ and $\overline{IRQ}$ Signal Path

An error condition that pulls the $\overline{RST}$ pin low is not latched. When the error condition goes away, the $\overline{RST}$ pin is released and is pulled high if no other error condition exists.

In addition to the PGOOD signals of the regulators the $\overline{IRQ}$ pin also indicates the status of the pushbutton, die temperature, and undervoltage flags. Pushbutton faults cannot be masked. A fault that causes the $\overline{IRQ}$ pin to be pulled low is latched with the exception of a pushbutton press that is less than 10 seconds (C_T = 0.01µF) while ON is HIGH. In the case of a transient pushbutton press $\overline{IRQ}$ will be held LOW for the duration of the button press latching after the 10 second power-down time has elapsed. In all other cases when the fault condition is cleared, the $\overline{IRQ}$ pin is still maintained in its low state. The user needs to clear the interrupt by using a CLRINT command.

On start-up, all PGOOD status outputs are unmasked with respect to $\overline{RST}$. While all PGOOD and UVLO status outputs are masked with respect to $\overline{IRQ}$. A power-on reset will cause $\overline{RST}$ to be pulled low. Once all enabled regulators have their output PGOOD for 230ms typical (C_T = 0.01µF) the $\overline{RST}$ output goes Hi-Z.

By masking a PGOOD signal, the $\overline{RST}$ or $\overline{IRQ}$ pin will remain Hi-Z even though the output voltage of a regulator may be below its PGOOD threshold. By masking a UVLO signal, the $\overline{IRQ}$ pin will remain Hi-Z even though its associated input voltage may be below its UVLO threshold. However, when the status registers are read back, the true conditions of PGOOD and UVLO are reported. If a UVLO $\overline{IRQ}$ is masked but the associated PGOOD signal is unmasked, then the $\overline{IRQ}$ pin may still be pulled low due to a PGOOD LOW signal that resulted from an input UVLO.

Temperature Monitoring and Overtemperature Protection

To prevent thermal damage to the LTC3375 and its surrounding components, the LTC3375 incorporates an overtemperature (OT) function. When the LTC3375 die temperature reaches 165°C (typical) all enabled buck switching regulators are shut down and remain in shutdown until the die temperature falls to 155°C (typical). The LTC3375 also has a die temperature warning function which warns a user that the die temperature has reached its programmed alarm threshold which allows the user to take any corrective action. The die temperature warning threshold is user programmable as shown in Table 2.

OPERATION

Table 2. Die Temperature Warning Thresholds

DT[1], DT[0]	DIE TEMPERATURE WARNING THRESHOLD
00 (Default)	Inactive
01	140°C
10	125°C
11	110°C

A die temperature warning is reported to the user by pulling the $\overline{IRQ}$ pin low. This warning can be read back on the LSB of the Temp_Monitor register. The die temperature warning flag is disabled when the DT bits are set to 00 (default).

The temperature may be read back by the user either digitally through the I²C Temp_Monitor Register or by sampling the TEMP pin analog voltage. The temperature, T, indicated by the TEMP pin voltage is given by:

$$T = \frac{V_{TEMP} + 19mV}{6.75mV} \bullet 1°C \quad (1)$$

The analog voltage can be digitally polled using an internal A/D converter. In order to digitally read the temperature voltage the user should first issue a RD_TEMP I²C command to tell the A/D converter to poll the TEMP voltage. At least 2ms after this command has been written the user may then poll the TEMP bits in the Temp_Monitor register. The TEMP bits are related to the TEMP voltage as follows:

$$V_{TEMP} = 1.3V \bullet (0.08333 + 0.007161 \bullet D) \quad (2)$$

where D corresponds to the bit weight of the digital code. Combining Equation 1 and Equation 2 yields:

$$T = 18.86°C + 1.379°C \bullet D \quad (3)$$

If die temperature warning and temperature read back functionality are not desired, then the user may shut down the temperature monitor in order to lower quiescent current (15µA typical) by tying TEMP to V_{CC}. In this case all enabled buck switching regulators are still shut down when the die temperature reaches 165°C (typical) and remain in shutdown until the die temperature falls to 155°C (typical). If none of the buck switching regulators are enabled, then the temperature monitor is also shut down to further reduce quiescent current.

RESET_ALL Functionality

The RESET_ALL bit shuts down all enabled regulators (enabled either via its enable pin or I²C) for one second. The RESET_ALL bit is self clearing, and all other I²C bits (besides the enable bits, which are set low) will remain in their previous states. The RESET_ALL bit will also reset the pushbutton to the powered-down state.

Programming the Operating Frequency

Selection of the operating frequency is a trade-off between efficiency and component size. High frequency operation allows the use of smaller inductor and capacitor values. Operation at lower frequencies improves efficiency by reducing internal gate charge losses but requires larger inductance values and/or capacitance to maintain low output voltage ripple.

The operating frequency for all of the LTC3375 regulators is determined by an external resistor that is connected between the RT pin and ground. The operating frequency can be calculated by using the following equation:

$$f_{OSC} = \frac{8 \bullet 10^{11} \bullet \Omega Hz}{R_T} \quad (4)$$

While the LTC3375 is designed to function with operating frequencies between 1MHz and 3MHz, it has safety clamps that will prevent the oscillator from running faster than 4MHz (typical) or slower than 250kHz (typical). Tying the RT pin to V_{CC} sets the oscillator to the default internal operating frequency of 2MHz (typical).

The LTC3375's internal oscillator can be synchronized, through an internal PLL circuit, to an external frequency by applying a square wave clock signal to the SYNC pin. During synchronization, the top MOSFET turn-on of any buck switching regulators operating at 0° phase are locked to the rising edge of the external frequency source. All other buck switching regulators are locked to the appropriate phase of the external frequency source (see Buck Switching Regulators). The synchronization frequency range is 1MHz to 3MHz.

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After detecting an external clock on the first rising edge of the SYNC pin, the PLL starts up at the current frequency being programmed by the RT pin. The internal PLL then requires a certain number of periods to gradually settle until the frequency at SW matches the frequency and phase of SYNC.

When the external clock is removed the LTC3375 needs approximately 5µs to detect the absence of the external clock. During this time, the PLL will continue to provide clock cycles before it recognizes the lack of a SYNC input. Once the external clock removal has been identified, the oscillator will gradually adjust its operating frequency to match the desired frequency programmed at the RT pin.

V_{CC} Shunt Regulator

The LTC3375 has the control circuitry to regulate the output of an N-type device. The circuit should be connected as shown in Figures 6a and 6b. The voltage at FBV_{CC} will servo to 1.20V and V_{CC} can be programmed between 2.7V and 5.5V. The N-type device can be used to regulate a lower voltage at V_{CC} while being powered from a high voltage supply. The N-type device must be chosen so that it can handle the power dissipated in regulating V_{CC}. The internal circuitry of the LTC3375 can only pull-down on the V_{SHNT} node. A pull-up resistor is required for positive gate drive.

If V_{CC} is incorrectly programmed or a current load at V_{CC} causes V_{SHNT} to go above 6.1V (typical), then V_{SHNT} will be internally clamped and V_{CC} may lose regulation.

If the use of the V_{CC} regulator is not desired, then V_{CC} should be tied to an external DC voltage source and a decoupling capacitor. FBV_{CC} and V_{SHNT} should be tied to ground.

Watchdog Timer

The watchdog circuit monitors a microprocessor's activity. The microprocessor is required to change the logic state of the WDI pin at least once every 1.5 seconds (typical) in order to clear the watchdog timer and prevent the WDO pin from signaling a timeout.

The watchdog timer begins running immediately after a power-on reset. The watchdog timer will continue to run until a transition is detected on the WDI input. During this time WDO will be in a Hi-Z state. Once the watchdog timer times out, WDO will be pulled low and the reset timer is started. WDO being pulled low may be used to force a reset on the controlling microprocessor. If no WDI transition is received when the reset timer times out, after 200ms (typical), WDO will again become Hi-Z and the 1.5 seconds watchdog reset time will begin again. If a transition is received on the WDI input during the watchdog timeout period, then WDO will become Hi-Z immediately after the WDI transition and the 1.5 seconds watchdog reset time will begin at that point.

APPLICATIONS INFORMATION

Buck Switching Regulator Output Voltage and Feedback Network

The output voltage of the buck switching regulators is programmed by a resistor divider connected from the switching regulator's output to its feedback pin and is given by $V_{OUT} = V_{FB}(1 + R2/R1)$ as shown in Figure 5. Typical values for R1 range from 40k to 1M. The buck regulator transient response may improve with optional capacitor C_{FF} that helps cancel the pole created by the feedback resistors and the input capacitance of the FB pin. Experimentation with capacitor values between 2pF and 22pF may improve transient response.

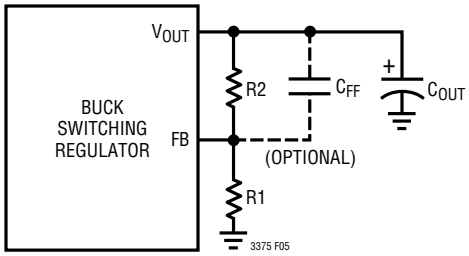


Figure 5. Feedback Components

Buck Regulators

All eight buck regulators are designed to be used with inductors ranging from 1µH to 3.3µH depending on the lowest switching frequency that the buck regulator must operate at. To operate at 1MHz a 3.3µH inductor should be used, while to operate at 3MHz a 1µH inductor may be used. Table 3 shows some recommended inductors for the buck regulators.

The input supply needs to be decoupled with a 10µF capacitor while the output needs to be decoupled with a 22µF capacitor. Refer to Capacitor Selection for details on selecting a proper capacitor.

Each buck regulator can be programmed via I^2C. To program buck regulator 1 use sub-address 01h, buck regulator 2 sub-address 02h, buck regulator 3 sub-address 03h, buck regulator 4 sub address 04h, buck regulator 5 sub-address 05h, buck regulator 6 sub-address 06h, buck regulator 7 sub-address 07h, and buck regulator 8 sub-address 08h. The bit format is explained in Table 7.

Combined Buck Regulators

A single 2A buck regulator is available by combining two adjacent 1A buck regulators together. Likewise a 3A or 4A buck regulator is available by combining any three or four adjacent buck regulators respectively. Tables 4, 5, and 6 show recommended inductors for these configurations.

The input supply needs to be decoupled with a 22µF capacitor while the output needs to be decoupled with a 47µF capacitor for a 2A combined buck regulator. Likewise for 3A and 4A configurations the input and output capacitance must be scaled up to account for the increased load. Refer to Capacitor Selection in the Applications Information section for details on selecting a proper capacitor.

In many cases, any extra unused buck converters may be used to increase the efficiency of the active regulators. In general the efficiency will improve for any regulators running close to their rated load currents. If there are unused regulators, the user should look at their specific applications and current requirements to decide whether to add extra stages.

Table 3. Recommended Inductors for 1A Buck Regulators

PART NUMBER	L (µH)	MAX I_{DC} (A)	MAX DCR (MΩ)	SIZE IN mm (L × W × H)	MANUFACTURER
IHLP1212ABER1R0M-11	1.0	3	38	3 × 3.6 × 1.2	Vishay
1239AS-H-1R0N	1	2.5	65	2.5 × 2.0 × 1.2	Toko
XFL4020-222ME	2.2	3.5	23.5	4 × 4 × 2.1	CoilCraft
1277AS-H-2R2N	2.2	2.6	84	3.2 × 2.5 × 1.2	Toko
IHLP1212BZER2R2M-11	2.2	3	46	3 × 3.6 × 1.2	Vishay
XFL4020-332ME	3.3	2.8	38.3	4 × 4 × 2.1	CoilCraft
IHLP1212BZER3R3M-11	3.3	2.7	61	3 × 3.6 × 1.2	Vishay

APPLICATIONS INFORMATION

Table 4. Recommended Inductors for 2A Buck Regulators

PART NUMBER	L (µH)	MAX I_{DC} (A)	MAX DCR (mΩ)	SIZE IN mm (L × W × H)	MANUFACTURER
XFL4020-102ME	1.0	5.1	11.9	4 × 4 × 2.1	CoilCraft
74437324010	1	9	27	4.45 × 4.06 × 1.8	Wurth Elektronik
XAL4020-222ME	2.2	5.6	38.7	4 × 4 × 2.1	CoilCraft
FDV0530-2R2M	2.2	5.3	15.5	6.2 × 5.8 × 3	Toko
IHLP2020BZER2R2M-11	2.2	5	37.7	5.49 × 5.18 × 2	Vishay
XAL4030-332ME	3.3	5.5	28.6	4 × 4 × 3.1	CoilCraft
FDV0530-3R3M	3.3	4.1	34.1	6.2 × 5.8 × 3	Toko

Table 5. Recommended Inductors for 3A Buck Regulators

PART NUMBER	L (µH)	MAX I_{DC} (A)	MAX DCR (mΩ)	SIZE IN mm (L × W × H)	MANUFACTURER
XAL4020-102ME	1.0	8.7	14.6	4 × 4 × 2.1	CoilCraft
FDV0530-1R0M	1	8.4	11.2	6.2 × 5.8 × 3	Toko
XAL5030-222ME	2.2	9.2	14.5	5.28 × 5.48 × 3.1	CoilCraft
IHLP2525CZER2R2M-01	2.2	8	20	6.86 × 6.47 × 3	Vishay
74437346022	2.2	6.5	20	7.3 × 6.6 × 2.8	Wurth Elektonik
XAL5030-332ME	3.3	8.7	23.3	5.28 × 5.48 × 3.1	CoilCraft
SPM6530T-3R3M	3	7.3	27	7.1 × 6.5 × 3	TDK

Table 6. Recommended Inductors for 4A Buck Regulators

PART NUMBER	L (µH)	MAX I_{DC} (A)	MAX DCR (mΩ)	SIZE IN mm (L × W × H)	MANUFACTURER
XAL5030-122ME	1.2	12.5	9.4	5.28 × 5.48 × 3.1	CoilCraft
SPM6530T-1R0M120	1	14.1	7.81	7.1 × 6.5 × 3	TDK
XAL5030-222ME	2.2	9.2	14.5	5.28 × 5.48 × 3.1	CoilCraft
SPM6530T-2R2M	2.2	8.4	19	7.1 × 6.5 × 3	TDK
IHLP2525EZER2R2M-01	2.2	13.6	20.9	6.86 × 6.47 × 5	Vishay
XAL6030-332ME	3.3	8	20.81	6.36 × 6.56 × 3.1	CoilCraft
FDVE1040-3R3M	3.3	9.8	10.1	11.2 × 10 × 4	Toko

Table 7. Global Buck Regulator Program Register Bit Format

Bit7	ENABLE	Default is '0' which disables the part. A buck regulator can also be enabled via its enable pin. When enabled via pin, the contents of the I^2C register program its functionality.
Bit6	MODE	Default is '0' which is Burst Mode operation. A '1' programs the regulator to operate in forced continuous mode.
Bit5(PHASE1) Bit4(PHASE0)	Phase Control	Default varies per converter. '00' programs a SW HIGH transition to coincide with the internal clock rising edge. '01' programs a 90° offset, '10' programs a 180° offset, and '11' programs a 270° offset.
Bit3(DAC3) Bit2(DAC2) Bit1(DAC1) Bit0(DAC0)	DAC Control	These bits are used to program the feedback regulation voltage. Default is '1100' which programs a voltage of 725mV. Bits '0000' program the lowest feedback regulation of 425mV, and '1111' programs a full-scale voltage of 800mV. An LSB (DAC0) has a bit weight of 25mV.

APPLICATIONS INFORMATION

V_{CC} Shunt Regulator

If load steps seen on V_{CC} are of great concern, then the compensation capacitor should be tied from V_{CC} to ground as shown in Figure 6a. If load steps are not of a concern, but instead smaller compensation components are desired then the compensation capacitor should be tied from V_{SHNT} to ground as shown in Figure 6b.

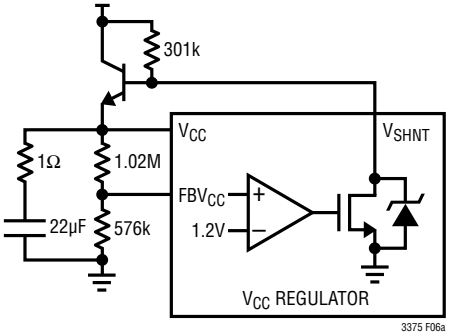


Figure 6a. V_{CC} Regulator Compensated from the V_{CC} Pin

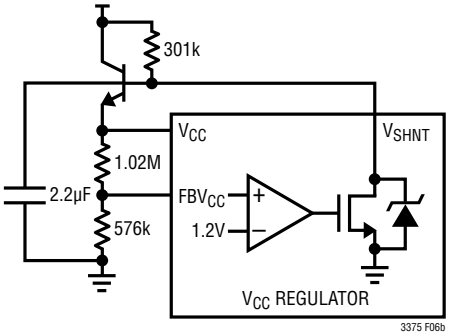


Figure 6b. V_{CC} Regulator Compensated from the V_{SHNT} Pin

The exact components used in the V_{CC} shunt regulator are dependent on the specific conditions used in the application. Care should be taken to make sure that the power dissipation limits of the specific N-type device used are not exceeded, because damage to the external device can lead to damage to the LTC3375.

For an NPN device the pullup resistor between V_{SHNT} and the supply voltage should be sized such that:

$$R_{PULLUP} < \frac{V_{SUPPLY(MINIMUM)} - (V_{CC} + V_{BE})}{I_{VCC(MAX)}} \bullet \beta$$

Where $V_{SUPPLY(MINIMUM)}$ is the lowest possible collector voltage, V_{BE} and β are specific to the NPN in the application, and $I_{VCC(MAX)}$ is the maximum desired load current from V_{CC}.

Likewise R_{PULLUP} may be sized such to current limit I_{VCC} from an NPN device to prevent damage to the circuit from a short on the V_{CC} pin, and to prevent the NPN from exceeding its safe operating current:

$$R_{PULLUP} > \frac{V_{SUPPLY(MAXIMUM)} - (V_{CC} + V_{BE})}{I_{VCC(LIMIT)}} \bullet \beta$$

Where V_{CC} = 0V in the case of a grounded output.

Alternatively, the current may be limited by adding a resistor between V_{CC} and the emitter of the NPN such that:

$$R_{LIM} = \frac{6.1V - (V_{CC} + V_{BE})}{I_{VCC(LIMIT)}}$$

In this case when I_{VCC} exceeds $I_{VCC(LIMIT)}$ V_{CC} will start to collapse. The NPN should be sized to be able to survive at least:

$$I_{VCC(MAX)} = \frac{6.1V - V_{BE}}{R_{LIM}}$$

for the given supply voltage, where 6.1V is the maximum V_{SHNT} voltage (typical).

The user should verify that the circuit is stable over the specific conditions of the desired application. In general increasing the value of the compensation capacitor used or increasing R_{PULLUP} can improve stability. The user should keep in mind that increasing R_{PULLUP} also decreases $I_{VCC(MAX)}$. In general the highest V_{SUPPLY} at $I_{VCC(MAX)}$ yields the worst stability for the circuit in Figure 6a, while the highest V_{SUPPLY} at no load on V_{CC} yields the worst stability for the circuit in Figure 6b.

APPLICATIONS INFORMATION

In general the circuit in 6a is recommended if the application needs to drive any external circuitry with V_{CC} or if the larger compensation capacitor is tolerable. If V_{CC} is only needed to drive the LTC3375 and smaller component sizes are critical, then the circuit in Figure 6b may be used.

Input and Output Decoupling Capacitor Selection

The LTC3375 has individual input supply pins for each buck switching regulator. Each of these pins must be decoupled with low ESR capacitors to GND. These capacitors must be placed as close to the pins as possible. Ceramic dielectric capacitors are a good compromise between high dielectric constant and stability versus temperature and DC bias. Note that the capacitance of a capacitor deteriorates at higher DC bias. It is important to consult manufacturer data sheets and obtain the true capacitance of a capacitor at the DC bias voltage it will be operated at. For this reason, avoid the use of Y5V dielectric capacitors. The X5R/X7R dielectric capacitors offer good overall performance.

The input supply voltage Pins 2, 5, 8, 11, 26, 29, 32 and 35 all need to be decoupled with at least 10µF capacitors.

Choosing the C_T Capacitor

The C_T capacitor may be used to program the timing parameters associated with the pushbutton. For a given C_T capacitor the timing parameters may be calculated as below. C_T is in units of µF.

$t_{\overline{PB}\_LO} = 5000 \bullet C_T$ ms

$t_{\overline{PB}\_ON} = 20000 \bullet C_T$ ms

$t_{\overline{PB}\_OFF} = 1000 \bullet C_T$ seconds

$t_{HR} = 100 \bullet C_T$ seconds

$t_{\overline{IRQ}\_PW} = 5000 \bullet C_T$ ms

$t_{\overline{KILL}H} = 1000 \bullet C_T$ seconds

$t_{\overline{KILL}L} = 5000 \bullet C_T$ ms

$t_{\overline{RST}} = 23000 \bullet C_T$ ms

Programming the Global Register

The Global Register contains functions that either act on the LTC3375 top level or act on all buck switching regulators at once. These functions are described in Table 8. The default structure is '0000 0000b'.

Programming the $\overline{RST}$ and $\overline{IRQ}$ Mask Registers

The $\overline{RST}$ mask register can be programmed by the user at sub-address 09h and its format is shown in Table 9.

If a bit is set to '1', then the corresponding regulator's PGOOD will pull $\overline{RST}$ low if a PGOOD fault were to occur. The default for this register is FFh.

The $\overline{IRQ}$ mask registers have the same bit format as the $\overline{RST}$ mask register. The $\overline{IRQ}$ mask registers are located at sub-addresses 0Ah and 0Bh and their default contents are 00h.

Status Byte Read Back

When either the $\overline{RST}$ or $\overline{IRQ}$ pin is pulled low, it indicates to the user that a fault condition has occurred. To find out the exact nature of the fault, the user can read the status registers. There are three registers that contain status information. The register at sub-address 0Ch provides PGOOD fault condition reporting, while the register at sub-address 0Dh provides UVLO fault condition reporting. These bits are all latched at interrupt. If any of the bits are disabled via masking, then their real time, unlatched status information is still available. Bit7 of the register at sub-address 0Eh provides latched information on the status of the DT Warning. Figure 4 shows the operation of the status registers. The contents of the $\overline{IRQ}$ status register are cleared when a CLRINT signal is issued. A PGOOD bit is a '0' if the regulator's output voltage is more than 7.5% below its programmed value. A UVLO bit is a '0' if the associated V_{IN} is above its input UVLO threshold. The format for the status registers is shown in Table 10.

A write operation cannot be performed to any of these status registers.

APPLICATIONS INFORMATION

Table 8. Global Control Program Register Bit Format

Bit7	RESET_ALL	Default is '0'. When asserted all buck converters will power down for 1 second after which the bit will clear itself.
Bit6(DT1) Bit5(DT0)	DT WARNING CONTROL	Default is '00' which deactivates the DT warning. '01' programs –140°, '10' programs –125°, and '11' programs –110°.
Bit4	IGNORE_EN	Default is '0' which allows the EN pins to power on the buck converters. When written to '1' the enable pins will be ignored. This allows power-down sequencing via I^2C even if the EN pins are tied to a logic HIGH voltage source.
Bit3	1KPD	Default is '0' in which the SW node remains in a high impedance state when the regulator is in shutdown. A '0' pulls the SW node to GND through a 10k resistor. This bit acts on all buck converters at once.
Bit2	SLOW EDGE	This bit controls the slew rate of the switch node. Default is '0' which enables the switch node to slew at a faster rate, than if the bit were programmed a '1'. This bit acts on all buck converters at once.
Bit1	RD_TEMP	Default is '0'. This bit commands the temperature A/D to sample the voltage present at the TEMP pin. After a read is complete this bit will clear itself.
Bit0	Unused	This bit is unused and must be written to "0"

Table 9

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
PGOOD[8]	PGOOD[7]	PGOOD[6]	PGOOD[5]	PGOOD[4]	PGOOD[3]	PGOOD[2]	PGOOD[1]

Table 10

Sub-Address	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0Ch	PGOOD[8]	PGOOD[7]	PGOOD[6]	PGOOD[5]	PGOOD[4]	PGOOD[3]	PGOOD[2]	PGOOD[1]
0Dh	UVLO[8]	UVLO[7]	UVLO[6]	UVLO[5]	UVLO[4]	UVLO[3]	UVLO[2]	UVLO[1]
0Eh	DT_WARN	TEMP[6]	TEMP[5]	TEMP[4]	TEMP[3]	TEMP[2]	TEMP[1]	TEMP[0]

PCB Considerations

When laying out the printed circuit board, the following list should be followed to ensure proper operation of the LTC3375:

1. The exposed pad of the package (Pin 49) should connect directly to a large ground plane to minimize thermal and electrical impedance.
2. All the input supply pins should each have a decoupling capacitor.
3. The connections to the switching regulator input supply pins and their respective decoupling capacitors should be kept as short as possible. The GND side of these capacitors should connect directly to the ground plane of the part. These capacitors provide the AC current to the internal power MOSFETs and their drivers. It is important to minimize inductance from these capacitors to the V_{IN} pins of the LTC3375.
4. The switching power traces connecting SW1, SW2, SW3, SW4, SW5, SW6, SW7 and SW8 to their respective inductors should be minimized to reduce radiated EMI and parasitic coupling. Due to the large voltage swing of the switching nodes, high input impedance sensitive nodes, such as the feedback nodes, should be kept far away or shielded from the switching nodes or poor performance could result.
5. The GND side of the switching regulator output capacitors should connect directly to the thermal ground plane of the part. Minimize the trace length from the output capacitor to the inductor(s)/pin(s).
6. In a combined buck regulator application the trace length of switch nodes to the inductor must be kept equal to ensure proper operation.

TYPICAL APPLICATIONS

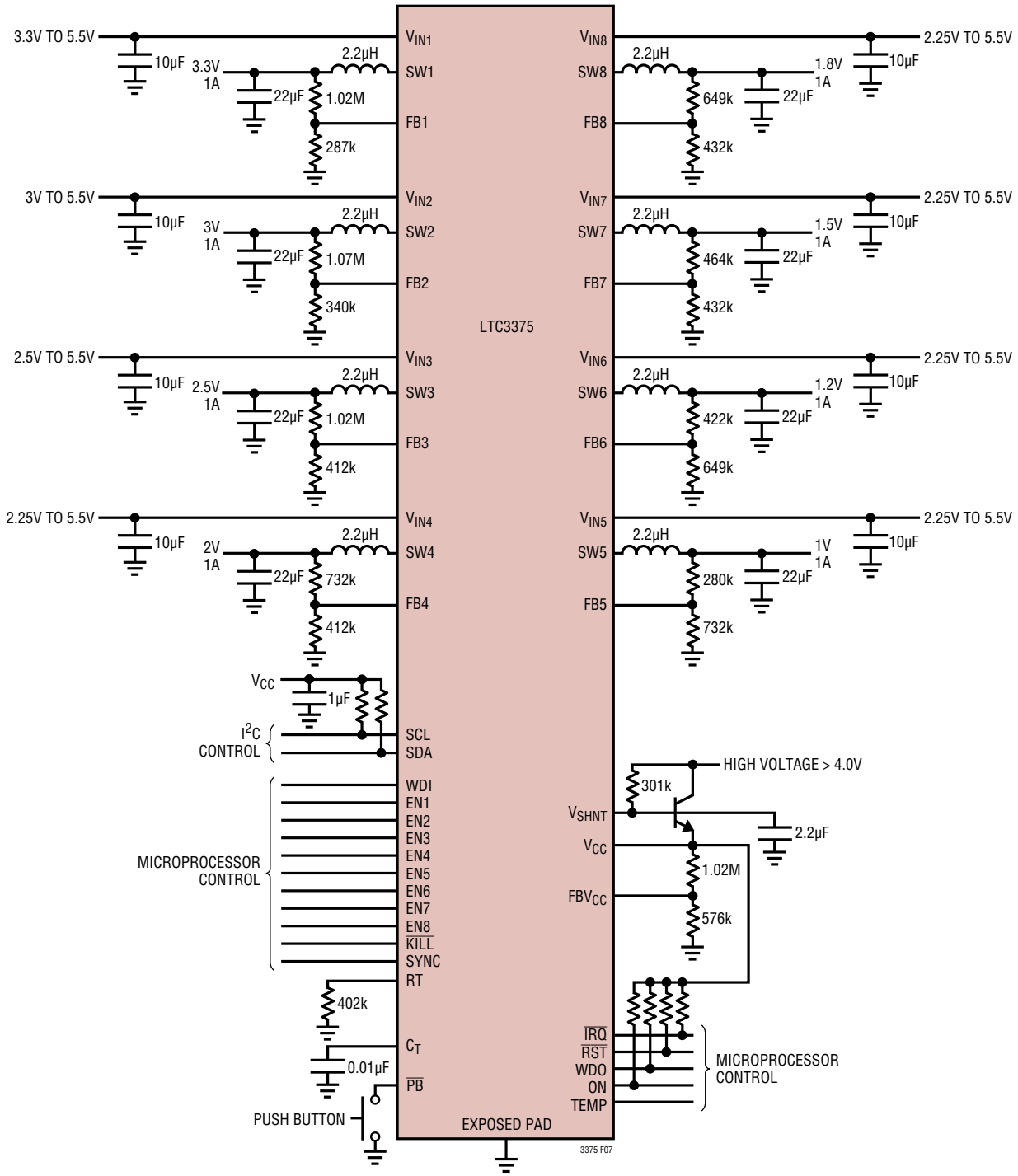


Figure 7. Detailed Front Page Application Circuit

TYPICAL APPLICATIONS

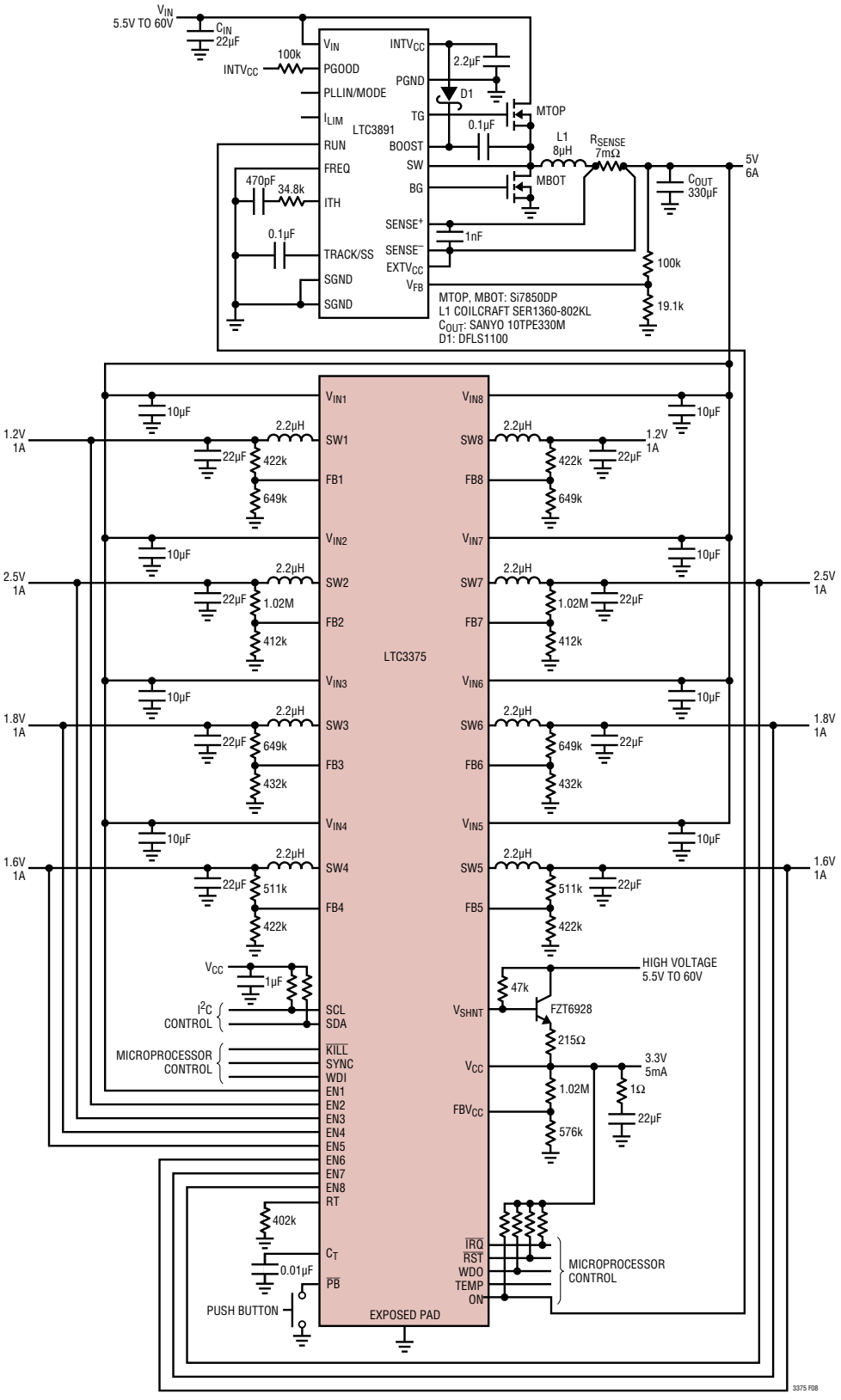


Figure 8. Buck Regulators with Sequenced Start-Up Driven from a High Voltage Upstream Buck Converter

TYPICAL APPLICATIONS

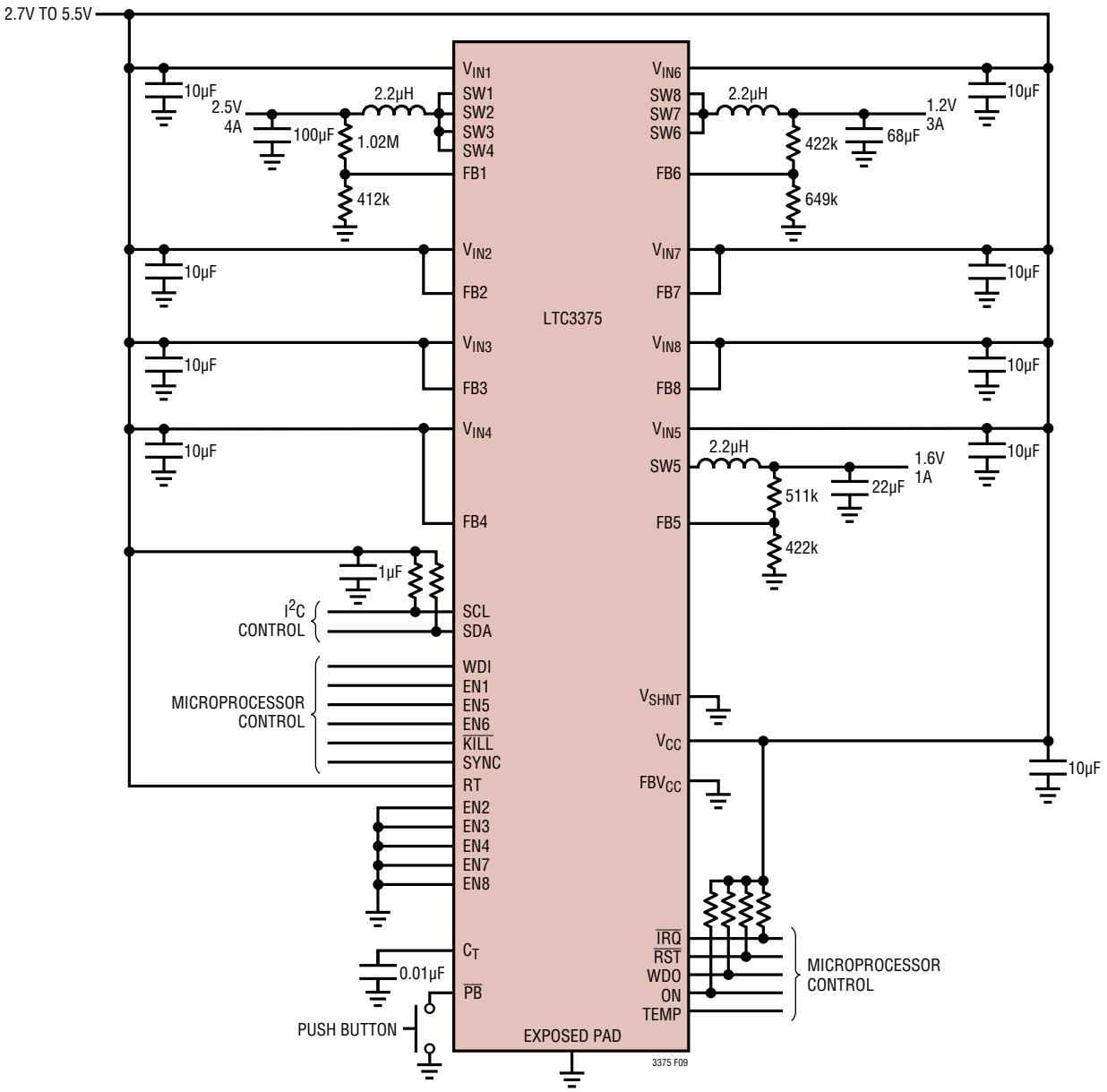
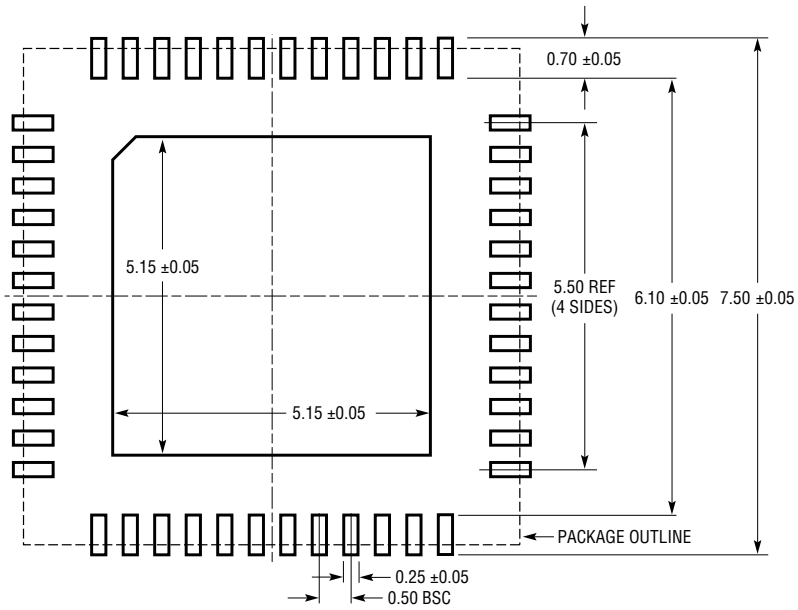


Figure 9. Combined Buck Regulators with Common Input Supply

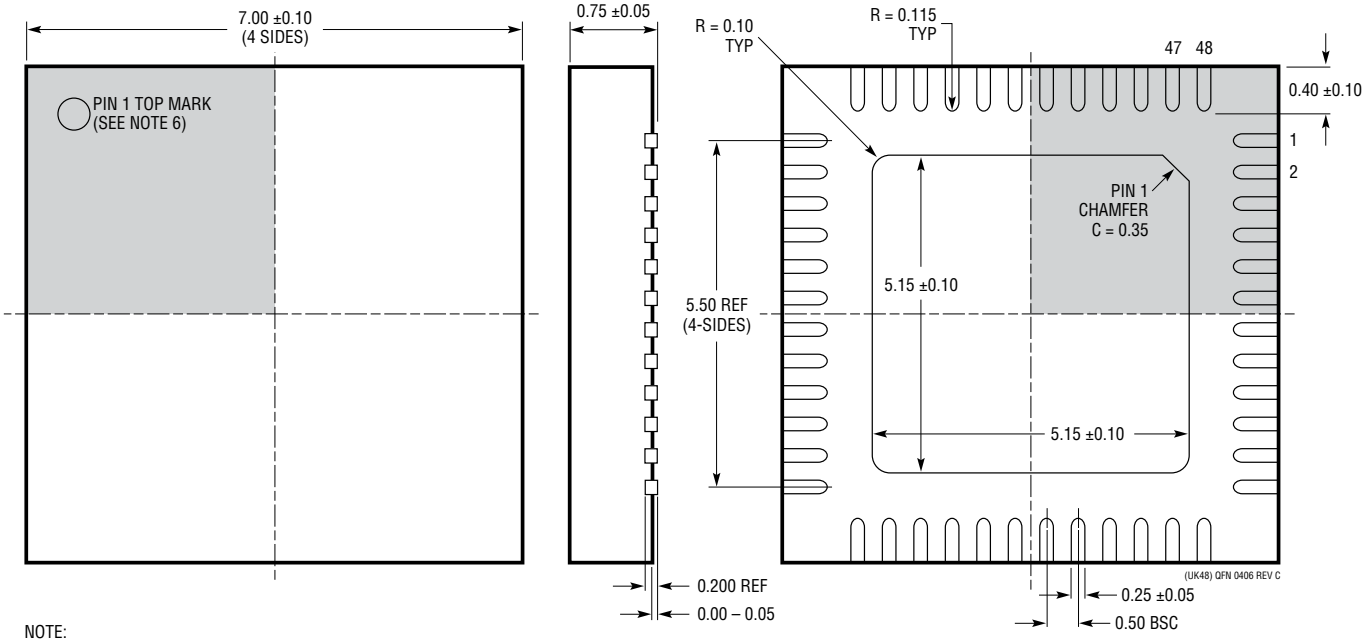
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

UK Package
48-Lead Plastic QFN (7mm × 7mm)
(Reference LTC DWG # 05-08-1704 Rev C)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



BOTTOM VIEW—EXPOSED PAD

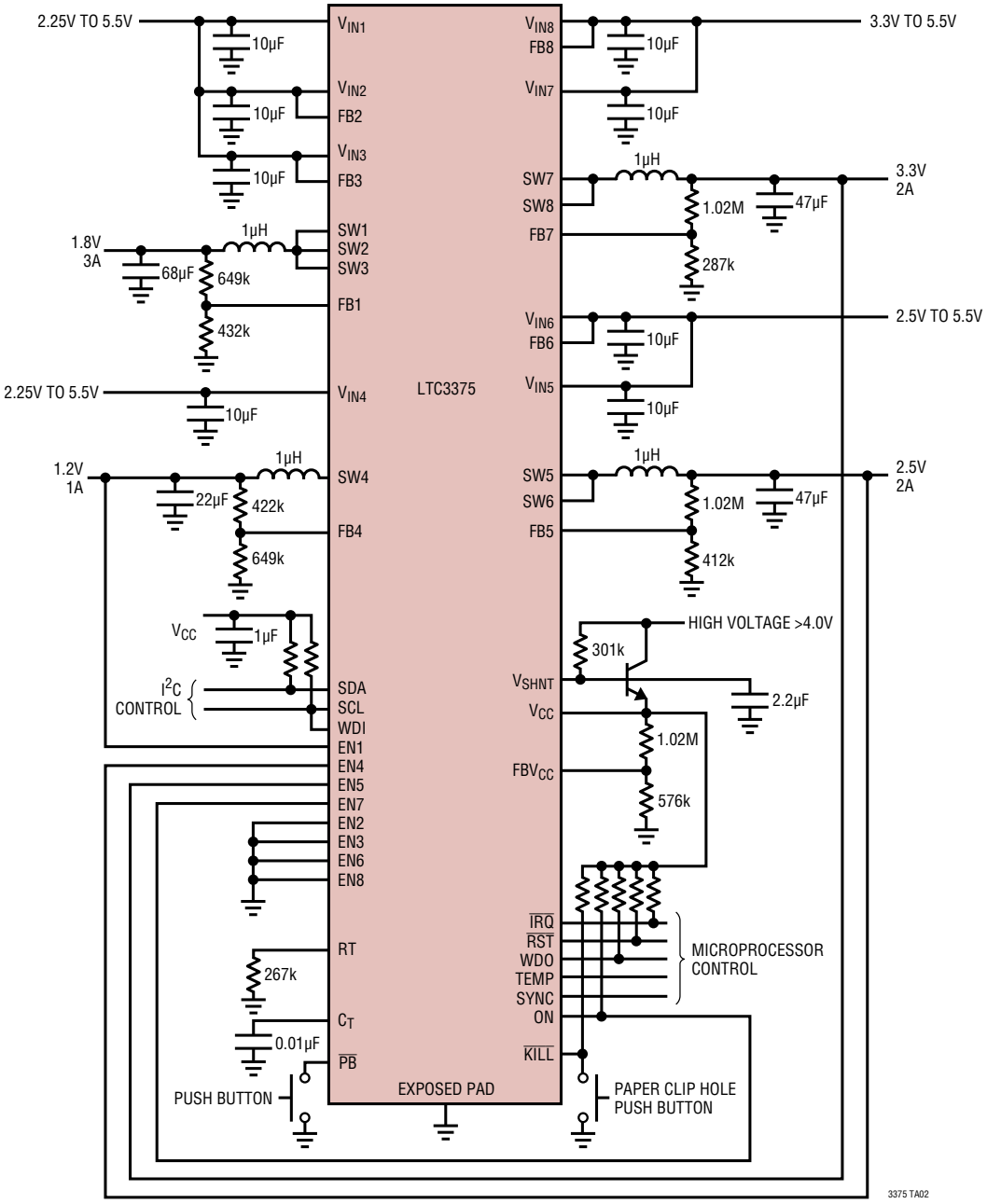
NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION (WKKD-2)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE, IF PRESENT
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	03/13	Clarified V_{CC} input supply current specification	4
		Clarified RST pin functionality	12
		Clarified Buck Regulators with Combined Power Stages	16, 17
		Clarified Table 6 Recommended Inductor Ratings	27

TYPICAL APPLICATION

Combined Bucks with 3MHz Switch Frequency, Sequenced Power Up, and $\overline{KILL}$ Based Hardware Override Shut Down



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3675	7-Channel Configurable High Power PMIC	Four Parallelable Buck DC/DCs (1A, 1A, 500mA, 500mA), 1A Boost, 1A Buck-Boost, 25mA LDO, Dual String LED Driver, Pushbutton, I²C Control
LTC3589/LTC3589-1	8-Output Regulator with Sequencing and I²C	Three Buck DC/DCs, Three 250mA LDOs, 25mA LDO, 1.2A Buck-Boost, Pushbutton, I²C Control

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