Siliconix incorporated

D125
Monolithic 6-Channel FET Switch Drivers

FEATURES

- TTL Compatible
- DC Level Shifting to > 19 V
- Fast Switching (t_{OFF} < 1.5 µs)

BENEFITS

- Reduces System Component Requirements
- Fast Level Shifting

APPLICATIONS

- Interfacing Low Level Logic to MOSFETs or JFETs

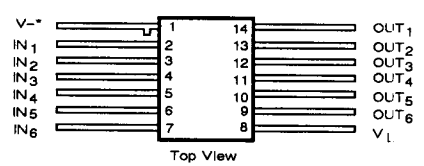
DESCRIPTION

The D125 contains six drivers, designed to perform the level-shifting and amplification needed to interface low-level logic outputs and field-effect transistor switches (MOSFET or JFET). With the input logic supply, (V_L), at 5 V, the driver output reference, (V–) may be set between –1 and –25 V. Each output is designed to sink 5 mA of current in the ON condition, and to hold off up to 30 V in the OFF condition. The input stage is a base-input PNP transistor, with the emitter returned to the V_L supply through a resistor. To turn the driver ON, the logic stage driving it must be capable of sinking 0.7 mA.

Package options include the 14-pin side braze and flatpack packages. Performance grades include both the industrial, B suffix (–25 to 85°C) and military, A suffix (–55 to 125°C) temperature ranges.

PIN CONFIGURATION

Flat Package

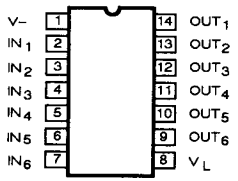


Top View

Order Numbers: D125AL/883

* Common to Substate and Base of Package

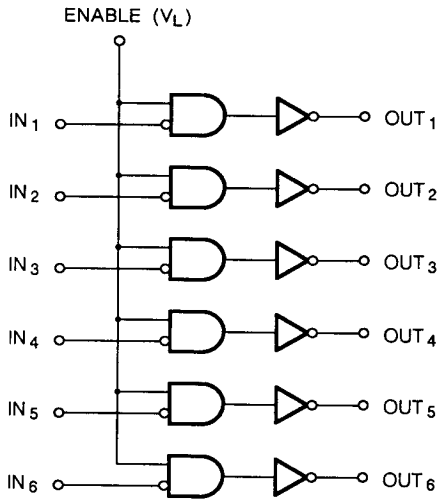
Dual-In-Line Package



Top View

Order Numbers:
D125AP, D125BP

FUNCTIONAL BLOCK DIAGRAM



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Not Recommended for New Designs

ABSOLUTE MAXIMUM RATINGS

V_O to V- ..... 36 V
V_L to V- ..... 30 V
V_{IN} to V- ..... 30 V
V_{IN} to V_L ..... ±6 V
Current, (Any Terminal) ..... 30 mA
Storage Temperature ..... -65 to 150°C

Operating Temperature (A Suffix) ..... -55 to 125°C
(B Suffix) ..... -25 to 85°C

Power dissipation*
Flat Package** ..... 750 mW
14-Pin DIP*** ..... 825 mW

* All leads soldered or welded to PC board.
** Derate 10 mW/°C above 75°C.
*** Derate 11 mW/°C above 75°C.

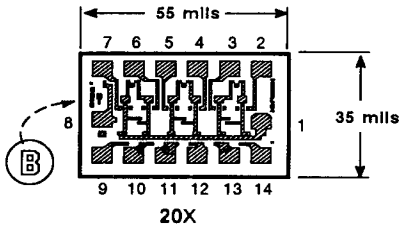
ELECTRICAL CHARACTERISTICS [a]

PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V- = 20 V, V_L = 5 V	LIMITS 1=25°C 2=125,85°C 3=-55,-25°C		A SUFFIX -55 to 125°C		B SUFFIX -25 to 85°C		UNIT
			TEMP	TYP [d]	MIN [b]	MAX [b]	MIN [b]	MAX [b]	
OUTPUT									
Output Voltage LOW	V_{OL}	I_O = 5 mA, V_L = 4.5 V, V_{IN} = 0.5 V	1,3 2	-19.8		-19.6 -19.5		-19.6 -19.5	V
Output Current HIGH	I_{OH}	V_O = 10 V, V_{IN} = 4.6 V	1,3 2	0.005		0.1 10		0.1 10	µA
INPUT									
Input Current Voltage HIGH	I_{INH}	V_{IN} = 4.6 V	1,3 2	0.001	-1 -10	1 10	-1 -20	1 20	µA
Input Current Voltage LOW	I_{INL}	V_{IN} = 0	1,2,3	-0.15	-0.7		-1		mA
DYNAMIC									
Turn-ON Time	t_{ON}	See Switching Time Test Circuit	1	0.11		0.5		0.5	µs
Turn-OFF Time	t_{OFF}		1	1.05		1.2		1.5	
SUPPLY									
Negative Supply Current	I_-	V_{IN1} = 0, All Other V_{IN} = 4.6 V	1,2,3	-1.5	-2.5		-2.5		mA
Logic Supply Current	I_L		1,2,3	1.6		2.5		2.5	
Negative Supply Current	I_-	All V_{IN} = 4.6 V	1,3 2	-0.09	-2 -200		-2 -100		µA
Logic Supply Current	I_L		1,3 2	0.09		1 100		2 100	

NOTES:
a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Guaranteed by design, not subject to production test.
d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Not Recommended for New Designs

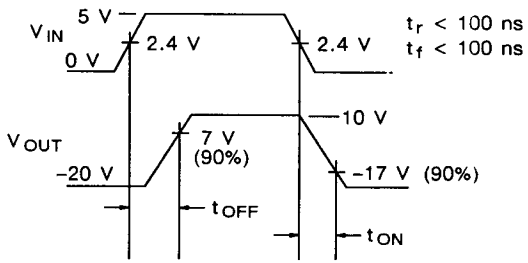
DIE TOPOGRAPHY

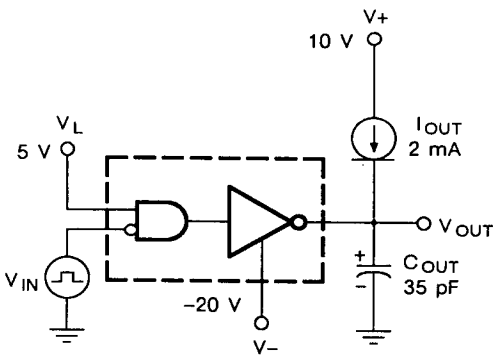


IBAF
12 Resistors
6 PNP bipolar Transistors
6 NPN Bipolar Transistors

Pad No.	Function
1	V- (Substrate)
2	Input 1
3	Input 2
4	Input 3
5	Input 4
6	Input 5
7	Input 6
8	V_L
9	Output 6
10	Output 5
11	Output 4
12	Output 3
13	Output 2
14	Output 1

SWITCHING TIME TEST CIRCUIT





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