HARRIS

HI-DAC16B/ DAC16C

16-Bit D to A Converter

Features

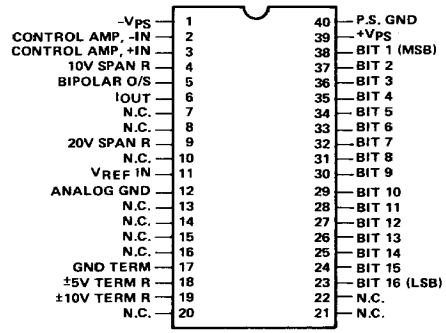
- 16 BIT RESOLUTION
- MONOLITHIC DI BIPOLAR CONSTRUCTION
- FAST SETTLING TIME — 1 μs TO .003%FS
- LOW DIFF. NONLIN. DRIFT — ±0.3ppm/°C
- LOW GAIN DRIFT — ±1ppm/°C
- ON-CHIP SPAN & OFFSET RESISTORS
- TTL/5V-CMOS COMPATIBLE
- LOW UNIPOLAR OFFSET — ≤1/2LSB@ +25°C
- LOW UNIPOLAR OFFSET T.C. — ±0.2ppm/°C
- EXCELLENT STABILITY

Applications

- HIGH RESOLUTION CONTROL SYSTEMS
- HIGH FIDELITY AUDIO RECONSTRUCTION
- PRECISION FUNCTION GENERATION AND INSTRUMENTATION

Pinout

TOP VIEW



Description

The HARRIS HI-DAC16 is a 16-bit, current output D/A converter. Single chip construction includes thin-film application resistors for use with an external op amp. These permit standard output voltage ranges of 0 to +5V, 0 to +10V, ±2.5V, ±5V and ±10V. The HI-DAC16B is monotonic to 15 bits; and the HI-DAC16C to 14 bits.

Reference and span resistors have adjacent placement on the chip for optimum match and thermal tracking. Futhermore, this layout feature helps minimize the superposition error caused by self-heating of the span resistor, reducing it to less than 1/10LSB. This and other design innovations have produced exceptionally stable operation over temperature. Typical temperature coefficients are ± 1ppm/°C for gain error and 0.3ppm/°C for differential non-linearity error.

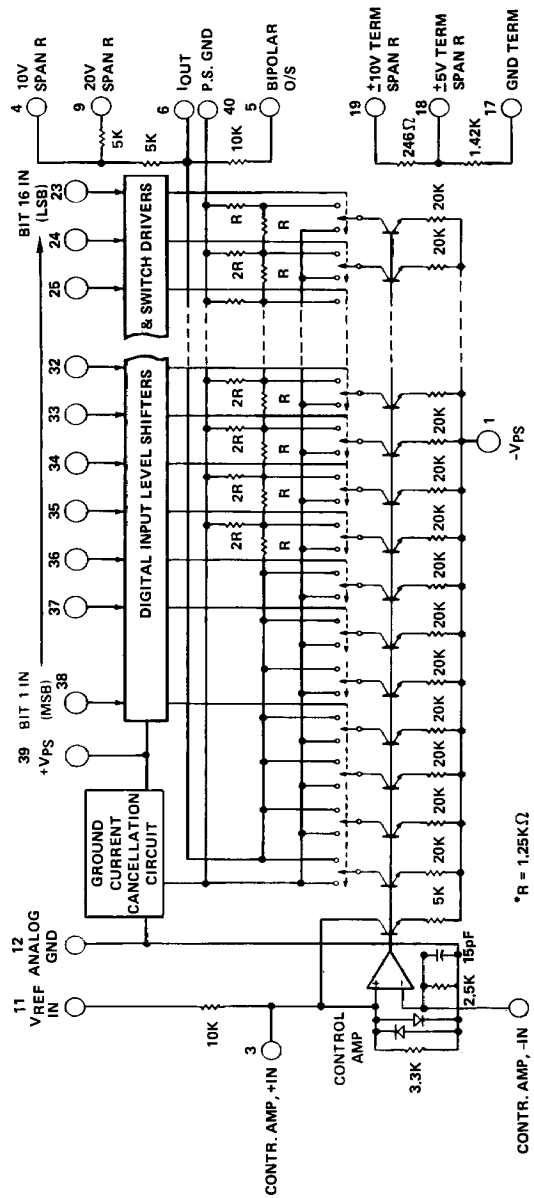
The internal architecture is an extension of the earlier HI-562 with several major improvements. All code dependent ground currents are steered to a separate non-critical path, namely, power supply ground. This feature allows the precision ground of the converter to be sensed with virtually zero voltage drop referred to system ground. The result is the complete elimination of non-linearities due to code dependent ground currents while yielding an extremely low unipolar offset of less than 1/2LSB. Because of this separation, the user may route the precision ground some distance to the system ground without degrading converter accuracy.

The HARRIS HI-DAC16 delivers a stable, accurate output without sacrifice in speed. Settling time to within ±0.003% is one microsecond. Overall performance of this monolithic device should be attractive for applications such as high fidelity audio and high-resolution control systems.

Two accuracy grades are offered, and typical power dissipation is 465mW. Package is a 40 pin ceramic DIP. For further information, see Application Note 539.

CAUTION: These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

Functional Diagram



Absolute Maximum Ratings (Referred to Ground)

Power Supply Inputs	$V_{ps}+$	+20V	Junction Temperature	175°C
	$V_{ps}-$	−20V	Operating Temperature Range	
Reference Inputs	V_{REF} (Hi)	$\pm V_{ps}$		
Digital Inputs	Bits 1 to 16	−1V, +12V	HI-DAC 16B/C	0°C to +75°C
Outputs		$\pm V_{ps}$	Storage Temperature Range	−65°C to +150°C

Electrical Specifications (T_A = +25°C, V_{ps} = ±15V, V_{ref} = +10V, unless otherwise specified)

PARAMETER	CONDITIONS	HI-DAC16B MIN	HI-DAC16B TYP	HI-DAC16B MAX	HI-DAC16C MIN	HI-DAC16C TYP	HI-DAC16C MAX	UNITS
INPUT CHARACTERISTICS								
Digital Inputs	Bit ON "Logic 1" Bit OFF "Logic 0"							
Input Voltage								
Logic "1"	Full Temperature Range	2.0			2.0			V
Logic "0"				0.8			0.8	V
Input Current								
Logic "1"			20	500		20	500	nA
Logic "0"		-50			-50			μA
Reference Input								
Input Resistance			10			10		kΩ
Input Voltage			10			10		V
TRANSFER CHARACTERISTICS								
Resolution	Full Temperature Range		16			16		Bits
Nonlinearity	25°C		±0.0023			±0.0045		%FSR(3)
	Full Temperature Range			±0.0045			±0.009	
Differential Nonlinearity	25°C		±0.0015			±0.003		%FSR
	Full Temperature Range			±0.003			±0.006	
Relative Accuracy (5)	With 100Ω(1%) Trim Resistors							
Unipolar Gain Error	All Bits ON		±0.1	±0.25		±0.1	±0.25	
Bipolar Offset Error	All Bits OFF		±0.15	±0.43		±0.15	±0.43	%FSR
Unipolar Offset Error			±0.002	±0.05		±0.002	±0.05	
Adjustment Range	See Operating Instructions							
Gain	Using Trim Potentiometers			±3			±3	%FSR
Bipolar Offset	as shown in Figure 1			±0.43			±0.43	
Temperature Stability	Drift specified with internal span resistors for voltage output							
Gain Drift (2)	Full Temperature Range		±1	±5		±1	±5	ppm of FSR/°C
Offset Drift (2)								
Unipolar Offset	All Bits OFF		±0.2			±0.2		
Bipolar Offset			±0.5			±0.5		
Differential Nonlinearity	Full Temperature Range		±0.3			±0.3		
Settling Time (2) to ±0.003%FS	All Bits ON-to-OFF or OFF-to-ON		1.0			1.0		μs

Specifications HI-DAC16B/DAC16C

PARAMETER	CONDITIONS	HI-DAC16B			HI-DAC16C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Glitch (2)	From 0111 . . .1 to 100 . . . 0 or 100 . . . 0 to 011 . . . 1		1300			1300		mV–ns
Power Supply (2) Rejection Ratio, PSRR (3) $V_{ps}+$ $V_{ps}-$			1.5 1.5			1.5 1.5		ppm of FSR/% V_{ps}
OUTPUT CHARACTERISTICS								
Output Current Unipolar Bipolar		-1.6 ±0.8	-2 ±1	-2.4 ±1.2	-1.6 ±0.8	-2 ±1	-2.4 ±1.2	mA
Resistance			2.5k			2.5k		
Capacitance			10			10		pF
Output Voltage Ranges Unipolar Bipolar	Using external op amp and internal scaling resistors. See Figure 1 and Table 1 for connections		0 to +5 0 to +10 ±2.5 ±5 ±10			0 to +5 0 to +10 ±2.5 ±5 ±10		V
Compliance Limit (2)		-3		+10	-3		+10	V
Compliance Voltage (2)	Full Temperature Range		±1			±1		V
Output Noise	0.1 to 5MHz (All bits ON)		30			30		μVRMS
POWER REQUIREMENTS								
$V_{ps}+$ (7) $V_{ps}-$	Full Temperature Range	13.5 -13.5	+15 -15	16.5 -16.5	13.5 -13.5	+15 -15	16.5 -16.5	V
$I_{ps}+$ (4) $I_{ps}-$ (4)	All Bits ON or OFF Full Temperature Range	-25	+13 -18	+18	-25	+13 -18	+18	mA
Power Dissipation			465			465		mW

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impared. Functional operation under any of these conditions is not necessarily implied.
2. See Definitions.
3. FSR is "full scale range" and is 20V for ±10V range, 10V for ±5V range, etc., or 2mA (±20%) for current output.
4. After 30 seconds warm-up.
5. Using an external op amp with internal span resistors and specified external trim resistors in place of potentiometers R_1 and R_2. Errors are adjustable to zero using R_1 and R_2 potentiometers. (See Operating Instructions Figure 2.)

Definition of Specifications

DIGITAL INPUTS

The HI-DAC 16B/C accepts digital input codes in binary format and may be user connected for any one of three binary codes. Straight Binary, Two's Complement, or Offset Binary. (See Operation Instructions).

DIGITAL INPUT	ANALOG OUTPUT		
	Straight Binary	Offset Binary	Two's Complement *
MSB LSB			
000...000	Zero	-FS 9(Full Scale)	Zero
100...000	½FS	Zero	−FS
111...111	+FS − 1 LSB	+FS − 1 LSB	Zero − 1 LSB
011...111	½FS − 1 LSB	Zero − 1 LSB	+FS − 1 LSB

*Invert MSB with external inverter to obtain Two's Complement Coding

ACCURACY

INTEGRAL NONLINEARITY – The maximum deviation of the actual transfer characteristic from an ideal straight line. The ideal line is positioned according to "end-point linearity" for D/A converter products from Harris Semiconductor, i.e. the line is drawn between the end-points of the actual transfer characteristic (codes 00...0 and 11...1).

DIFFERENTIAL NONLINEARITY – The difference between one LSB and the output voltage change corresponding to any two consecutive codes. A Differential Nonlinearity of ±1 LSB or less guarantees monotonicity.

MONOTONICITY – The property of a D/A converter's transfer function which guarantees that the output derivative will not change sign in response to a sequence of increasing (or decreasing) input codes. That is, the only output response to a code change is to remain constant, increase for increasing code, or decrease for decreasing code.

SETTLING TIME

Settling time is the time required for the output to settle to within the specified error band for any input code transition. It is usually specified for a full scale or major carry transition.

DRIFT

GAIN DRIFT – The change in full scale analog output over the specified temperature range expressed in parts per million of full scale per °C (ppm of FSR/°C). Gain error is measured with respect to +25°C at high (T_H) and low (T_L) temperatures. Gain drift is calculated for both high (T_H −25°C) and low ranges (+25°C−T_L) by dividing the gain error by the respective change in temperature. The specification is the larger of the two representing worst case drift.

OFFSET DRIFT – The change in analog output with all bits OFF over the specified temperature range expressed in parts per million of full scale range per °C (ppm of FSR/°C). Offset error is measured with respect to +25°C at high (T_H) and low (T_L) temperatures. Offset Drift is calculated for both high (T_H −25°C) and low (+25°C −T_L) ranges by dividing the offset error by the respective change in temperature. The specification given is the larger of the two, representing worst-case drift.

POWER SUPPLY SENSITIVITY

Power Supply Sensitivity is a measure of the change in gain and offset of the D/A converter resulting from a change in −15V, or +15V supplies. It is specified under DC conditions and expressed as parts per million of full scale range per percent of change in power supply (ppm of FSR/%).

COMPLIANCE

Compliance Voltage is the maximum output voltage range that can be tolerated and still maintain its specified accuracy. Compliance Limit implies functional operation only and makes no claims to accuracy.

GLITCH

A glitch on the output of a D/A converter is a transient spike resulting from unequal internal ON–OFF switching times. Worst case glitches usually occur at half-scale or the major carry code transition from 011...1 to 100...0 or vice versa. For example, if turn ON is greater than turn OFF for 011...1 to 100...0, an intermediate state of 000...0 exists, such that, the output momentarily glitches toward zero output. Matched switching times and fast switching will reduce glitches considerably. (Calculated as the product of duration and amplitude.)

Operating Instructions

UNIPOLAR AND BIPOLAR VOLTAGE OUTPUT CONNECTIONS

FIGURE 1

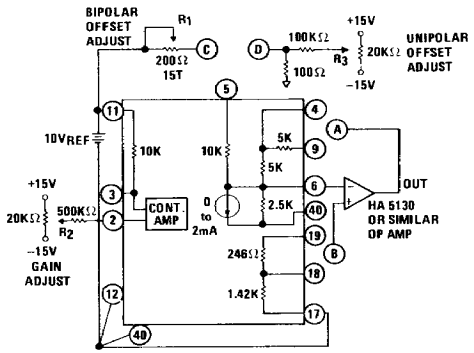


TABLE 1

	OUTPUT RANGE	CONNECTIONS PIN5 to	PIN4 to	PIN9 to	PIN B to
UNIPOLAR MODE	0 to +10V	D	A	N.C.	19
	0 to +5V	D	A	PIN6	*
BIPOLAR MODE	±10V	C	N.C.	A	19
	±5V	C	A	N.C.	18
	±2.5V	C	A	6	*

*Connect an external 1.1K ohm resistor to ground.

GAIN AND ZERO CALIBRATION

The HI-DAC16B/C input reference resistor, bipolar offset resistor and span resistors are optimized for excellent tracking over temperature. LASER trimming of the reference circuit resistors corrects the unipolar Gain and Offset errors to high accuracy. The remaining error can be adjusted with trimming potentiometers. The bipolar Gain and Offset errors are greater since the LASER correction is done in the unipolar mode, however these too are easily adjusted. Figure 1 illustrates the connections for unipolar and bipolar operation. Trimming potentiometers R_1, R_2, and R_3 are required for adjustment.

UNIPOLAR CALIBRATION

Step 1: Offset
- Turn all bits OFF (00..0)
- Adjust R_3 for zero volts output

Step 2: Gain
- Turn all bits ON (11..1)
- Adjust R_2 for an output of FS-1 LSB
  That is, adjust for:

  9.999847 for +10V range
  4.999924 for +5V range

BIPOLAR CALIBRATION

Step 1: Offset
  Turn all bits OFF (00..0)
  Adjust R_1 for an output of
  −10V for ± 10V range
  −5V for ± 5V range
  −2.5V for ± 2.5V range

Step 2: Gain
  Turn all bits ON (11..1)
  Adjust R_2 for FS-1LSB output
  That is, adjust for:

  9.999695 for ±10V range
  4.999847 for ± 5V range
  2.499924 for ± 2.5V range

Other Considerations

GROUNDS

The HI-DAC16 has two ground terminals, pin 12 (REF GND) and pin 40 (PWR GND). These should not be tied together near the package unless that point is also the system signal ground to which all returns are connected. (If such a point exists, then separate paths are required to pins 12 and 40).

The current through pin 12 is near-zero DC*, but pin 40 carries up to 1.75mA of code - dependent current from bits 1, 2, and 3. The general rule is to connect pin 12 directly to the system signal, or analog ground. Connect pin 40 to the local digital or power ground. Then, of course, a single path must connect the analog/signal and digital/power grounds.

Other Considerations (Continued)

*Current cancellation is a two-step process in which code-dependent variations are eliminated, then the resulting DC current is supplied internally. First, an auxiliary 13-bit R-2R Ladder is driven by the complement of the DAC's input code. Together the main and auxiliary ladders draw a continuous 3.25mA from the internal ground node, regardless of input code. Part of this DC current is supplied by the zener voltage reference, and the remainder is sourced from the positive supply via a current mirror which is laser trimmed for zero current through the external terminal (pin 12).

LAYOUT

Connections to pin 6 (I_{OUT}) on the HI-DAC16 are most critical for high speed performance. Output capacitance of the DAC is only 10pF, so a small additional capacitance will alter the op amp's stability and affect settling time. Connections to pin 6 should be short and few. Component leads should be short on the side connecting to pin 6.

BYPASS CAPACITORS

Power supply bypass capacitors on the op amp will serve the HI-DAC16 also. If no op amp is used, a 0.01μF ceramic capacitor from each supply terminal to pin 40 is sufficient, since supply current variations are small.

THERMAL EFFECTS

A consideration when using the DAC16 is Temperature Stability. In applications where full scale shift could be a problem, the use of a heat sink and/or a cooling fan is suggested. This will decrease the magnitude of the total variation by lowering the effective thermal resistance between the package and its environment. The device should be kept in a stable isothermal environment, and a warm-up time consistent with accuracy requirements should be provided.

SELECTING AN OPERATIONAL AMPLIFIER

The HI-DAC16 is a high resolution, high accuracy DAC. Many applications will require an op-amp used as a current-to-voltage converter at the DAC output. (Careful consideration should be given the choice of this amplifier as a poor selection can seriously degrade the inherent qualities of the DAC.)

The HA-5130 is an excellent choice to maintain high accuracy with an average Offset Drift of only 0.4 μV/°C leading to an error over temperature of 30 μV (0.0003% FSR for a 10V FS). Initial offset and bias current are 10 μV and 3nA respectively, while input noise current of 0.2pA/$\sqrt{Hz}$. Settling time is adequate for most audio applications. (11 μs typ. to 0.1%).

COMPOSITE AMPLIFIER

It is desirable at times to have an output amplifier which combines the qualities of those op-amps available to the designer. For instance one may wish to combine the excellent front-end characteristics of the HA-5130 with the speed of a device such as the HA-2540 (t_{settle} =250ns to 0.1%). In these instances there is the option of the composite amplifier. The basic configuration is shown in Figure 2.

COMPOSITE AMPLIFIER

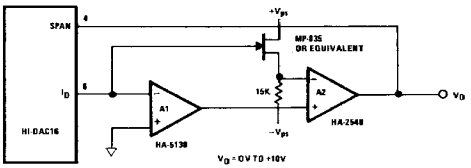


FIGURE 2

The composite amplifier may be used to achieve a compromise depending on the requirements of a design. Trade-offs in performance can be made and the following equations apply:

Offset; $$V_{OFF} = \frac{V_{OFF2}}{A_{01}} + V_{OFF1}$$

Bias; $$I_{BIAS} = I_{BIAS2} + I_{BIAS1}$$

Gain; $$\frac{V_0}{V_1} = A_{V}(S) = A_{V2}(S)\,[1 + A_{V1}(S)]$$

The amplifier A_2 should be of wide bandwidth and fast settling time.

Die Characteristics

Transistor Count		190
Die Size:		215 x 125 mils
Thermal Constants;	θ_{ja}	41°C/W
	θ_{jc}	11°C/W
Tie Substrate to:		Analog Ground
Process:		Bipolar - DI