PRELIMINARY

5 VOLT SERIES 200 FLASH MEMORY MINIATURE CARD

iFM004G, iFM008G and iFM016G

- **Low-Cost Linear Flash Card**
  - **5 Volt Intel® StrataFlash™ Memory Flash Technology**
- **Fast Read Performance**
  - **150 ns Max Access Time**
- **High-Performance Writes**
  - **12 µs Typical Byte Write**
- **32 Byte Write Buffer**
  - **Frees CPU to Perform Other Tasks**
- **Low Deep Power-Down Current**
  - **145 µA Maximum for 4-MB Card**
- **x16 Data Interface**
- **Single Supply Operation**
  - **5 V Read/Write**
- **Automated Write and Erase Algorithms**
  - **CFI and SCS Compliant**
- **Enhanced Automated Suspend Options**
  - **Block Erase Suspend to Write**
  - **Block Erase Suspend to Read**
- **Enhanced Data Protection Features**
  - **Flexible Block Locking**
- **100,000 Erase Cycles per Block**
- **128-Kbyte Erase Blocks**

The Intel® Series 200 Miniature Cards deliver the benefits of Intel® StrataFlash™ memory to users of portable electronic systems. Capitalizing on two-bit-per-cell technology, Intel StrataFlash memory products provide 2X the bits in 1X the space. Intel StrataFlash memory devices are the first to bring reliable, two-bit-per-cell storage technology to the flash memory market.

Intel StrataFlash memory benefits include: more density in less space, lowest cost-per-bit NOR devices, support for code and data storage, and easy migration to future devices.

Using the same NOR-based ETOX™ technology as Intel's one-bit-per-cell products, Intel StrataFlash memory devices take advantage of 400 million units of manufacturing experience since 1988. As a result, Intel StrataFlash components are ideal for code or data applications where high density and low cost are required. Examples include networking, telecommunications, audio recording, and digital imaging.

Intel StrataFlash memory components provide a new generation of forward-compatible software support built upon the Intel® FlashFile™ memory architecture. By using the Common Flash Interface (CFI) and the Scaleable Command Set (SCS), customers can take advantage of density upgrades and optimized write capabilities of future Intel StrataFlash memory devices.

Manufactured on the Intel® 0.4 micron ETOX V process technology, Intel StrataFlash memory provides the highest levels of quality and reliability.

The 5 Volt Series 200 Miniature Cards, based on the Miniature Card Implementers Forum (MCIF), employ 5 Volt Intel StrataFlash components to provide the ultimate in convenient, low-cost data storage for users of portable electronics systems. To meet the demanding requirements of diverse portable electronic system, these Miniature Cards are designed as small form factor removable media and are favored for their cost-effectiveness and reliability. Ideal platforms for the 5 Volt Series 200 include digital still cameras, audio recorders, smart cellular phones and hand-held PCs. Such applications require low-cost, consumer-friendly data storage media, as well as a convenient method to transport data to a PC for file manipulation and enhancement.

Host-based filing system software, such as Flash Translation Layer (FTL), eliminates the need for expensive card-based microcontrollers and ASICs. The 5 Volt Series 200 Flash Memory Miniature Cards enable the consumer to enjoy compatibility across a wide range of systems, allowing easy data exchange with MS-DOS* and Windows* 95-based PCs.

NOTE: This document formerly known as *Series 200 Flash Memory Miniature Card 4, 8, 16 Mbytes*.

December 1998 Order Number: 290620-005

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PRELIMINARY

REVISION HISTORY

Date of Revision	Version	Description
12/01/97	-001	Original version
03/16/98	-002	Updated front cover sheet highlights: write speed changed to 7 µs, erase cycles per block changed to 100,000 In Table 5, *Card Signal Values for the Card's Bus Operations and Modes*, changed conditions for Word Read, Word Write and Standby operations In first sentence of paragraph 4.1.3, *Standby*, re-defined standby mode entry conditions In Table 11, *CIS Memory Map*, removed CISTPL_DEVICE_OC row entry, "bumped-up" the address locations for the final 2 row entries of the table In paragraph 6.3, *CIS Data,* eliminated all references to 4 MB–200 ns, 8 MB–150 ns and 16 MB–150 ns card density-speed combinations and changed description entry for addresses 05H – 0DH from null to CISTPL_NULL (in bold font) In the last row (for I_{CCES}) of the DC Characteristics table of paragraph 7.4 changed CE_1# to CEL# and CE_2# to CEH# In note 1 of paragraph 7.5.2, *Write Operations*, restated the "CE# deasserted" conditions to be both CE#s (CEL# and CEH#) instead of either one of the CEs (CEL# or CEH#) In paragraph 7.6, *Block Erase, Write, and Lock-Bit Configuration Performance*, changed the "Typ" entries for first 3 parameters (pertaining to write time) to increase write times by 16.67%; added note 6 to describe expected write time performance relative to the specified maximum and typical values, and to suggest use of BUSY# to maximize system performance.
05/01/98	-003	Updated front cover sheet highlights: changed write speed to 6.3 µs
06/05/98	-004	Updated front cover sheet highlights: changed write speed to 12 µs In Paragraph 7.6 *Block Erase, Write, and Lock-Bit Configuration Performance,* changed typical values for the following parameters: Write Buffer Word Write Time, Word Write Time (Using Word Write Command), and Block Write Time (Using Write to Buffer Command)
12/21/98	-005	All densities of the 5 Volt Series 200 Miniature Card are now based on the 28F320J5. Specifications were changed accordingly. Name of document changed from *Series 200 Flash Memory Miniature Card 4, 8, 16, Mbyte.*

1.0 SCOPE OF DOCUMENT

This datasheet describes a 5 Volt Intel® StrataFlash™ memory card architecture, AC and DC characteristics and command definitions. Refer to Intel order number 290606 when ordering the datasheet.

2.0 PRODUCT OVERVIEW

The 4-, 8- and 16-Mbyte flash memory cards each contain a flash memory array made up of 5 Volt Intel StrataFlash memory components. The 4-Mbyte card consists of a single 4-Mbyte component (product number 28F320J5) configured for x 16 operation. Similarly, the 8-Mbyte card consists of two 4-Mbyte components (Intel® 28F320J5) configured for x16 operation. The 16-Mbyte card consists of four 4-Mbyte components which are configured for x16 operation. Intel StrataFlash memory can store more than one bit per flash memory cell, reducing the size and cost of large flash memory arrays. Figure 1 provides a generic block diagram which illustrates the card's functional layout and user interface.

A Command User Interface (CUI) serves as the interface between the system processor and internal operation of the card's memory device(s). A valid command sequence written to the CUI initiates device automation. An internal Write State Machine (WSM) automatically executes the algorithms and timings necessary for block erase, write, and lock-bit configuration operations.

Each Intel StrataFlash memory device incorporates a 16 word (32 byte) write buffer. This dramatically improves write performance by optimizing a flash memory device's programming algorithm, thereby freeing the CPU from writing data and polling status on a word-by-word basis. The 32-byte buffer can be loaded at full bus speed; then a single command can be issued to transfer the buffer into the flash memory array. While the Write State Machine (WSM) is handling all of the flash memory programming details for a memory write operation, the host CPU is free to perform other tasks.

The 4-, 8-, and 16-Mbyte cards contain, respectively, 32, 64, and 128 separate 128-Kbyte erase blocks. A block erase operation erases one of the 128-Kbyte blocks typically within one second—independent of other blocks. Each block can be independently erased 100,000 times. Block erase suspend mode allows system software to suspend block erase to read data from or write data to any other block.

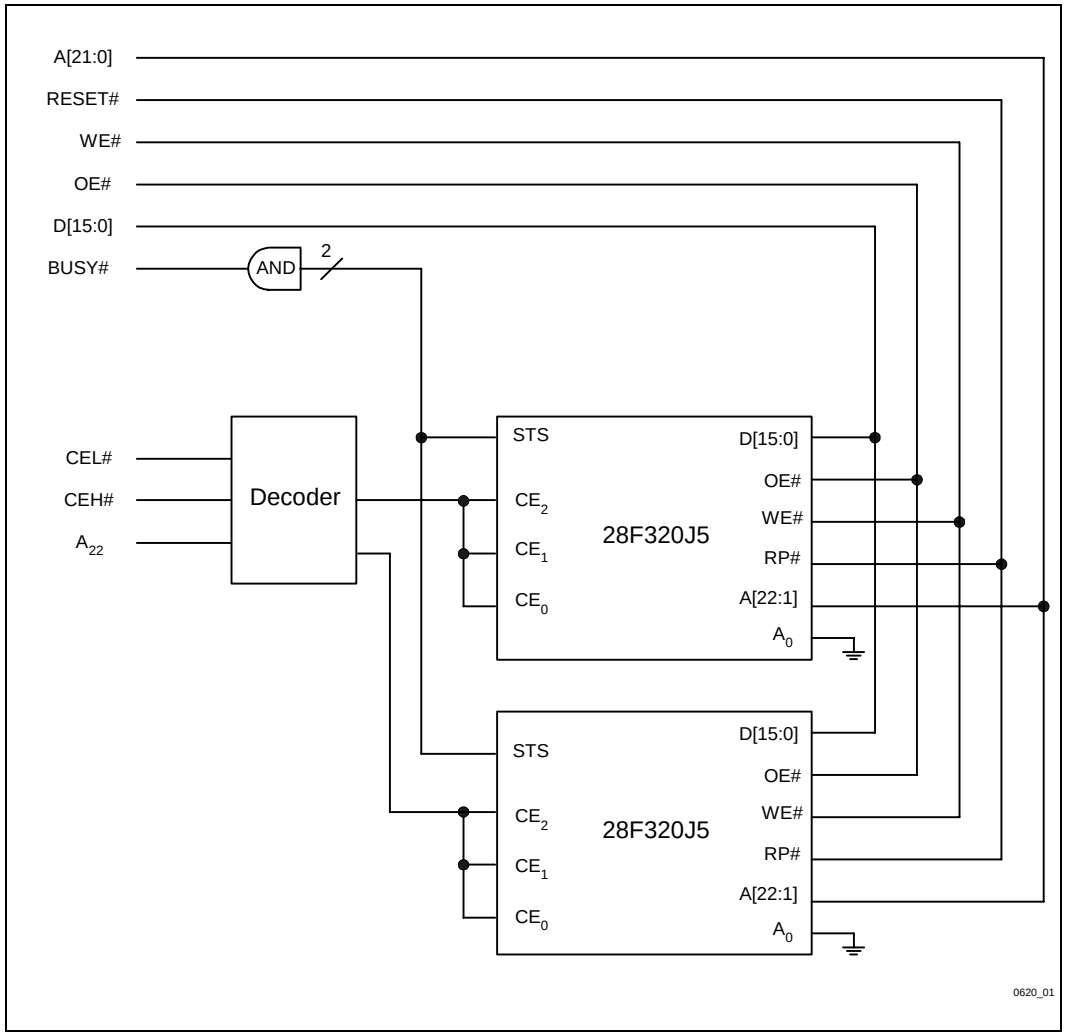


Figure 1. 8-Mbyte Flash Memory Card Block Diagram Showing Major Functional Elements

3.0 CARD ARCHITECTURE

The 5 Volt Series 200 Miniature Card implements the functionality of the Miniature Card Specification with X16 (word-wide) data transfers. The card does not support individual 8-bit (byte)—wide memory data transfers as the card's memory devices(s) and data bus interface are structured word-wide. The card ignores the Miniature Card interface signal BS#8 (for selecting between byte and word host data transfers) and assumes the BS#8 signal to be HIGH (for word access between the host and card).

Various information about the card is contained in an Attribute Information Structure (AIS) as defined in the PCMCIA Miniature Card Specification. The AIS is stored in Block 0 of the card's memory array. The high byte of the AIS is always FFH, the low byte contains the actual AIS data.

3.1 Card Signal Description

The signals for the 5 Volt Series 200 Miniature Card are listed in Table 1 and Table 2. They comply with the Miniature Card Specification. Table 3 and Table 4 describes the signals.

Table 1. 5 Volt Series 200 Flash Memory Miniature Card Interface Signals

Pad #	Signal Name	Pad #	Signal Name	Pad #	Signal Name
1	A_{18}	21	D_{12}	41	A_4
2	A_{16}	22	D_{10}	42	CEL#
3	A_{14}	23	D_9	43	A_1
4	V_{CCR}(1)	24	D_0	44	CASL#(1)
5	CEH#	25	D_2	45	CASH#(1)
6	A_{11}	26	D_4	46	CD#
7	A_9	27	RFU	47	A_{21}(4)
8	A_8	28	D_7	48	BUSY#
9	A_6	29	SDA(1)	49	WE#
10	A_5	30	SCL(1)	50	D_{14}
11	A_3	31	A_{19}	51	RFU(1,2)
12	A_2	32	A_{17}	52	D_{11}
13	A_0	33	A_{15}	53	VS2#(1)
14	RAS#(1)	34	A_{13}	54	D_8
15	A_{24}(1)	35	A_{12}	55	D_1
16	A_{23}(1)	36	RESET#	56	D_3
17	A_{22}(1)	37	A_{10}	57	D_5
18	OE#	38	VS1#	58	D_6
19	D_{15}	39	A_7	59	RFU(1,2)
20	D_{13}	40	BS8#(1)	60	A_{20}(3)

NOTES:

1. These signals make no internal connection into the card.
2. Reserved pins must not be driven by the host. They should be left floating.
3. A_{21} and A_{22} are not decoded on the 4-Mbyte card.
4. A_{22} is not decoded on the 8-Mbyte card.

Table 2. 5 Volt Series 200 Flash Memory Miniature Card Power/Insertion Signals

Signal #	Signal Name
61	GND
62	CINS#
63	V_{CC}

Table 3. 5 Volt Series 200 Flash Memory Miniature Card Interface Signal Description

Symbol	Type	Name and Function
A_0–A_{24}	INPUT	**ADDRESS INPUTS:** Addresses A_0 through A_{24} enable direct addressing of up to 64 MB of memory on the card. The memory will wrap at the card density boundary. The system should NOT try to access memory beyond the card's density, since the upper addresses are not decoded.
D_0–D_{15}	INPUT/ OUTPUT	**DATA INPUT/OUTPUT:** D_0 through D_{15} constitute the bi-directional data bus. D_{15} is the most significant bit.
CEL#, CEH#	INPUT	**CARD ENABLE LOW & HIGH:** CEL# enables accesses on the low byte of the data bus $D_{0–7}$. CEH# enables accesses on the high byte of the data bus $D_{8–15}$. Both CEL# and CEH# are active low signals. A host is expected to assert both CEL# and CEH# as the card's memory provides for word-wide data transfers but not byte-wide data transfers.
OE#	INPUT	**OUTPUT ENABLE:** Active low signal, enables read data from the memory card.
WE#	INPUT	**WRITE ENABLE:** Active low signal, enables write data to the memory card.
BUSY#	OUTPUT	**BUSY:** Active low signal, indicates the status of internally timed erase or write activities. A high output indicates the memory card is ready to accept another command.
CD#	OUTPUT	**CARD DETECT:** Active low signal, provides for card insertion detection. CD# connects to ground internally on the memory card, and will be forced low when the CD# interface signal connects to the host.
RESET#	INPUT	**RESET:** Active low input signal, resets the device's command user interface and places the card into a deep power-down mode. The host must drive this signal.
BS8#	INPUT	**8-BIT BUS WIDTH:** This signal is not connected on the 5 Volt Series 200 Miniature Card. The card assumes the Miniature Card Implementers Forum Specification's HIGH state definition of this signal to provide for only 16-bit data transfers between the host and card.
VS1#, VS2#	OUTPUT	**VOLTAGE SENSE:** Notifies the host socket of the card's V_{CC} requirements. VS_1 and VS_2 are both left **open** to indicate that the card only operates at 5 V.
RFU	—	**RESERVED FOR FUTURE USE**

Table 4. 5 Volt Series 200 Flash Memory Miniature Card Power/Insertion Signal Description

Symbol	Type	Name and Function
CINS#	OUTPUT	**CARD INSERTION DETECT:** This signal provides for early card insertion detection. CINS# connects to ground internally on the memory card, and will be forced low when the power/insertion signals connect to the host.
V_{CC}	-	**CARD POWER SUPPLY:** 5 V
GND	-	**GROUND**

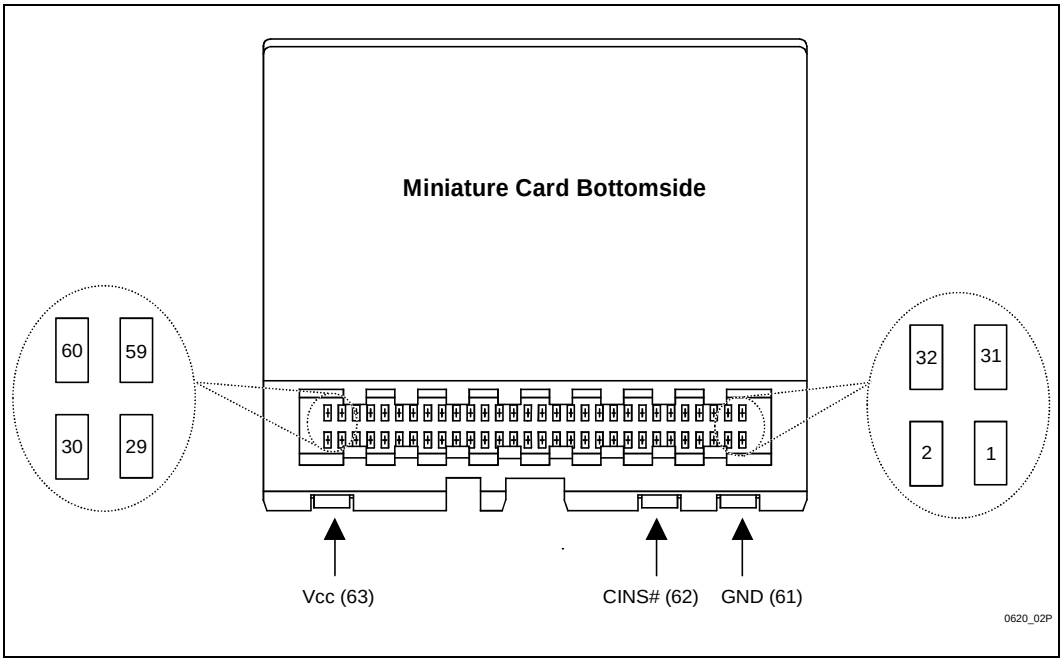


Figure 2. Card Interface Signal Assignment

4.0 MEMORY CONTROL LOGIC

4.1 Bus Operations

The host executes memory read, write and erase operations by issuing the appropriate command to the flash memory's Command User Interface (CUI). The CUI, which supports the command set of the card's memory devices, serves as the interface between the host processor and internal operation of a flash device. Commands can be issued to the CUI using standard microprocessor bus cycles.

Table 5 lists the Miniature Card's bus operations and modes. For each listed bus operation or mode the table defines the value of the card's relevant bus and control signals.

4.1.1 READ ARRAY

The host enables reads from the card by writing the appropriate read command to the CUI. The memory devices automatically reset to read array mode upon initial card power-up or after card reset. CEL#, CEH#, and OE# must be logically active to obtain 16 data bits at the outputs. The Card Enable (CEL# and CEH#) inputs together with the card's address inputs are used to select the addressed devices. Output Enable (OE#) is the data input/output (D_0–D_{15}) direction control, and when active, drives data from the selected memory onto the data bus. WE# must be driven to V_{IH} (inactive) during a read access.

4.1.2 OUTPUT DISABLE

With OE# at a logic-high level (V_{IH}), the device outputs are disabled. Outputs (D_0–D_{15}) are placed in a high-impedance state.

Table 5. Card Signal Values for the Card's Bus Operations and Modes

Bus Operation/Mode	RESET#	CEL#	CEH#	OE#	WE#	A_1	BS8#	$D_{8–15}$	$D_{0–7}$	Notes
Word Read	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	X	X	High	Low	1, 2, 4,
	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	X	X	High	Low	1, 2, 4, 5
	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	X	X	High	Low	1, 2, 4, 5
Word Write	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	X	X	High	Low	1, 2, 4
	V_{IH}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	X	X	High	Low	1, 2, 4, 6
	V_{IH}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	X	X	High	Low	1, 2, 4, 6
Manufacturer ID	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	X	00H	89H	
Device ID	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	00H	ID	3
Standby	V_{IH}	X	V_{IH}	X	X	X	X	High-Z	High-Z	
	V_{IH}	V_{IH}	X	X	X	X	X	High-Z	High-Z	
Output Disable	V_{IH}	X	X	V_{IH}	V_{IH}	X	X	High-Z	High-Z	
Reset/Power-Down	V_{IL}	X	X	X	X	X	X	High-Z	High-Z	

NOTES:

1. X can be V_{IL} or V_{IH} for control signals and address.
2. BUSY# is V_{OL} when the WSM is executing internal write or block erase algorithms. It is V_{OH} when the WSM is not busy, in erase suspend mode, or deep power-down mode.
3. The device code can be 14H, or 15H. Software should check for both cases for compatibility with future cards.
4. High indicates high byte data, low indicates low byte data.
5. Both memory bytes will be read from memory as the card's memory component data bus is word-wide and does not provide for individual byte access. The bus operation is non-compliant with the *PCMCIA PC Card Standard* as the *PC Card Standard* specifies a byte read operation instead of a word read operation for the listed signal conditions.
6. Both memory bytes will be written to memory as the card's memory component data bus is word-wide and does not provide for individual byte access. The bus operation is non-compliant with the *PCMCIA PC Card Standard* as the *PC Card Standard* specifies a byte write operation instead of a word write operation for the listed signal conditions. If a host system desires a byte write operation instead of a word write operation, then the host system must write V_{IH} to the unwanted active byte (which should be inactive according the *PC Card Standard*) in order to prevent the unwanted active byte from being written to card memory.

4.1.3 STANDBY

If both CEL# and CEH# are at a logic-high level (V_{IH}), the card enters standby mode. Standby operation disables much of the card's circuitry and substantially reduces device power consumption. The outputs (D_0–D_{15}) are placed in a high-impedance state independent of the status of OE#. If the host deselects the card during a write or erase, the card continues to function and consume normal active power until the operation completes.

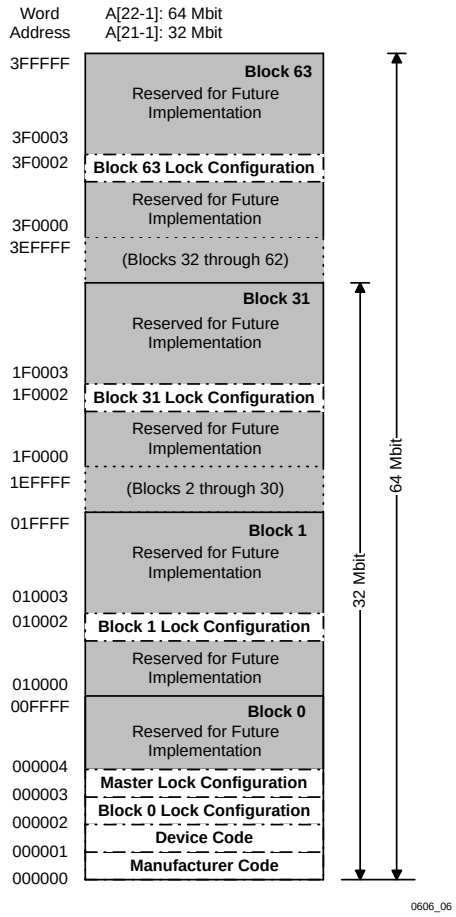
4.1.4 RESET/POWER-DOWN

RESET# at V_{IL} initiates the reset/power-down mode.

In read modes, RESET#-low deselects the card's memory, places output drivers in a high-impedance state, and turns off numerous internal memory circuits. RESET# must be held low for a minimum of t_w. Time t_{su} is required after return from reset mode until initial memory access outputs are valid. After this wake-up interval, normal operation is restored. The CUI is reset to read array mode and all memory device status registers are set to 80H.

During block erase, write, or lock-bit configuration modes, RESET#-low will abort the operation BUSY# transitions low and remains low for a maximum time of $t_w + t_{su}$ until the reset operation is complete. Memory contents being altered are no longer valid; the data may be partially corrupted after a write operation or partially altered after an erase or lock-bit configuration operation. Time t_{su} is required after RESET# goes to logic-high (V_{IH}) before another command can be written.

As with any automated device, it is important to assert RESET# during system reset. When the system comes out of reset, it expects to read data from the flash memory. Automated flash memories provide status information when accessed during block erase, write, or lock-bit configuration modes. If a CPU reset occurs with no flash memory reset, proper initialization may not occur because the flash memory may be providing status information instead of array data. Intel® Flash memories allow proper initialization following a system reset through the use of the RESET# input. In this application, RESET# is controlled by the same signal that resets the system CPU.



NOTES:

1. Data is always given on the low byte (upper byte contains 00h).
2. Memory shown is accessed by the Read Identifier Codes command only and is physically distinct from the card's flash memory array.
3. Master Lock function of the card's underlying memory devices is not a card function. The Master Lock Configuration information identified in the above memory map is shown only for the sake of consistency between the illustrated memory map and a corresponding memory map shown in the datasheet for the memory devices.

Figure 3. Device Identifier Code Memory Map

4.1.5 READ IDENTIFIER CODES

The read identifier codes operation outputs the manufacturer code, device code, block lock configuration codes for each block, and the master lock configuration code (see Figure 3) Using the manufacturer and device codes, the system CPU can automatically match the device with its proper algorithms. The block lock and master lock configuration codes identify locked and unlocked blocks and master lock-bit setting.

4.1.6 WRITE

Writing commands to the CUI enables reading of device data, query, identifier codes, inspection and clearing of the status register, as well as block erasure, writing of data and lock-bit configuration.

The Block Erase command requires appropriate command data and an address within the block to be erased. The Word Write command requires the command and address of the location to be written. The Write to Buffer command requires the command, starting address of the memory region to be written and the number of words to be written to the write buffer. Set Master and Block Lock-Bit commands require the command and address within the device (Master Lock) or block within the device (Block Lock) to be locked. The Clear Block Lock-Bits command requires the command and address within the device.

The CUI does not occupy an addressable memory location. It is part of each memory device and is written when the device is enabled and WE# is active. The address and data needed to execute a command are latched on the rising edge of WE# or the first edge of CEL# or CEH# that disables the device. Write cycle timing is specified in Section 9.2 (*Write Operations*).

4.2 Decode Logic

The card's decode logic enables the appropriate memory component during a read or write access of card memory. Unused upper addresses for the 5 Volt Series 200 Miniature Card will not be decoded. The address decoding will wrap around at the card's density.

5.0 COMMAND DEFINITION

The operations of the card's memory device(s) are selected by the writing of specific commands into the CUI. The 5 Volt Series 200 Miniature Card implements two command sets: the basic command set and the scaleable command set. The Basic Command Set is backward compatible with the Series 100 Miniature Card with the exception that write (program) suspend is not supported in the 5 Volt Series 200. The Scaleable Command Set adds three capabilities to the Miniature Card in addition to the Basic Command Set:

1. Common Flash Interface (CFI)
2. Buffered writes which employ a 32-byte write buffer to allow higher performance writes than available with the Basic Command Set; and
3. A configurable BUSY# output.

5.1 Basic Command Set

Table 6 presents the 5 Volt Series 200 Miniature Card's Basic Command Set. The table indicates that the commands require one or more bus cycles to implement. The table and notes following the table describe each bus cycle. Complete descriptions of the individual commands follow in subsections of the current document section.

5.1.1 READ ARRAY COMMAND

Upon initial device power-up and after exit from reset/power-down mode, the card's memory devices default to read array mode. This operation is also initiated by writing the Read Array command to a memory device. The device remains enabled for reads until another command is written. Once the internal WSM has started a block erase, write, or lock-bit configuration, the device will not recognize the Read Array command until the WSM completes its operation unless the WSM is suspended via an Erase Suspend command.

Table 6. Basic Command Set Definitions(9)

Command	Bus Cycles Req'd.	Notes	First Bus Cycle			Second Bus Cycle		
			Oper(1)	Addr(2)	Data(3,4)	Oper(1)	Addr(2)	Data(3,4)
Read Array	1		Write	X	XXFFH			
Read Identifier Codes	≥2	5	Write	X	XX90H	Read	IA	ID
Read Status Register	2		Write	X	XX70H	Read	X	SRD
Clear Status Register	1		Write	X	XX50H			
Word Write	2	6, 7	Write	X	XX40H or XX10H	Write	WA	WD
Block Erase	2	7	Write	X	XX20H	Write	BA	XXD0H
Block Erase Suspend	1	7	Write	X	XXB0H			
Block Erase Resume	1	7	Write	X	XXD0H			
Set Block Lock-Bit	2		Write	X	XX60H	Write	BA	XX01H
Clear Block Lock-Bits	2	8	Write	X	XX60H	Write	X	XXD0H

NOTES:

1. Card signal values for the identified bus operations are defined in Table 5.
2. X = Any valid address within the device.
   IA = Identifier Code Address:
   BA = Address within the block being erased or locked.
   WA = Address of memory location to be written.
3. SRD = Data read from Status Register.
   WD = Data to be written at location WA. Data is latched on the rising edge of WE#.
   ID = Data read from Identifier Codes.
4. The upper byte of the data bus during command writes is a "Don't Care" (X).
5. Following the Read Identifier Codes command, read operations access manufacturer, device, block lock, and master lock codes. See Read Identifier Section for read identifier code data.
6. Either XX40H or XX10H are recognized by the WSM as the word-write command setup.
7. The issue of a block erase or write-word command to a locked block will fail.
8. The clear block lock-bits operation simultaneously clears all block lock-bits.
9. Commands other than those shown above are reserved by Intel for future device implementations and should not be used.

5.1.2 READ IDENTIFIER CODES COMMAND

The identifier code operation is initiated by writing the Read Identifier Codes command to a memory device. Following the command write, read cycles from addresses shown in Figure 3 retrieve the manufacturer, device, block lock configuration and master lock configuration codes (see Table 7 for identifier code values). To terminate the operation, write another valid command. The Read Identifier Codes command is valid only when the WSM is off or the device is suspended. Following the Read Identifier Codes command, the following information can be read:

Table 7. Identifier Codes(1)

Code		Address(1)	Data
Manufacture Code		00000	(00) 89
Device Code	32-Mbit	00001	(00) 14
	64-Mbit	00001	(00) 15
Block Lock Configuration		X0002(2)	
• Block Is Unlocked			$DQ_0 = 0$
• Block Is Locked			$DQ_0 = 1$
• Reserved for Future Use			DQ_{1-7}
Master Lock Configuration(3)		00003	
• Device Is Unlocked			$DQ_0 = 0$
• Device Is Locked			$DQ_0 = 1$
• Reserved for Future Use			DQ_{1-7}

NOTES:

1. Data is always presented on the low byte (upper byte contains 00h).
2. X selects the specific block's lock configuration code. See Figure 3 for the device identifier code memory map.
3. See *5 Volt Intel® StrataFlash™ Memory; 28F320J5 and 28F640J5* datasheet for a description of Master Lock Configuration information. For 5 Volt Series 200 Miniature Cards the Master Lock Configuration byte should indicate that the device is unlocked ($DQ_0 = 0$).

5.1.3 READ STATUS REGISTER COMMAND

The status register may be read to determine when a block erase, write, or lock-bit configuration operation is complete and whether the operation completed successfully. Table 8 defines the content and format of the status register. The register may be read at any time by writing the Read Status Register command. After writing this command, all subsequent read operations output data from the status register until another valid command is written. The status register contents are latched on the falling edge of OE# or the first edge of CEL# and CEH# that enables the device (see Table 5, *Card Signal Values for the Card's Bus Operations and Modes*). OE# must toggle to V_{IH} or the device enter standby mode (Table 5) before further reads to update the status register latch.

During a word write, write to buffer, block erase, set lock-bit, or clear lock-bit command sequence, only SR.7 is valid until the Write State Machine completes or suspends the operation. Device I/O pins DQ_0–DQ_6 and DQ_8–DQ_{15} are placed in a high-impedance state. When the operation completes or suspends (check Status Register bit 7), all contents of the Status Register are valid when read.

5.1.4 CLEAR STATUS REGISTER COMMAND

Status register bits SR.5, SR.4, SR.3, and SR.1 are set to "1"s by the WSM and can only be reset by the Clear Status Register command. These bits indicate various failure conditions (see Table 8). By allowing system software to reset these bits, several operations (such as cumulatively erasing or locking of multiple blocks or writing of several bytes in sequence) may be performed. The status register may be polled to determine if an error occurred during the sequence.

To clear the status register, the Clear Status Register command (50H) is written. The Clear Status Register Command is only valid when the WSM is off or the device is suspended.

Table 8. Status Register Definitions(1)

WSMS	ESS	ECLBS	PSLBS	VPENS	R	DPS	R
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0

High Z When Busy?	Status Register Bits	NOTES:
No	SR.7 = WRITE STATE MACHINE STATUS 1 = Ready 0 = Busy	Check BUSY# or SR.7 to determine block erase, write (program), or lock-bit configuration completion. SR.6–SR.0 are not driven while SR.7 = "0."
Yes	SR.6 = ERASE SUSPEND STATUS 1 = Block Erase Suspended 0 = Block Erase in Progress/Completed	If both SR.5 and SR.4 are "1"s after a block erase or lock-bit configuration attempt, an improper command sequence was entered.
Yes	SR.5 = ERASE AND CLEAR LOCK-BITS STATUS 1 = Error in Block Erasure or Clear Lock-Bits 0 = Successful Block Erase or Clear Lock-Bits	SR.3 does not provide a continuous memory device (write) programming voltage level indication. The WSM interrogates and indicates the programming voltage level only after Block Erase, Word Write, Write to Buffer, Set Block/Master Lock-Bit, or Clear Block Lock-Bits command sequences.
Yes	SR.4 = WRITE AND SET LOCK-BIT STATUS 1 = Error in Write Operation or Set Master/Block Lock-Bit 0 = Successful Write Operation or Set Master/Block Lock Bit	SR.1 does not provide a continuous indication of master and block lock-bit values. The WSM interrogates the master lock-bit, block lock-bit, and RESET# (RP#) only after Block Erase, Write Word, Write to Buffer or Lock-Bit configuration command sequences. It informs the system, depending on the attempted operation, if the block lock-bit is set, master lock-bit is set, and/or RESET# (RP#) is not V_{HH}. Read the block lock and master lock configuration codes using the Read Identifier Codes command to determine master and block lock-bit status.
Yes	SR.3 = PROGRAMMING VOLTAGE STATUS 1 = Low Programming Voltage Detected, Write Operation Aborted 0 = Programming Voltage OK	
Yes	SR.2 = RESERVED FOR FUTURE ENHANCEMENTS	
Yes	SR.1 = DEVICE PROTECT STATUS 1 = Master Lock-Bit, Block Lock-Bit and/or RESET# (RP#) Lock Detected, Operation Abort 0 = Unlock	
Yes	SR.0 = RESERVED FOR FUTURE ENHANCEMENTS	SR.2 and SR.0 are reserved for future use and should be masked when polling the status register.

NOTE:

1. See the *5 Volt Intel® StrataFlash™ Memory; 28F320J5 and 28F640J5* datasheet (order number 290606) for a description of the Master Lock-bit. For 5 Volt Series 200 Miniature Cards, the Master Lock-bit should always be ="0" and should not interfere with any of the card's write or erase operations. The bit is referenced in the table for consistency of definition between the card and card memory device datasheets as the card status register information is actually provided by whatever memory device receives the Read Status Register command.

Table 9. eXtended Status Register Definitions

WBS	Reserved
bit 7	bits 6–0

High Z When Busy?	Status Register Bits	NOTES:
No	XSR.7 = WRITE BUFFER STATUS 1 = Write buffer available 0 = Write buffer not available	After a Buffer-Write command, XSR.7 = 1 indicates that a Write Buffer is available.
Yes	XSR.6–XSR.0 = RESERVED FOR FUTURE ENHANCEMENTS	SR.6–SR.0 are reserved for future use and should be masked when polling the status register.

5.1.5 BLOCK ERASE COMMAND

Erase is executed one block at a time and initiated by a two-cycle command. A block erase setup is first written, followed by an block erase confirm. This command sequence requires an appropriate address within the block to be erased (erase changes all block data to FFH). Block preconditioning, erase, and verify are handled internally by the WSM (invisible to the system). After the two-cycle block erase sequence is written, the device automatically outputs status register data when read. The CPU can detect block erase completion by analyzing the logic level of the STS pin or status register bit SR.7. Toggle OE#, CEL# or CEH# to update the status register.

When the block erase is complete, status register bit SR.5 should be checked. If a block erase error is detected, the status register should be cleared before system software attempts corrective actions. The CUI remains in read status register mode until a new command is issued.

This two-step command sequence of set-up followed by execution ensures that block contents are not accidentally erased. An invalid Block Erase command sequence will result in both status register bits SR.4 and SR.5 being set to “1.” Successful block erase requires that the corresponding block lock-bit be cleared. If block erase is attempted when the corresponding block lock-bit is set, SR.1 and SR.5 will be set to “1.”

5.1.6 BLOCK ERASE SUSPEND COMMAND

The Block Erase Suspend command allows block-erase interruption to read or write data in another block of memory. Once the block erase process starts, writing the Block Erase Suspend command requests that the WSM suspend the block erase sequence at a predetermined point in the algorithm. The device outputs status register data when read after the Block Erase Suspend command is written. Polling status register bit SR.7 then SR.6 can determine when the block erase operation has been suspended (both will be set to “1”). The BUSY# output will also transition to V_{OH}. Specification t_{WHRH} defines the block erase suspend latency.

At this point, a Read Array command can be written in order to read data from blocks other than that which is suspended. A word-write or write-to-buffer command sequence can also be issued during erase suspend to write data in other blocks. During a write operation with block erase suspended, status register bit SR.7 will return to “0” and the BUSY# output will transition to V_{OL}.

The only other valid commands while block erase is suspended are Read Query, Read Status Register, Clear Status Register, Configure, and Block Erase Resume. After a Block Erase Resume command is written to the flash memory, the WSM will continue the block erase process. Status register bits SR.6 and SR.7 will automatically clear and the BUSY# output will return to V_{OL}. After the Erase Resume command is written, the device automatically outputs status register data when read. Block erase cannot resume until write operations initiated during block erase suspend have completed.

5.1.7 WORD-WRITE COMMAND

Word-Write commands are executed in a two-cycle command sequence. Word-Write command setup (standard 40H or alternate 10H) is written in the first cycle and then followed in the next cycle by a second write that specifies the address and data (latched on the rising edge of WE#) to be written in memory. The WSM then takes over, controlling the word-write and Word-Write verify algorithms internally. After the word-write command sequence is written, the device automatically outputs status register data when read. The CPU can detect the completion of the write event by analyzing the logic state of the BUSY# output or status register bit SR.7.

When the word-write operation is complete, status register bit SR.4 should be checked. If a write error is detected, the status register should be cleared. The internal WSM verify only detects errors for “1”s that do not successfully program to “0”s. The CUI remains in read status register mode until it receives another command.

Successful write operations require that the corresponding block lock-bit be cleared. If a word write operation is attempted when the corresponding block lock-bit is set, SR.1 and SR.4 will be set to “1.”

5.1.8 SET BLOCK LOCK-BIT COMMAND

A flexible block locking and unlocking scheme is enabled via a combination of block lock-bits. The block lock-bits gate memory write and erase operations. Individual block lock-bits can be set using the Set Block Lock-Bit command. Set Block Lock-Bit commands are invalid while the WSM is running or the device is suspended.

Set block lock-bit commands are executed by a two-cycle sequence. The set block lock-bit setup along with appropriate block or device address is written followed by either the set block lock-bit confirm (and an address within the block to be locked). The WSM then controls the set lock-bit algorithm. After the sequence is written, the device automatically outputs status register data when read. The CPU can detect the completion of the set lock-bit event by analyzing the logic state of the BUSY# pin output or status register bit SR.7.

When the set lock-bit operation is complete, status register bit SR.4 should be checked. If an error is detected, the status register should be cleared. The CUI will remain in read status register mode until a new command is issued.

This two-step sequence of set-up followed by execution ensures that lock-bits are not accidentally set. An invalid Set Block Lock-Bit command will result in status register bits SR.4 and SR.5 being set to “1.”

5.1.9 CLEAR BLOCK LOCK-BITS COMMAND

All set block lock-bits are cleared in parallel via the Clear Block Lock-Bits command. This command is invalid while the WSM is running or the device is suspended.

Clear block lock-bits command is executed by a two-cycle sequence. A clear block lock-bits setup is first written followed by the clear block lock-bits confirm. The device automatically outputs status register data when read. The CPU can detect completion of the clear block lock-bits event by analyzing the logic state of the BUSY# pin output or status register bit SR.7.

When the operation is complete, status register bit SR.5 should be checked. If a clear block lock-bit error is detected, the status register should be cleared. The CUI will remain in read status register mode until another command is issued.

This two-step sequence of set-up followed by execution ensures that block lock-bits are not accidentally cleared. An invalid Clear Block Lock-Bits command sequence will result in status register bits SR.4 and SR.5 being set to “1.”

If a clear block lock-bits operation is aborted due to V_{CC} transitioning out of valid range or RESET# active transition, block lock-bit values are left in an undetermined state. A repeat of the Clear Block Lock-Bits command is then required to initialize block lock-bit contents to known values.

5.2 Scaleable Command Set

Table 10 presents the 5 Volt Series 200 Miniature Card’s Scaleable Command Set. The table indicates that the commands require one or more bus cycles to implement. The table and notes following the table describe each bus cycle. Complete descriptions of the individual commands follow in subsections of the current document section.

Table 10. Scaleable Command Set Definitions(10)

Command	Bus Cycles Req'd.	Notes	First Bus Cycle			Second Bus Cycle		
			Oper(1)	Addr(2)	Data(3,4)	Oper(1)	Addr(2)	Data(3,4)
Read Query	≥ 2		Write	X	XX98H	Read	QA	QD
Write to Buffer	> 2	5, 6, 7, 8, 9	Write	BA	XXE8H	Write	BA	N
— Confirm	1	6, 7	Write	X	XXD0H			
Configuration		9						

NOTES:

1. Card signal values for the identified bus operations are defined in Table 5, *Signal Values for the Card's Bus Operations and Modes*.
2. X = Any valid address within the device.
   QA = QUERY database Address.
   BA = Block Address.
3. QD = Data read from QUERY database.
   CC = Configuration Code.
4. The upper byte of the data bus during command writes is a "Don't Care."
5. After the first bus cycle of the Write to Buffer command, check the Extended Status Register to make sure the write buffer is available for writing. If the buffer is available for writing, proceed with the second bus cycle; otherwise, continue repeating the first bus cycle and checking the Extended Status Register in turn until the buffer becomes available; when the buffer becomes available, proceed with the second bus cycle of the Write to Buffer command.
6. The number of words to be written to the Write Buffer = N + 1, where N = word count argument. The word count range on this device is N = 0000H to N = 000FH. Writing a word count outside the buffer boundary causes unexpected results and should be avoided.

   The third and consecutive bus cycles of a Write to Buffer command sequence, as determined by N, are for writing data into the Write Buffer. In the third bus cycle a device start address is given along with the write buffer data. Subsequent write cycles provide additional device addresses and data. All subsequent addresses must lie within the start address plus the count. The Confirm command (XXD0H) is expected after exactly N + 1 write cycles; any other command at that point in the sequence aborts the write to buffer operation. Please see the *5 Volt Intel® StrataFlash™ Memory; 28F320J5 and 28F640J5* datasheet for additional information on the Write to Buffer command.
7. The Write Buffer operation does not begin until a Confirm command is issued.
8. The issue of a Write to Buffer command to a locked block will fail.
9. The Configuration Command is not supported on the 5 Volt Series 200 Miniature Card. The Configuration Command serves to program the configurable status output (STS output pin) of a memory device. To satisfy the Miniature Card Implementers Forum Specification the STS output pin for all card memory devices must be configured as a RY/BY# pin to generate the card's BUSY# output signal. At card power-up the STS output for all devices defaults to RY/BY# pin operation; thereafter, host software shall not issue the Configuration Command.
10. Commands other than those shown above are reserved for future use and should not be used.

5.2.1 BLOCK WRITE COMMAND

To write to the flash device write buffer, a Write to Buffer command sequence is initiated. A variable number of bytes, up to the buffer size, can be loaded into the buffer and written to the Flash device. First, the Write to Buffer setup command is issued along with the Block Address of the memory device erase block to which the buffer content will be written. At this point, the eXtended Status Register information (reference Table 9) is loaded into the register and XSR.7 reverts to reflecting "buffer available" status. Whenever the memory device is read immediately after receiving a Write to Buffer command, the eXtended Status Register content will be presented by the memory. If XSR.7=0, the write buffer is not available for writing. When XSR.7 = “1,” the memory device will allow data to be written to the write buffer. To determine when the write buffer can be written, continue to monitor XSR.7 until XSR.7=1 by repeating the sequence of first issuing the Write to Buffer setup command along with the appropriate Block Address, and then reading the eXtended Status Register.

When the write buffer becomes available for writing, a word count (N) is given to the memory device with the Block Address of the memory device erase block to which the buffer content will be written. On the next write, a device start address is given along with the write buffer data. For maximum programming performance and lower power, align the start address at the beginning of a Write Buffer boundary. Subsequent writes provide additional device addresses and data. All subsequent addresses must lie within the start address plus the count.

After the final buffer data is given, a Write Confirm command is issued. This initiates the WSM (Write State Machine) to begin copying the buffer data to the flash memory. If a command other than Write Confirm is written to the device, an “Invalid Command/Sequence” error will be generated and Status Register bits SR.5 and SR.4 will be set to a “1.” For additional buffer writes, issue another Write to Buffer setup command and check XSR.7. The write buffers can be loaded while the WSM is busy as long as XSR.7 indicates that a buffer is available.

If an error occurs while a device is writing data to memory, the device will stop writing, and status register bit SR.4 will be set to a “1” to indicate a write operation failure. Any time a media failure occurs during a write or an erase (for which SR.4 or SR.5 is set, respectively), the device will not except any more buffered write commands. Additionally, if the user attempts to write past an erase block boundary with a Write to Buffer command, the device will abort the write. This will generate an “Invalid Command/Sequence” error (“botch”) and Status Register bits SR.5 and SR.4 will be set to a “1.” To clear SR.4 and/or SR.5 issue a Clear Status Register command.

Successful writing to an erase block requires that the block’s associated Block Lock-Bit bit be reset. If the Block Lock-Bit is set, the erase block is locked. A Write to Buffer command which attempts to write data to the locked block will fail and result in SR.1 and SR.4 being set to “1.”

5.2.2 CONFIGURATION COMMAND

The Configuration Command is not supported on the 5 Volt Series 200 Miniature Card. The Configuration Command serves to program the configurable status output (STS output pin) of a memory device. To satisfy the PCMCIA Miniature Card Specification the STS output pin for all card memory devices must be configured as a RY/BY# pin to generate the card’s BUSY# output signal. At card power-up the STS output for all devices defaults to RY/BY# pin operation; thereafter, host software shall not issue the Configuration Command.

5.2.3 READ QUERY COMMAND

The SCS (Scaleable Command Set) Read Query command causes the flash component to output the Common Flash Interface (CFI) Query structure or “database” information. The Common Flash Interface provides a standard means for a flash memory to tell a host system about the memory's architecture, algorithms and characteristics. See *AP-646 Common Flash Interface (CFI) and Command Sets* (order number 292204) for a full description of CFI.

Writing the Read Query command to the memory puts it in Read Query mode. While in read query mode, the memory responds to read bus operations with data from a ROM instead of data from the flash array data. The data in the ROM describes the memory component to which the Ready Query command is addressed.

As the definition of CFI data presented by a card memory device is quite extensive, the definition is not repeated as part of the current document. Refer to the *5 Volt Intel® StrataFlash™ Memory; 28F320J5 and 28F640J5* datasheet for a complete definition of the card memory's CFI data and the Read Query command by which the data is accessed.

6.0 CARD ATTRIBUTE INFORMATION

The Card Attribute Information consists of a Miniature Card Attribute Information Structure (AIS) in accordance with the Miniature Card Implementers Forum as well as a Card Information Structure (CIS) in compliance with the PCMCIA PC Card Specification. These two structures co-exist for compatibility with both industry standards. This allows the 5 Volt Series 200 Miniature Card to function in both PC Card and Miniature Card environments.

The Card Attribute Information data for the 5 Volt Series 200 Miniature Card is found in Section 6.3. For more information on the description of these structures refer to the appropriate specification.

CAUTION:

The Card Attribute Information data is located in Block 0. This information is not write protected and should not be erased by the system software if this information is needed for card recognition.

6.1 Card Information Structure

The CIS begins at address 0000H (device tuple) of the card's memory. The CIS data resides only in the low byte of the word. It contains a variable length chain of data blocks (tuples) that conform to a basic format. See Table 11 for the CIS memory map.

6.2 Attribute Information Structure

The AIS begins at address 0010H (identifier byte) of the card's memory. The AIS data resides only in the low byte of the word. It contains a fixed list of data information that ends at address 00FFH. See Table 12 for the AIS memory map.

NOTE:

All addresses listed in Table 11 and Table 12 are **WORD** addresses.

Table 11. CIS Memory Map

Tuple Name	Description	Tuple Code	Address Location
CISTPL_DEVICE	Device Information	01H	0H - 04H
CISTPL_NULL	Null (Ignore)	00H	05H - 0DH
CISTPL_MINI	Miniature Card AIS (Vendor Unique)	80H	0EH - FFH
CISTPL_DEVICEGEO	Device Geometry Information	1EH	100H - 107H
CISTPL_MANFID	Manufacturer Identification String	20H	108H - 10DH
CISTPL_FUNCID	Function Class Identification	21H	10EH - 111H
CISTPL_LONGLINK_C	Longlink to Common Memory	12H	112H - 117H
CISTPL_VERS_1	Level 1 Version/Product Information	15H	118H - 167H
CISTPL_JEDEC_C	JEDEC ID	18H	168H - 16BH
CISTPL_END	The End-of-Chain Tuple	FFH	16CH - 16DH

Table 12. AIS Memory Map

AIS Section	Description	Address Location
Identification Data	Identifies Card Type	10H - 3FH
Compatibility Data	Describes Attributes of Card	40H - 4FH
Not Used	Reserved for Future Use	50H - FFH

6.3 CIS Data

CIS data is located in memory and describes the 5 Volt Series 200 Miniature Card as follows:

Address	Values	Description
00H	01H	**CISTPL_DEVICE**
01H	03H	TPL_LINK
02H	53H	FLASH = 150 ns
	52H	FLASH = 200 ns
03H	0EH	CARD SIZE: 4 MB
	1EH	CARD SIZE: 8 MB
	3EH	CARD SIZE: 16 MB
04H	FFH	END OF DEVICE
05H - 0DH	00H	**CISTPL_NULL**
0EH	80H	**CISTPL_MIN**
0FH	F0H	TPL_LINK
10H	99H	Identifier
11H	10H	Rev 1.0 Compliant
12H	65H	4-MB,150 ns AIS Checksum
	5BH	8-MB, 200 ns AIS Checksum
	52H	16-MB, 200 ns AIS Checksum
13H	49H	Manufacturer Name I
14H	4EH	N
15H	54H	T
16H	45H	E

Address	Values	Description
17H	4CH	L
18H	20H	SPACE
19H	43H	C
1AH	4FH	O
1BH	52H	R
1CH	50H	P
1DH	4FH	O
1EH	52H	R
1FH	41H	A
20H	54H	T
21H	49H	I
22H	4FH	O
23H	4EH	N
24H - 26H	00H	NULL
27H	53H	Card Name S
28H	45H	E
29H	52H	R
2AH	49H	I
2BH	45H	E
2CH	53H	S
2DH	20H	SPACE
2EH	32H	2

Address	Values	Description
2FH	30H	0
30H	30H	0
31H	20H	SPACE
32H	43H	C
33H	41H	A
34H	52H	R
35H	44H	D
36H - 3AH	00H	NULL
3BH	01H	1 Technology Device
3CH - 3FH	00H	Reserved Space Set to 00H
40H	00H	Flash
41H	89H	Device JEDEC Manufacturer ID
42H	14H	4-MB Device Component JEDEC ID
	15H	8-MB Device Component JEDEC ID
	15H	16-MB Device Component JEDEC ID
43H	03H	4 MB
	07H	8 MB
	0FH	16 MB
44H	00H	no x.x V Accesses
45H	00H	no 3.3 V Access Time
46H	0FH	150 ns 5.0 V Access Time
	14H	200 ns 5.0 V Access Time
47H	00H	no x.x V Accesses
48H	00H	no 3.3 V Accesses
49H	47H	40 mA read/70 mA write @ 5.0 V

Address	Values	Description
4AH	01H	100 µA standby - 4 MB
	01H	180 µA standby - 8 MB
	02H	340 µA standby - 16 MB
4BH - 4FH	00H	Reserved
50H - FFH	00H	NULL / Not Used
100H	1EH	**CISTPL_DEVICEGEO**
101H	06H	TPL_LINK
102H	02H	DGTPL_BUS
103H	11H	DGTPL_EBS
104H	01H	DGTPL_RBS
105H	01H	DGTPL_WBS
106H	01H	DGTPL_PART = 1
107H	01H	FLASH DEVICE INTERLEAVE
108H	20H	**CISTPL_MANFID**
109H	04H	TPL_LINK
10AH	89H	TPLMID_MANF: LSB (INTEL JEDEC ID)
10BH	00H	TPLMID_MANF: MSB
10CH	12H	4 MB - 150 ns
	21H	8 MB - 200 ns
	31H	16 MB - 200 ns
10DH	86H	TPLMID_CARD MSB Value Series 200 Card
10EH	21H	**CISTPL_FUNCID**
10FH	02H	TPL_LINK
110H	01H	TPLFID_FUNCTION : Memory
111H	00H	TPLFID_SYSINIT
112H	12H	**CISTPL_LONGLINK_C**
113H	04H	TPL_LINK

Address	Values	Description
114H	00H	LOWEST BYTE
115H	00H	MID BYTE
116H	02H	MID BYTE
117H	00H	HIGHEST BYTE
118H	15H	**CISTPL_VERS1**
119H	4EH	TPL_LINK
11AH	05H	TPLLV1_MAJOR
11BH	00H	TPLLV1_MINOR
11CH	49H	TPLLV1_INFO I
11DH	6EH	n
11EH	74H	t
11FH	65H	e
120H	6CH	l
121H	00H	END TEXT
122H	53H	S
123H	45H	E
124H	52H	R
125H	49H	I
126H	45H	E
127H	53H	S
128H	20H	SPACE
129H	32H	2
12AH	30H	0
12BH	30H	0
12CH	20H	SPACE
12DH	46H	F
12EH	4CH	L
12FH	41H	A
130H	53H	S
131H	48H	H

Address	Values	Description
132H	20H	SPACE
133H	4DH	M
134H	49H	I
135H	4EH	N
136H	49H	I
137H	41H	A
138H	54H	T
139H	55H	U
13AH	52H	R
13BH	45H	E
13CH	20H	SPACE
13DH	43H	C
13EH	41H	A
13FH	52H	R
140H	44H	D
141H	00H	END TEXT
142H	30H	4 MB
	30H	8 MB
	31H	16 MB
143H	34H	4 MB
	38H	8 MB
	36H	16 MB
144H	20H	SPACE
145H	00H	END TEXT
146H	43H	C
147H	4FH	O
148H	50H	P
149H	59H	Y
14AH	52H	R
14BH	49H	I
14CH	47H	G

Address	Values	Description
14DH	48H	H
14EH	54H	T
14FH	20H	SPACE
150H	49H	I
151H	4EH	N
152H	54H	T
153H	45H	E
154H	4CH	L
155H	20H	SPACE
156H	43H	C
157H	4FH	O
158H	52H	R
159H	50H	P
15AH	4FH	O
15BH	52H	R
15CH	41H	A
15DH	54H	T
15EH	49H	I
15FH	4FH	O
160H	4EH	N
161H	20H	SPACE

Address	Values	Description
162H	31H	1
163H	39H	9
164H	39H	9
165H	37H	7
166H	00H	END TEXT
167H	FFH	END OF LIST
168H	18H	**CISTPL_JEDEC_C**
169H	02H	TPL_LINK
16AH	89H	MANUFACTURER ID
16BH	14H	4 MB Card Device Component JEDEC ID
	15H	8 MB Card Device Component JEDEC ID
	15H	16 MB Card Device Component JEDEC ID
16CH	FFH	**CISTPL_END**
16DH	00H	INVALID ADDRESS

7.0 ELECTRICAL SPECIFICATIONS

NOTICE: This datasheet contains preliminary information on new products in production. Do not finalize a design with this information. Revised information will be published when the product is available. Verify with your local Intel Sales office that you have the latest datasheet before finalizing a design.

7.1 Absolute Maximum Ratings*

Commercial Operating Temperature

During Read, Block Erase, Write, and Lock-Bit Configuration . –20 °C to +70 °C(1)
Temperature under Bias ..... –10 °C to +80 °C

Storage Temperature..... –65 °C to +125 °C

Voltage on Any Pin ..... –2.0 V to +7.0 V(2)

Output Short Circuit Current.....100 mA(3)

** WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may effect device reliability.*

NOTES:

1. Operating temperature is for commercial product defined by this specification.
2. All specified voltages are with respect to GND. Minimum DC voltage is –0.5 V on input/output pins and –0.2 V on V_{CC} pin. During transitions, this level may undershoot to –2.0 V for periods <20 ns. Maximum DC voltage on input/output pins and V_{CC} is V_{CC} +0.5 V which, during transitions, may overshoot to V_{CC} +2.0 V for periods <20 ns.
3. Output shorted for no more than one second. No more than one output shorted at a time.

7.2 Operating Conditions

Temperature and V_{CC} Operating Conditions

Symbol	Parameter	Notes	Min	Max	Unit	Test Condition
T_A	Operating Temperature		–20	+70	°C	Ambient Temperature
V_{CC}	V_{CC} Supply Voltage (5 V ± 5%)		4.75	5.25	V	

7.3 Capacitance(1)

T_A = +25 °C, f = 1 MHz

Symbol	Parameter	Typ	Max	Unit	Condition
C_{IN}	Input Capacitance	6	8	pF	V_{IN} = 0.0 V
C_{OUT}	Output Capacitance	8	12	pF	V_{OUT} = 0.0 V

NOTE:

1. Sampled, not 100% tested.

7.4 DC Characteristics

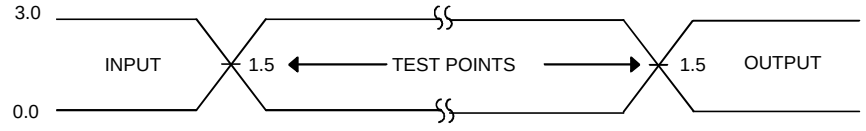
Sym	Parameter	Notes	Typ	Max	Unit	Test Conditions
I_{LI}	Input Load Current	1,4		20	µA	$V_{CC} = V_{CC}$ Max, $V_{IN} = V_{CC}$ or GND
I_{LO}	Output Leakage Current	1		20	µA	$V_{CC} = V_{CC}$ Max, $V_{IN} = V_{CC}$ or GND
I_{CCS}	V_{CC} Standby Current				µA	$V_{CC} = V_{CC}$ Max
	• 4-Mbyte Card	1,3	100	170		CEL# = CEH# = RESET# = V_{CC} ± 0.2 V
	• 8-Mbyte Card	1,3	180	320		
	• 16-Mbyte Card	1,3	340	620		
I_{CCD}	V_{CC} Deep Power-Down Current				µA	RESET#, GND ± 0.2V I_{OUT} (RESET) = 0 mA
	• 4-Mbyte Card	1,3	100	145		
	• 8-Mbyte Card	1,3	180	270		
	• 16-Mbyte Card	1,3	340	520		
I_{CCR}	V_{CC} Read Current	1	35	55	mA	$V_{CC} = V_{CC}$ Max, CEL#/CEH# = GND, f = 5 MHz, I_{OUT} = 0 mA
I_{CCW}	V_{CC} Word Write or Set Lock-Bit Current	1,3	35	60	mA	CMOS Inputs
I_{CCE}	V_{CC} Block Erase or Clear Lock-Bits Current	1,3	35	70	mA	CMOS Inputs
I_{CCES}	V_{CC} Block Erase Suspend Current	1,2		10	mA	CEL# = CEH# = V_{IH}

NOTES:

1. All currents are in RMS unless otherwise noted. These currents are valid for all product versions (speeds). Contact Intel's Application Support Hotline or your local sales office for information about typical specifications.
2. I_{CCES} is specified with the card's memory de-selected. If read or word write occurs while in erase suspend mode, the card's current draw is the sum of I_{CCES} and either I_{CCR} (read) or I_{CCW} (write).
3. CMOS inputs are either V_{CC} ± 0.2 V or GND ± 0.2 V.
4. Exceptions: With V_{IN} = GND, the leakage current on CEL#, CEH# will be < 50 µA each due to internal pull-up resistors.

7.4 DC Characteristics (Continued)

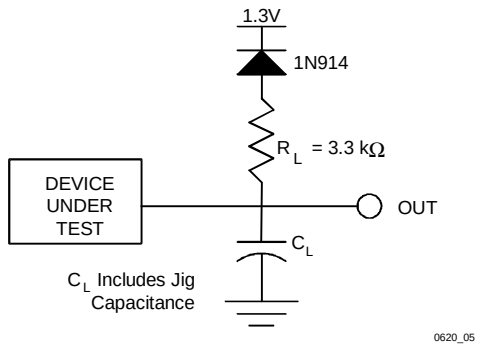
Sym	Parameter	Notes	Min	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage		–0.5	0.8	V	
V_{IH}	Input High Voltage		0.7 V_{CC}	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage			0.1 V_{CC}	V	V_{CC} = V_{CC} Min I_{OL} = 4.0 mA
V_{OH}	Output High Voltage		0.9 V_{CC}		V	V_{CC} = V_{CC} Min I_{OH} = –1 mA
V_{LKO}	V_{CC} Lockout Voltage		0.7 V_{CC}		V	



NOTE:

1. AC test inputs are driven at 3.0 V for a Logic "1" and 0.0 V for a Logic "0". Input timing begins, and output timing ends, at 1.5 V. Input rise and fall times (10% to 90%) < 10 ns.

Figure 4. Transient Input/Output Reference Waveform for V_{CC} = 5 V ± 5% (Standard Testing Configuration)



NOTE:
C_L Includes Jig Capacitance

Figure 5. Transient Equivalent Testing Load Circuit

Test Configuration Capacitance Loading Value

Test Configuration	C_L (pF)
V_{CC} = 5.0 V ± 5%	100

7.5 AC Characteristics

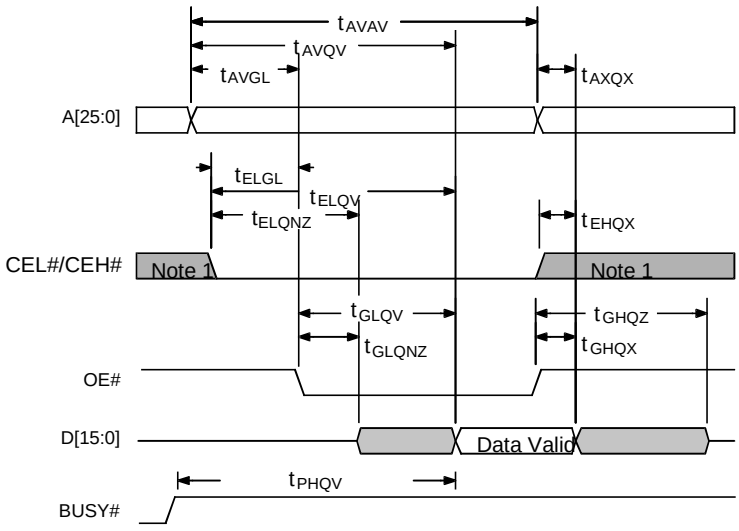
AC timing diagrams and characteristics are designed to meet or exceed the Miniature Card Specification.

7.5.1 READ OPERATIONS

IEEE Symbol	Parameter	4-, 8-, 16-MB Cards		Unit
		Min	Max	
t_{AVAV}	Read Cycle Time	150		ns
t_{AVQV}	Address Access Time		150	ns
t_{ELQV}	CE# Access Time		150	ns
t_{GLQV}	OE# Access Time		75	ns
t_{GHQZ}	Output Disable Time from OE# Inactive		75	ns
t_{GLQNZ}	Output Enable Time from OE# Active(1)	5		ns
t_{ELQNZ}	Output Enable Time from CE# Active(1)	5		ns
t_{AXQX}	Data Hold from Address, CE#, or OE# Change (Whichever Occurs First)	0		ns
t_{ELGL}	CE# Setup Time to OE# Active	0		ns
t_{AVGL}	Address Setup Time to OE# Active	20		ns
t_{PHQV}	BUSY# High to Output Delay		180	ns

NOTE:

1. Sampled, not 100% tested.



NOTE:
1. The filled area may be either high or low.

Figure 6. AC Waveforms for Read Operations

7.5.2 WRITE OPERATIONS

IEEE Symbol	Parameter	4-, 8-,16-MB Cards		Unit
		Min	Max	
t_{AVAV}	Write Cycle Time	150		ns
t_{WLWH}	WE# Pulse Width	80		ns
t_{AVWL}	Address Setup Time to WE# Active	20		ns
t_{DVWH}	Data Setup Time to WE# Inactive	50		ns
t_{WHDX}	Data Hold Time from WE# Inactive	20		ns
t_{WHAX}	Address Hold Time from WE# Inactive	10		ns
t_{WHEH}	CE# Hold Time from WE# Inactive	10		ns
t_{ELWL}	CE# Setup Time to WE# Active(1)	0		ns
t_{EHWL}	CE# Inactive Time to WE# Active(1)	35		ns
t_{WHWL}	WE# Inactive Time to WE# Active	30		ns
t_{WHRL}	WE# (CE#) Inactive Time to BUSY# Active		90	ns

NOTE:

1. These timings apply only if both CE#s (CEL# and CEH#) are deasserted prior to WE# asserted.

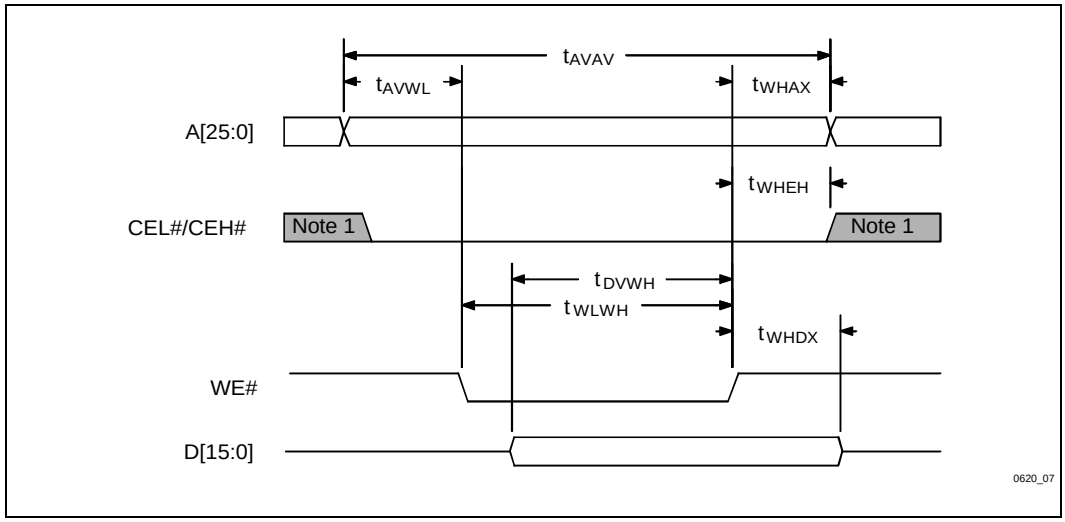


Figure 7. AC Waveforms for Write Operations

7.5.3 POWER-UP TIMING

Symbol	Parameter	Notes	Min	Max	Units
t_{su} (CEL#/CEH#)	CE# Setup Time		1		ms
t_{su} (RESET#)	RESET# Setup Time		1		ms
t_{pr}	V_{CC} Rising Time	1	0.1	100	ms
t_w (RESET#)	RESET# Width	2	36		µs

NOTES:

1. The t_{pr} is defined as a "linear waveform" in the period of 10% to 90%. Even if the waveform is not a "linear waveform," its rising time must meet this specification.
2. If RESET# is asserted while a block erase, write, or lock-bit configuration operation is not executing, then the minimum required RESET# Pulse Low Time is 1 µs.
3. A reset time, t_{PHQV} (reference Section 8.4.1), is required from BUSY# or RESET# going high until outputs are valid.

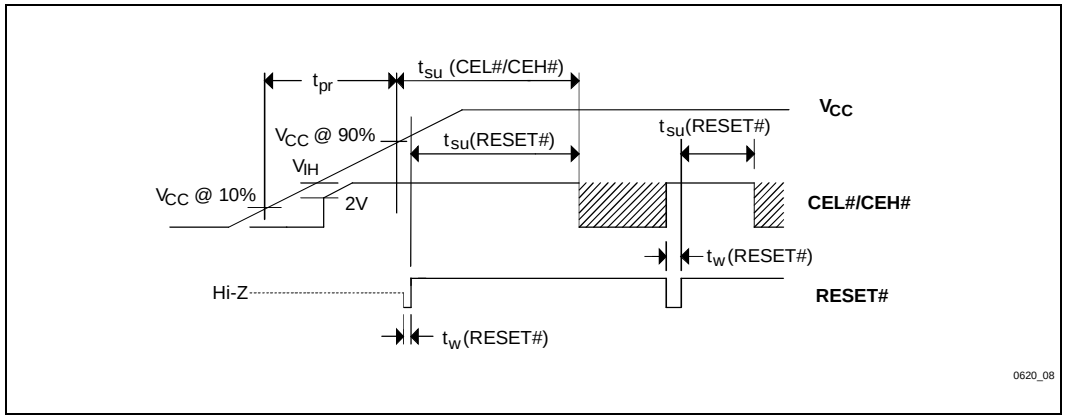


Figure 8. Power-Up Timing for Systems Supporting RESET#

7.6 Block Erase, Write, and Lock-Bit Configuration Performance(3,4)

Sym	Parameter	Notes	Min	Typ(1)	Max	Unit
t_{WHQV1} t_{EHQV1}	Write Buffer Word Write Time	2,5,6	TBD	12	TBD	µs
t_{WHQV2} t_{EHQV2}	Word Write Time (Using Word Write Command)	2,6	TBD	180	TBD	µs
—	Block Write Time (Using Write to Buffer Command)	2,6	TBD	1.6	TBD	sec
t_{WHQV4} t_{EHQV4}	Block Erase Time	2	TBD	0.7	TBD	sec
t_{WHQV5} t_{EHQV5}	Set Lock-Bit Time	2	TBD	32	TBD	µs
t_{WHQV6} t_{EHQV6}	Clear Block Lock-Bits Time	2	TBD	0.3	TBD	sec
t_{WHRH} t_{EHRH}	Erase Suspend Latency Time to Read			25	TBD	µs

NOTES:

1. Typical values measured at T_A = +25 °C and nominal voltages. Assumes corresponding lock-bits are not set. Subject to change based on device characterization.
2. Excludes system-level overhead.
3. These performance numbers are valid for all speed versions.
4. Sampled but not 100% tested.
5. These values are valid when the buffer is full, and the start address is aligned on a 32-byte boundary.
6. The maximum write time is the absolute maximum time it takes the write algorithm to complete. The overwhelming majority of the bits are written within the typical value specified. To maximize system performance, the BUSY# signal should be polled to determine the completion of a write operation.

8.0 PACKAGING

Figure 9 shows the outside dimensions of the 5 Volt Series 200 Miniature Card. For complete mechanical drawings refer to the Miniature Card Specification.

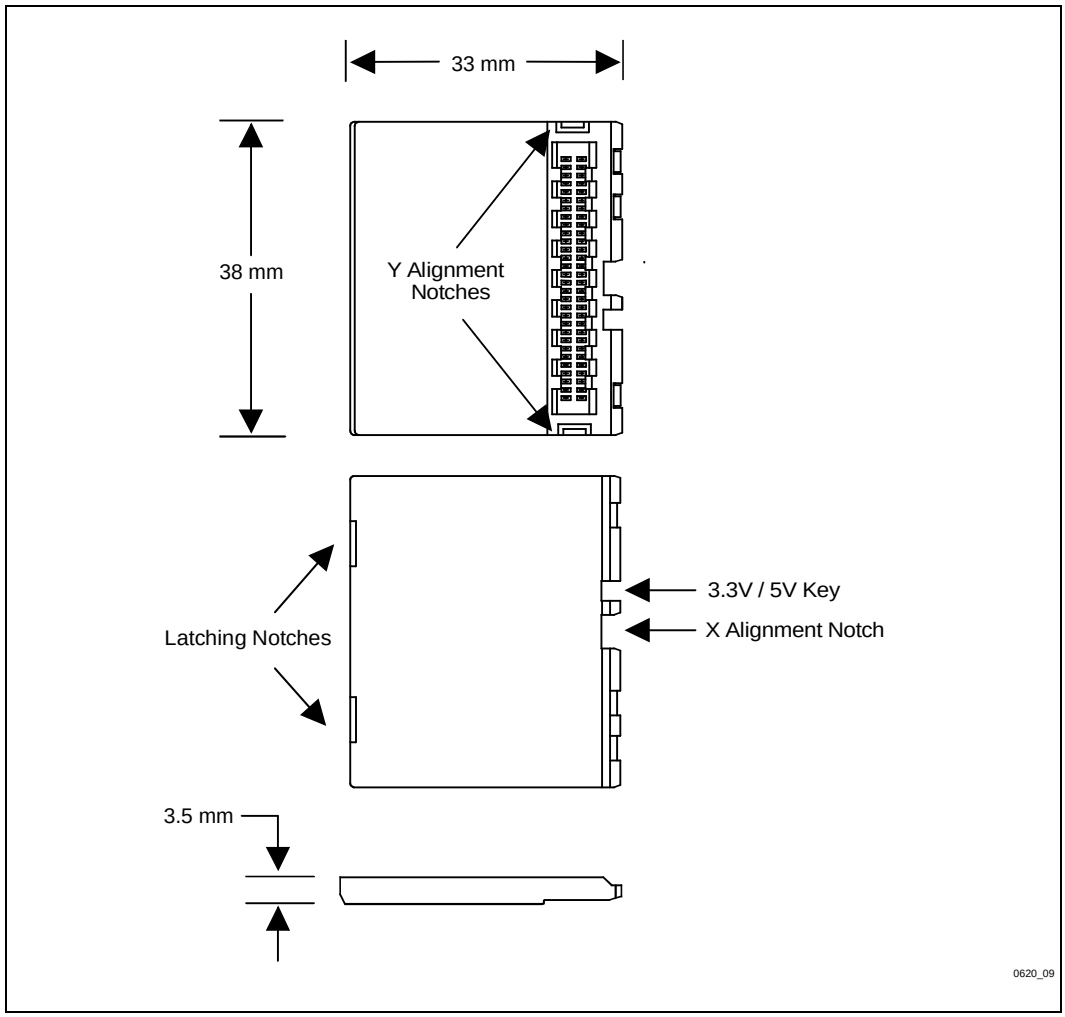


Figure 9. Miniature Card Dimensions

9.0 ORDERING INFORMATION

iFM004G, SHXXXXX

Where:

i	= INTEL
FM	= FLASH MINIATURE CARD
004	= DENSITY IN MEGABYTES (004, 008, 016 AVAILABLE)
G	= REVISION
SHXXXXX	= CUSTOMER IDENTIFIER

10.0 ADDITIONAL INFORMATION

Order Number	Document
210830	*Flash Memory Databook*
297899	*5 Volt Series 200 Flash Memory Miniature Card Specification Update*
290606	*5 Volt Intel® StrataFlash™ Memory; 28F320J5 and 28F640J5* datasheet
297848	*5 Volt Intel® StrataFlash™ Memory; 28F320J5 and 28F640J5 Specification Update*
292205	*AP-647 5 Volt Intel® StrataFlash™ Memory Design Guide*
292204	*AP-646 Common Flash Interface (CFI) and Command Sets*
292203	*AP-644 Migration Guide to Intel® StrataFlash™ Memory*
Note 3	*AP-374 Flash Memory Write Protection Techniques*

NOTE:

1. Please call the Intel Literature Center at (800) 548-4725 to request Intel documentation. International customers should contact their local Intel or distribution sales office.
2. Visit Intel's World Wide Web home page at http://www.intel.com for technical documentation and tools.
3. These documents can be located at the Intel World Wide Web support site, http://www.intel.com/support/flash/memory