P-Channel 1.8 V (G-S) MOSFET with Schottky Diode

MOSFET PRODUCT SUMMARY		
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)
- 20	0.110 at V_{GS} = - 4.5 V	- 3.6
	0.160 at V_{GS} = - 2.5 V	- 3.0
	0.240 at V_{GS} = - 1.8 V	- 2.4

SCHOTTKY PRODUCT SUMMARY		
V_{KA} (V)	V_f (V) Diode Forward Voltage	I_F (A)
20	0.375 V at 1 A	1.0

FEATURES

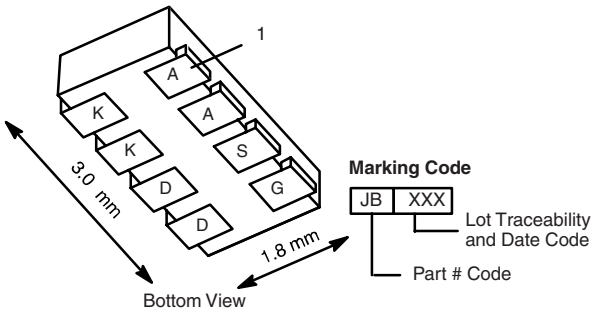
- **Halogen-free According to IEC 61249-2-21 Definition**
- TrenchFET® Power MOSFETs
- Ultra Low V_f Schottky
- Si5853DC Pin Compatible
- Compliant to RoHS Directive 2002/95/EC

Pb-free
RoHS COMPLIANT
HALOGEN FREE Available

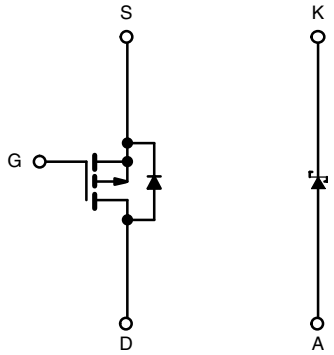
APPLICATIONS

- Charging Circuit in Portable Devices

1206-8 ChipFET®



Ordering Information: Si5855DC-T1-E3 (Lead (Pb)-free)
Si5855DC-T1-GE3 (Lead (Pb)-free and Halogen-free)



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted					
Parameter		**Symbol**	**5 s**	**Steady State**	**Unit**
Drain-Source Voltage (MOSFET)		V_{DS}	- 20		V
Reverse Voltage (Schottky)		V_{KA}	20		
Gate-Source Voltage (MOSFET)		V_{GS}	± 8		
Continuous Drain Current (T_J = 150 °C) (MOSFET)[a]	T_A = 25 °C	I_D	- 3.6	- 2.7	A
	T_A = 85 °C		- 2.6	- 1.9	
Pulsed Drain Current (MOSFET)		I_{DM}	- 10		
Continuous Source Current (MOSFET Diode Conduction)[a]		I_S	- 1.8	- 0.9	
Average Forward Current (Schottky)		I_F	1.0		
Pulsed Forward Current (Schottky)		I_{FM}	7		
Maximum Power Dissipation (MOSFET)[a]	T_A = 25 °C	P_D	2.1	1.1	W
	T_A = 85 °C		1.1	0.6	
Maximum Power Dissipation (Schottky)[a]	T_A = 25 °C		1.9	1.1	
	T_A = 85 °C		1.0	0.56	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 150		°C
Soldering Recommendations (Peak Temperature)[b, c]			260		

Notes:
a. Surface mounted on 1" x 1" FR4 board.
b. See reliability manual for profile. The ChipFET is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
c. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.

THERMAL RESISTANCE RATINGS

Parameter		Device	Symbol	Typical	Maximum	Unit
Junction-to-Ambient[a]	t ≤ 5 s	MOSFET	R_{thJA}	50	60	°C/W
		Schottky		54	65	
	Steady State	MOSFET		90	110	
		Schottky		95	115	
Junction-to-Foot	Steady State	MOSFET	R_{thJF}	30	40	
		Schottky		30	40	

Notes:
a. Surface mounted on 1" x 1" FR4 board.

MOSFET SPECIFICATIONS T_J = 25 °C, unless otherwise noted

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = - 250 µA	- 0.45		- 1.0	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 8 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = - 20 V, V_{GS} = 0 V			- 1	µA
		V_{DS} = - 20 V, V_{GS} = 0 V, T_J = 85 °C			- 5	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} ≤ – 5 V, V_{GS} = - 4.5 V	- 10			A
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = - 4.5 V, I_D = - 2.7 A		0.095	0.110	Ω
		V_{GS} = - 2.5 V, I_D = - 2.2 A		0.137	0.160	
		V_{GS} = - 1.8 V, I_D = - 1 A		0.205	0.240	
Forward Transconductance[a]	g_{fs}	V_{DS} = - 10 V, I_D = - 2.7 A		7		S
Diode Forward Voltage[a]	V_{SD}	I_S = - 0.9 A, V_{GS} = 0 V		- 0.8	- 1.2	V
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = - 10 V, V_{GS} = - 4.5 V, I_D = - 2.7 A		5.1	7.7	nC
Gate-Source Charge	Q_{gs}			1.2		
Gate-Drain Charge	Q_{gd}			1.0		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = - 10 V, R_L = 10 Ω I_D ≅ - 1 A, V_{GEN} = - 4.5 V, R_g = 6 Ω		16	25	ns
Rise Time	t_r			30	45	
Turn-Off Delay Time	$t_{d(off)}$			30	45	
Fall Time	t_f			27	40	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = - 0.9 A, dI/dt = 100 A/µs		20	40	

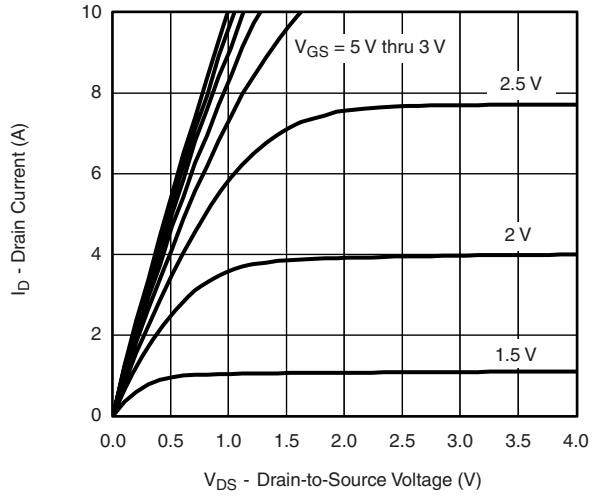
Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

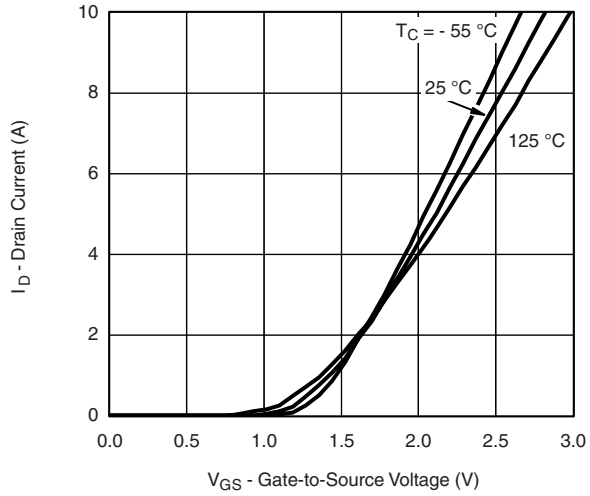
SCHOTTKY SPECIFICATIONS T_J = 25 °C, unless otherwise noted

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Forward Voltage Drop	V_F	I_F = 1 A		0.34	0.375	V
		I_F = 1 A, T_J = 125 °C		0.255	0.290	
Maximum Reverse Leakage Current	I_{rm}	V_r = 20 V		0.05	0.500	mA
		V_r = 20 V, T_J = 85 °C		2	20	
		V_r = 20 V, T_J = 125 °C		10	100	
Junction Capacitance	C_T	V_r = 10 V		90		pF

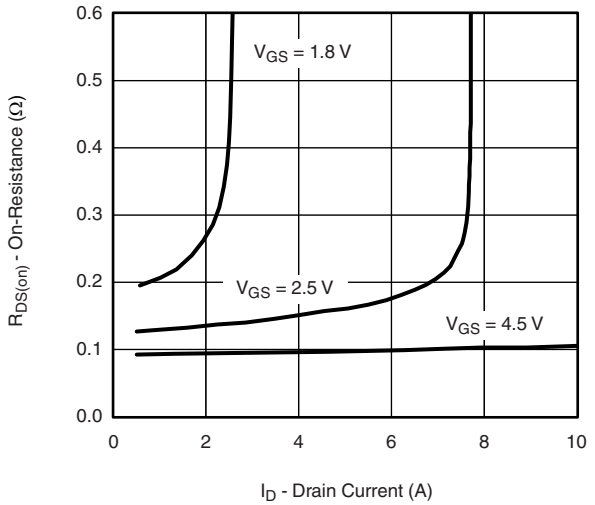
MOSFET TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



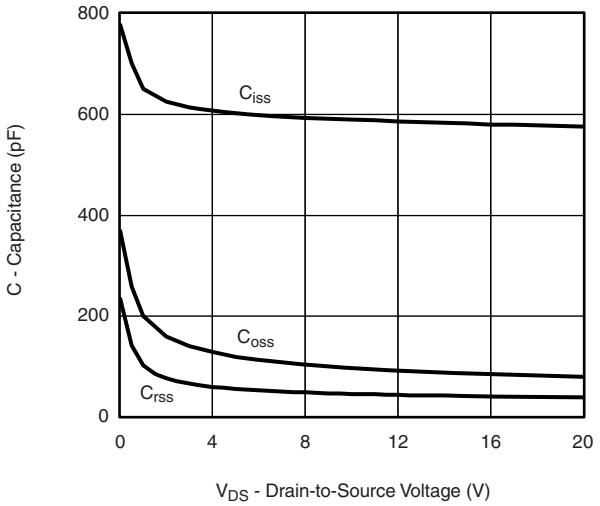
Output Characteristics



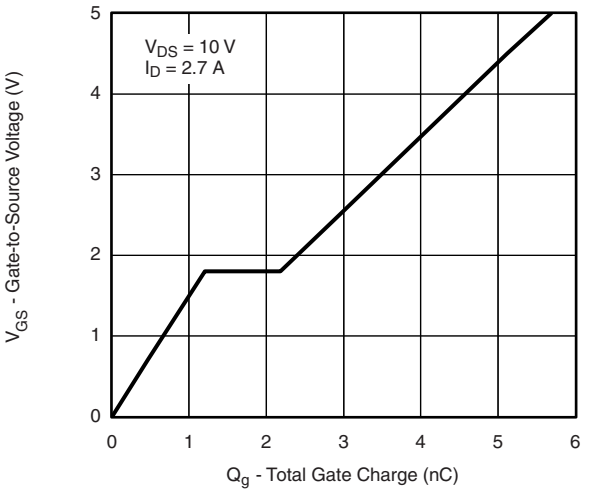
Transfer Characteristics



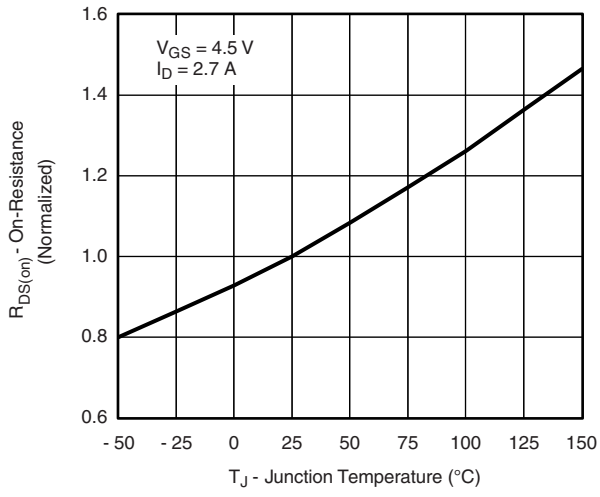
On-Resistance vs. Drain Current



Capacitance

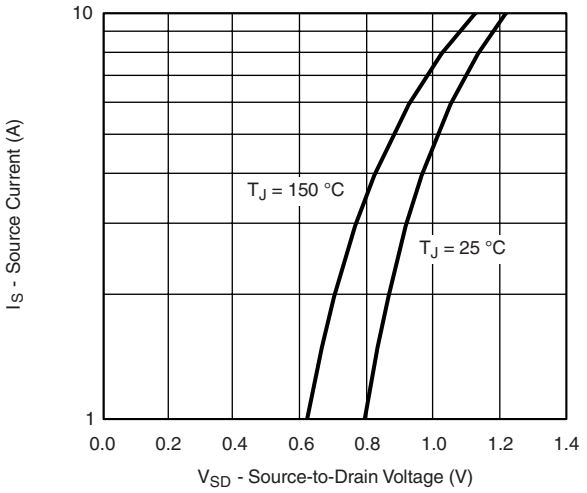


Gate Charge

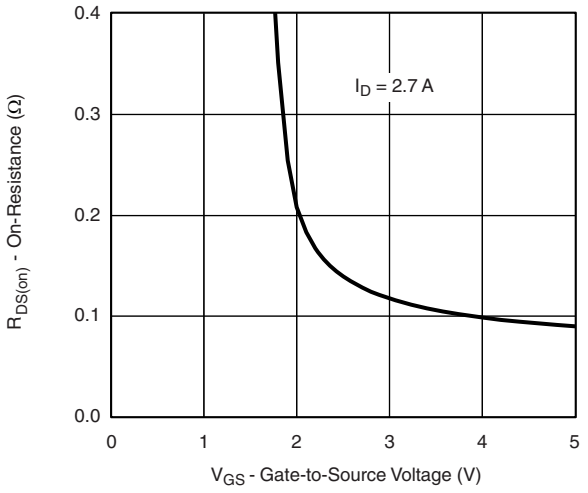


On-Resistance vs. Junction Temperature

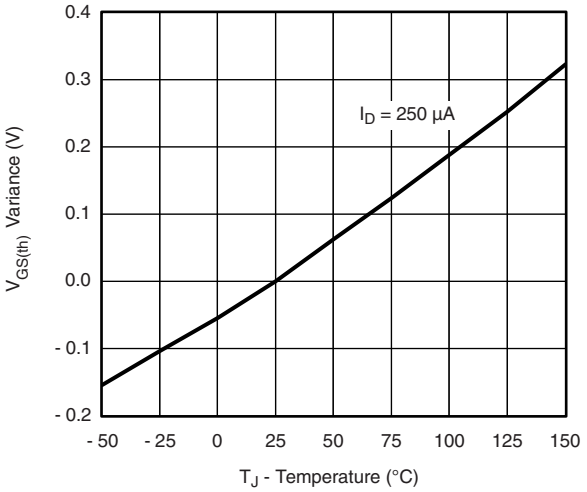
MOSFET TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



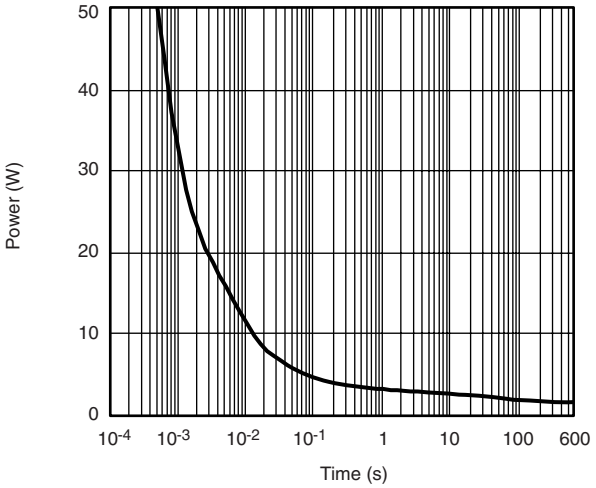
Source-Drain Diode Forward Voltage



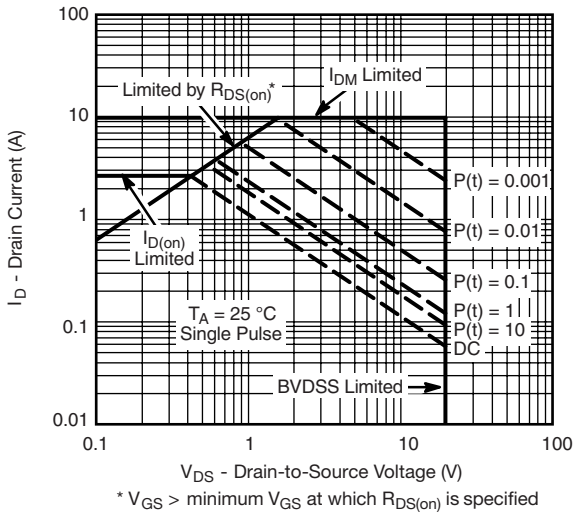
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

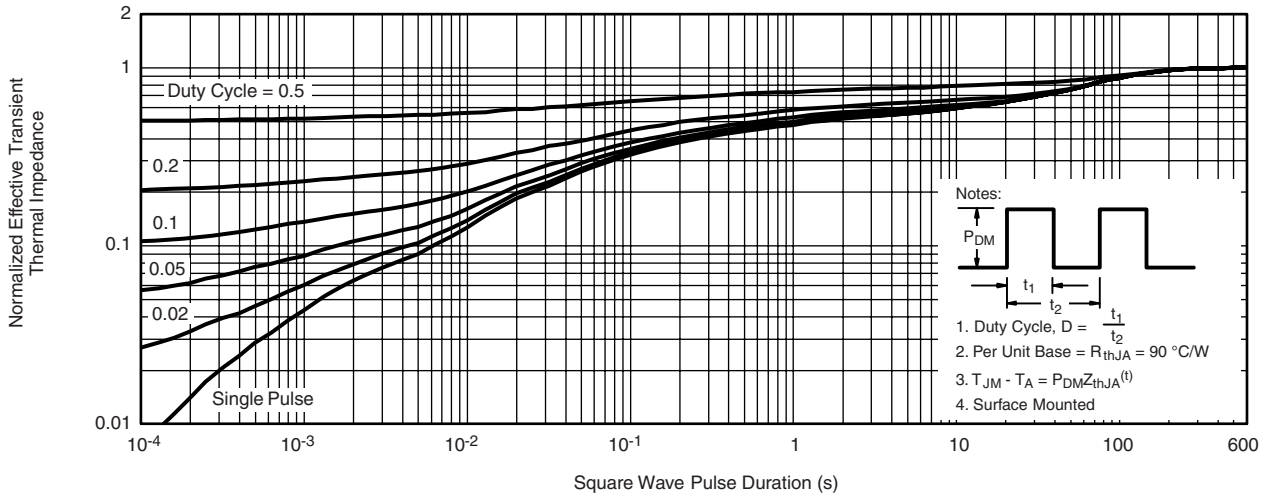


Single Pulse Power

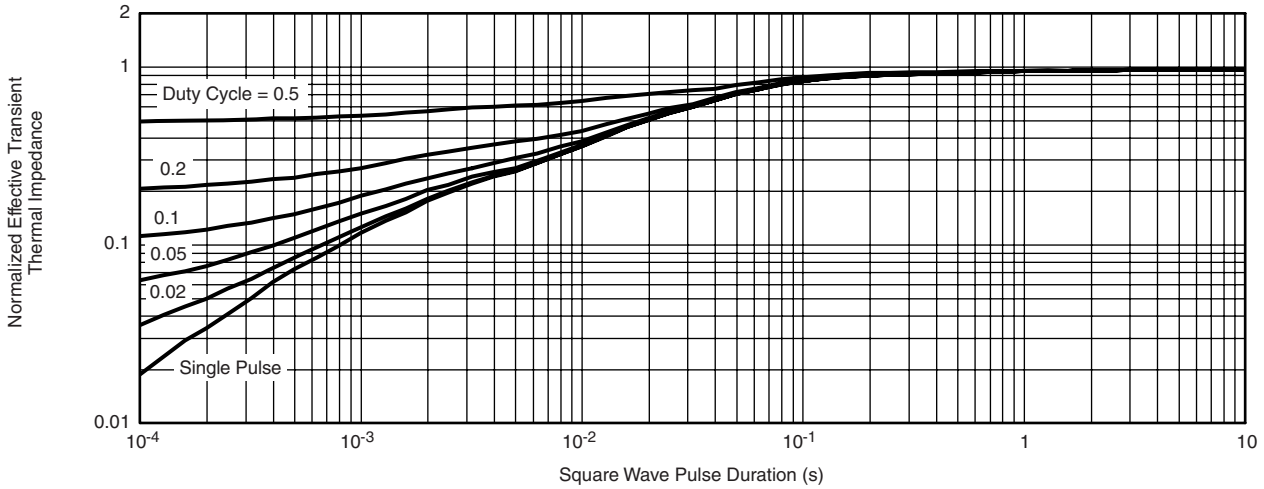


Safe Operating Area

MOSFET TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

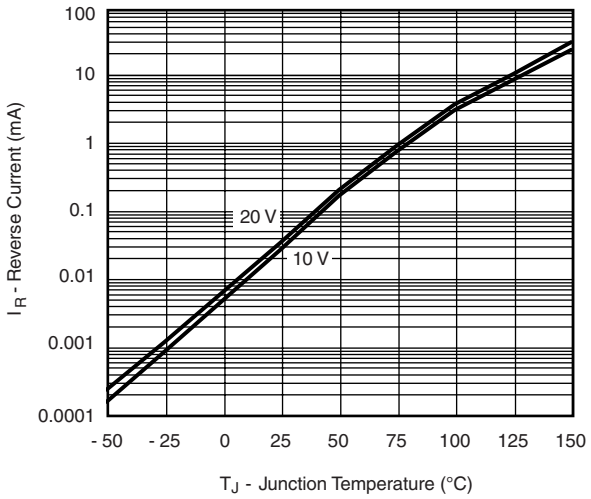


Normalized Thermal Transient Impedance, Junction-to-Ambient

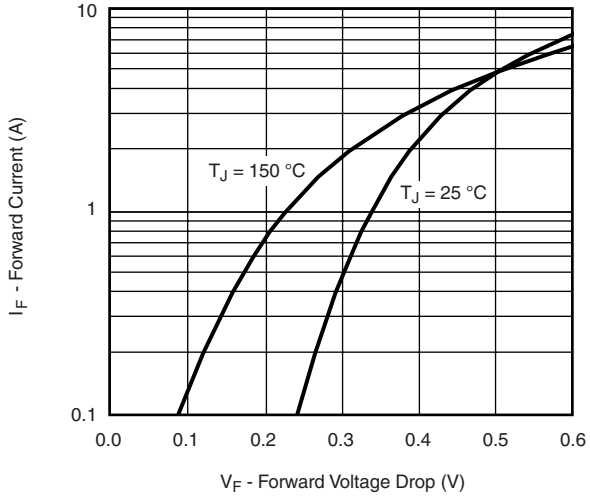


Normalized Thermal Transient Impedance, Junction-to-Foot

SCHOTTKY TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

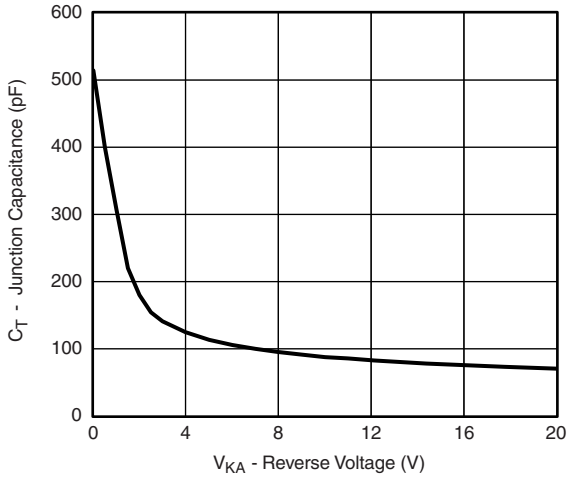


Reverse Current vs. Junction Temperature

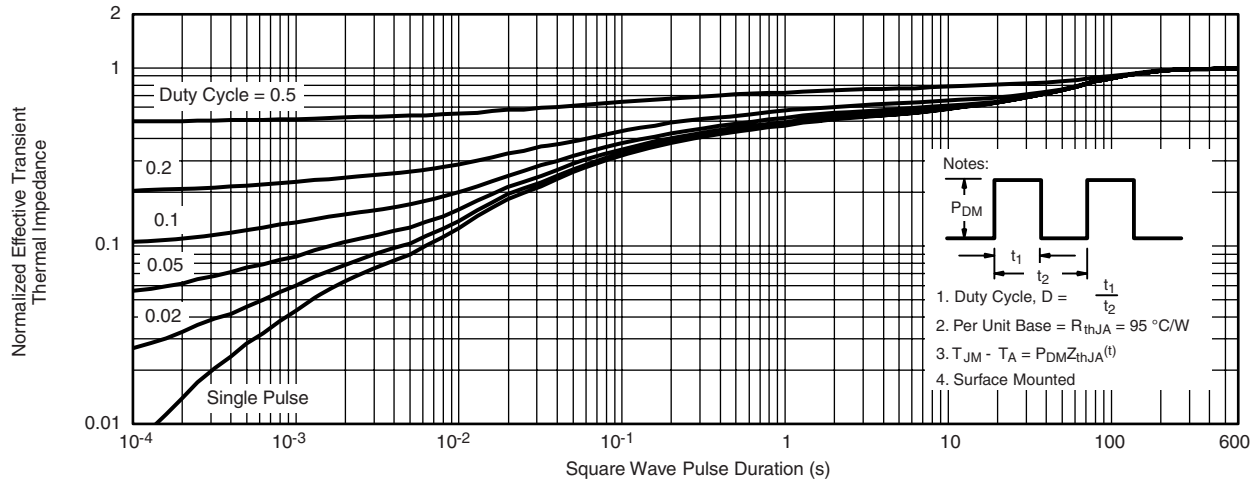


Forward Voltage Drop

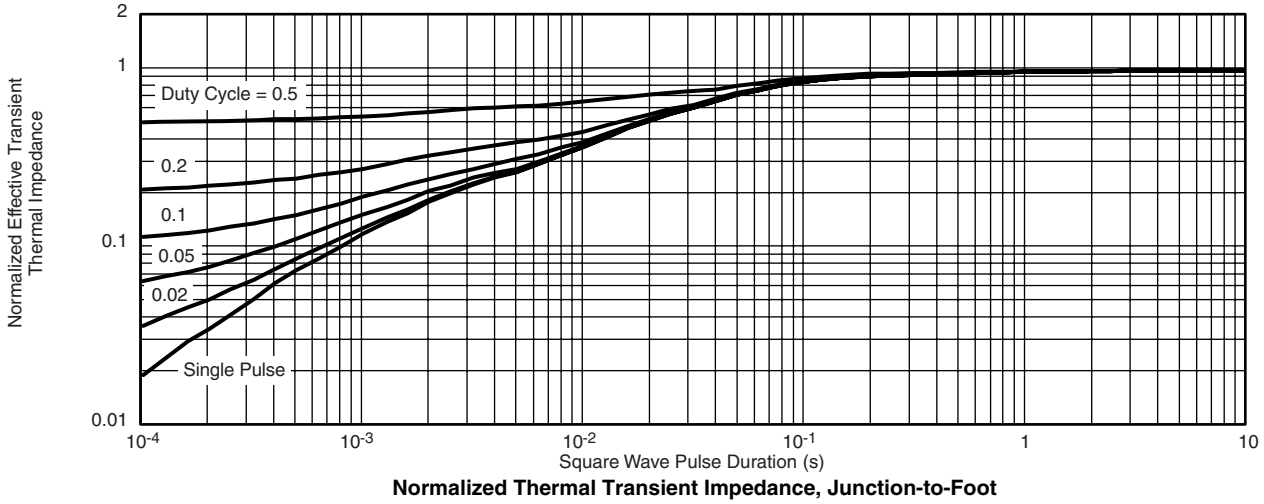
SCHOTTKY TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Capacitance



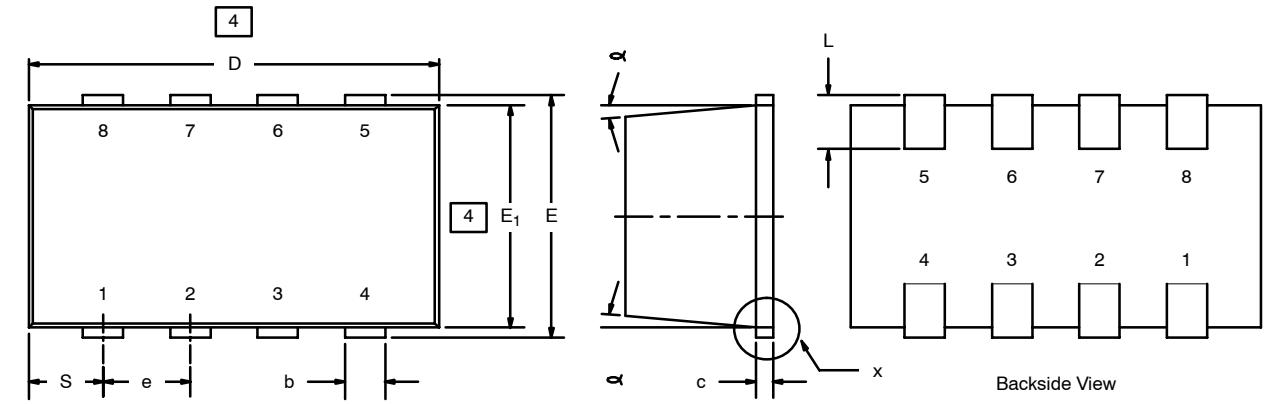
Normalized Thermal Transient Impedance, Junction-to-Ambient

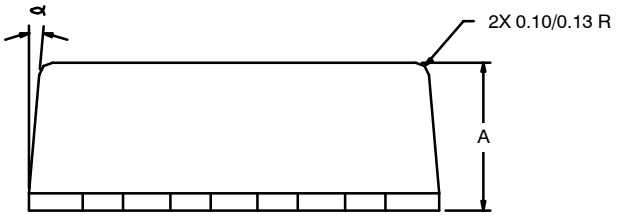


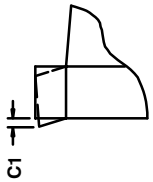
Normalized Thermal Transient Impedance, Junction-to-Foot

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?72232.

1206-8 ChipFET®







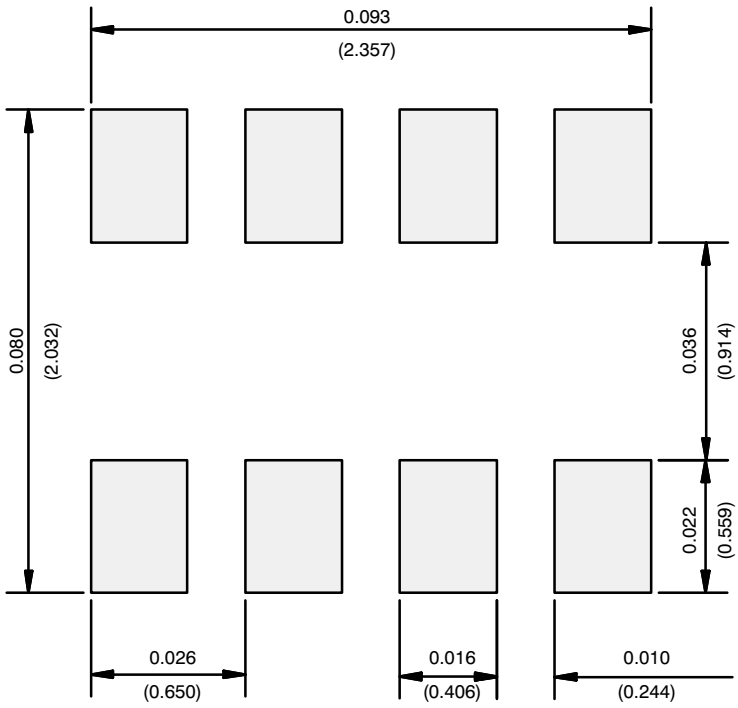
DETAIL X

NOTES:

1. All dimensions are in millimeaters.
2. Mold gate burrs shall not exceed 0.13 mm per side.
3. Leadframe to molded body offset is horizontal and vertical shall not exceed 0.08 mm.
4. Dimensions exclusive of mold gate burrs.
5. No mold flash allowed on the top and bottom lead surface.

	MILLIMETERS			INCHES		
Dim	**Min**	**Nom**	**Max**	**Min**	**Nom**	**Max**
A	1.00	–	1.10	0.039	–	0.043
b	0.25	0.30	0.35	0.010	0.012	0.014
c	0.1	0.15	0.20	0.004	0.006	0.008
c1	0	–	0.038	0	–	0.0015
D	2.95	3.05	3.10	0.116	0.120	0.122
E	1.825	1.90	1.975	0.072	0.075	0.078
E_1	1.55	1.65	1.70	0.061	0.065	0.067
e	0.65 BSC			0.0256 BSC		
L	0.28	–	0.42	0.011	–	0.017
S	0.55 BSC			0.022 BSC		
α	5°Nom			5°Nom		
ECN: C-03528—Rev. F, 19-Jan-04 DWG: 5547						

RECOMMENDED MINIMUM PADS FOR 1206-8 ChipFET®



Recommended Minimum Pads
Dimensions in Inches/(mm)

Return to Index

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