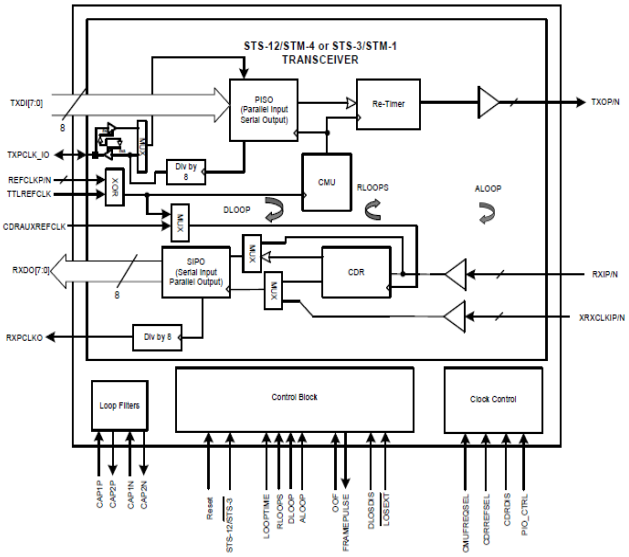
# XRT91L30 STS12-STM4 OR STS3-STM1 SONET-SDH Transceiver

## General Description:

The XRT91L30 is a fully integrated SONET/SDH transceiver for SONET/SDH 622.08 Mbps STS-12/STM-4 or 155.52 Mbps STS-3/STM-1 applications. The transceiver includes an on-chip Clock Multiplier Unit (CMU), which uses a high frequency Phase- Locked Loop (PLL) to generate the high-speed transmit serial clock from a slower external clock reference. It also provides Clock and Data Recovery (CDR) function by synchronizing its on-chip Voltage Controlled Oscillator (VCO) to the incoming serial data stream. The internal CDR unit can be disabled and bypassed in lieu of an externally recovered received clock from the optical module. Either the internally recovered clock or the externally recovered clock can be used for loop timing applications. The chip provides serial-to-parallel and parallel-to-serial converters using an 8-bit wide LVTTL system interface in both receive and transmit directions. The transmit section includes an option to accept a parallel clock signal from the framer/mapper to synchronize the transmit section timing. The device can internally monitor Loss of Signal (LOS) condition and automatically mute received data upon LOS. An on-chip SONET/SDH frame byte and boundary detector and frame pulse generator offers the ability recover SONET/SDH framing and to byte align the receive serial data stream into the 8-bit parallel bus.

## Key Features:




- Targeted for SONET STS-12/STS-3 and SDH STM-4/STM-1 Applications
- Selectable full duplex operation between STS-12/STM-4 standard rate of 622.08 Mbps or STS-3/STM-1 155.52 Mbps
- Single-chip fully integrated solution containing parallel-to-serial converter, clock multiplier unit (CMU), serialto-parallel converter, clock data recovery (CDR) functions, and a SONET/SDH frame and byte boundary detection circuit
- Ability to disable and bypass onchip CDR for external based received reference clock recovery thru Differential LVPECL input pins XRXCLKIP/N

- 8-bit LVTTL parallel data bus paths running at 77.76 Mbps in STS-12/STM-4 or 19.44 Mbps in STS-3/STM-1mode of operation
- Uses Differential LVPECL or Single-Ended LVTTL CMU reference clock frequencies of either 19.44 MHz or 77.76 MHz for both STS-12/STM-1 or STS-3/STM-1 operations
- Optional use of 77.76 MHz Single-Ended LVTTL input for independent CDR reference clock operation
- Able to Detect and Recover SONET/SDH frame boundary and byte align received data on the parallel bus
- Diagnostics features include LOS monitoring and automatic received data mute upon LOS
- Provides Local, Remote and Split Loop-Back modes as well as Loop Timing mode
- Optional flexibility to re-configure the transmit parallel bus clock output to a clock input and accept timing signal from the framer/mapper device to permit the framer/mapper device time domain to be synchronized with the transceiver transmit timing
- Meets Telcordia, ANSI and ITU-T G.783 and G.825 SDH jitter requirements including T1.105.03 – 2002 SONET Jitter Tolerance specification, Bellcore TR-NWT-000253 and GR-253-CORE, GR-253 ILR SONET Jitter specifications
- Complies with ANSI/TIA/EIA-644 and IEEE P1596.3 3.3V LVDS standard, 3.3V LVPECL, and JESD 8-B LVTTL and LVCMOS standard
- Operates at 3.3V Core with 3.3V I/O
- Less than 660mW in STS-3/STM-1 mode or 800mW in STS-12/STM-4 mode Typical Power Dissipation
- Package: 10 x 10 x 2.0 mm 64-pin QFP

## Applications:

- SONET/SDH-based Transmission Systems
- Add/Drop Multiplexers
- Cross Connect Equipment
- ATM and Multi-Service Switches, Routers and
- Switch/Routers
- DSLAMS
- SONET/SDH Test Equipment
- DWDM Termination Equipment

## Related Products Information:

| Mfr Part # | Farnell # | Newark # | Description |
|---|---|---|---|
| XRT91L30IQ-F | 1798688 | 24R1992 | STS-12/STM-4 OR STS-3/STM-1 SONET/SDH Transceiver-64-pin QFP package |
| XRT91L32IQ-F | 1798689 | 73R5147 | STS-12/STM-4 OR STS-3/STM-1 SONET/SDH Transceiver -100-pin QFP Package |