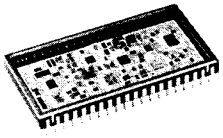
ADC-00305II

12 BIT 2 MHz T/H + A/D HYBRID
HIGH SPEED, SMALL SIZE, LOW COST



IMPROVED

DESCRIPTION

The ADC-00305II is a 12 bit, 500 nsec (2 MHz) track/hold and A/D converter hybrid packaged in a 40 pin TDIP, following in the footsteps of the industry standard ADC-00300 and ADC-00305.

Containing T/H, A/D converter, data registers, tri-state output buffers, and timing circuits, the ADC-00305II is a fast and small full-function digitizer. The ADC-00305II operates over a temperature range of 0°C to +70°C and is ideal for low-cost industrial applications.

The ADC-00305II is implemented with a 2-step A/D conversion algorithm. A number of factors contributed to achieving the ADC-00305II's technical breakthroughs in speed and size. Foremost among them were the high-speed T/H, DAC, and the gain amplifier. All are DDC proprietary designs and single custom monolithics. In addition, judicious use of thin-film and thick-film hybrid technology resulted in minimum layout area and power consumption.

With its high speed, small package, and wide operating temperature range, the ADC-00305II is ideal for the most demanding commercial data conversion applications. Typical of these applications are radar, IR, and NMR digitizing; vibration and FFT analysis; medical and scientific instrumentation; and high-speed data-acquisition systems.

FEATURES

- ***Includes:***
  - ***–Track/Hold***
  - ***–A/D Converter***
  - ***–Tri-state Output Registers***
  - ***–Timing Circuits***
- ***2 MHz Word Rate***
- ***Pin-for-pin Enhanced Revision to the ADC-00305***
- ***Low Power***
- ***Small 40 Pin TDIP Hermetic Hybrid***
- ***Low Cost***

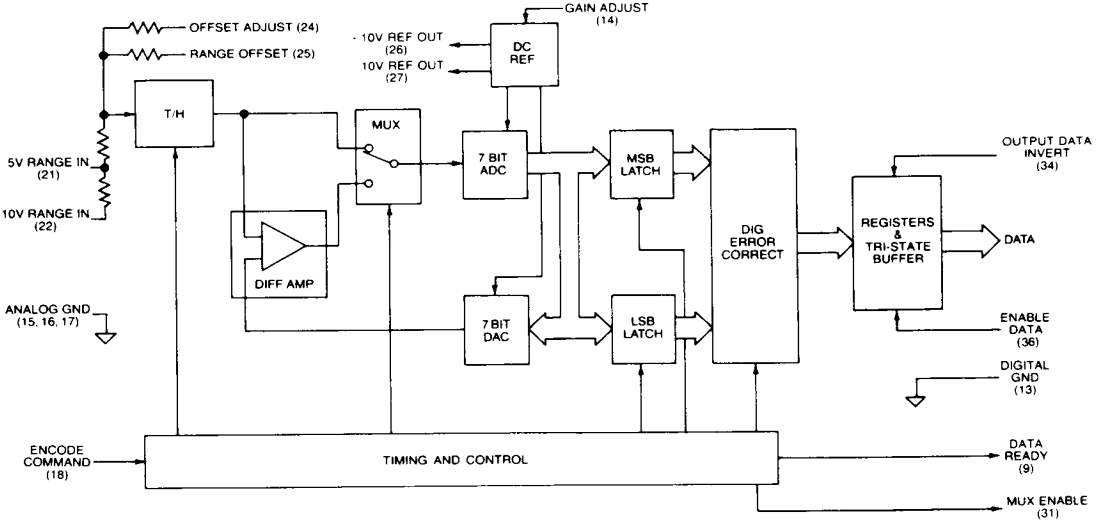


FIGURE 1. ADC-00305II BLOCK DIAGRAM

TABLE 1. ADC-00305II SPECIFICATIONS (T/H and A/D)
Typical values at +25°C case temperature and nominal power supply voltages.

PARAMETER	UNITS	VALUES
RESOLUTION	Bits	12
ACCURACY		
Linearity Error	%FSR	±0.012 typ, ±0.025 max
Linearity Error Tempco	ppm FSR/°C	2 max
Diff Linearity Error	LSB	±1 max
Gain Error(1)	%FSR	±0.5 max
Gain Error Tempco	ppm FSR/°C	40
Offset Error(1)	%FSR	±0.5 max
Offset Error Tempco	ppm FSR/°C	20 max
DYNAMICS		
Conversion Rate(2)	MHz	dc to 2 min
Harmonics(3)	dB below FSR	72 typ, 68 min
Signal to Noise Ratio(2)(4)	dB	68 typ, 65 min
Input Bandwidth(2)		
Small Signal(5)	MHz	10 min
Large Signal(6)	MHz	10 min
Flat to 0.25 dB	MHz	dc to 1
Aperture Jitter	psec	25 max
Aperture Delay	nsec	25 max
Overvoltage Recovery(7)	µsec	5 max
ANALOG INPUT		See table 2
DIGITAL INPUTS		
Encode Command(8)		
Width	nsec	50 min, 300max
Rise/Fall Time	nsec	25 max
Frequency	MHz	dc to 2 min
Output Data Invert Loading	Ohms	50K
DIGITAL OUTPUTS		
Parallel Data		
Format	Bits	12(tri-state)
Drive	TTL Loads	3
Coding		See table 3
Data Ready(9)		
Rise/Fall Time	nsec	25 max
Drive	TTL Loads	3
INTERNAL REFERENCE		
Pos Voltage Output	V	+10±0.65%
Pos Current Output(10)	mA	±2
Pos Voltage Tempco	ppm/°C	±25 max
Neg Voltage Output	V	-10±0.3%
Neg Current Output(10)	mA	±2
Neg Voltage Tempco	ppm/°C	±20 max
POWER SUPPLIES		
+15 Volt Supply	V	+15±5%
Current Drain	mA	40 typ, 60 max
-15 Volt Supply	V	-15±5%
Current Drain	mA	55 typ, 70 max
+5 Volt Supply	V	+5±5%
Current Drain	mA	175 typ, 220 max
-5 Volt Supply	V	+5±10%
Current Drain	mA	40 typ, 50 max
PSRR	%FSR/V	0.1

TABLE 1. ADC-00305II SPECIFICATIONS (T/H and A/D) (continued)

PARAMETER	UNITS	VALUES
POWER DISSIPATION	W	2.5 typ, 3.5 max
TEMPERATURE RANGE		
Operating (Case)	°C	0 to +70
PACKAGE		
Type		40 pin TDIP
Size	in(mm)	1.3 x 2.2 x 0.25 (33 x 56.0 x 6.4)

Notes:
(1) Trimmable to zero with external potentiometer.
(2) Value specified over operating temperature range.
(3) For dc to 1MHz input with 2 MHz encode rate.
(4) Rms signal to rms noise ratio with 200 kHz analog input.
(5) 3 dB bandwidth with analog input 40 dB below full scale.
(6) 3 dB bandwidth with full scale analog input.
(7) Recovery to rated accuracy from twice full scale input step.
(8) LOW to HIGH transition initiates encoding.
(9) LOW to HIGH transition indicates start of valid data interval.
(10) Current load for no performance degradation.

GENERAL DESCRIPTION

Figure 1 is a functional block diagram of the ADC-00305II sampling A/D converter following in the footsteps of the industry standard ADC-00300. Its major elements are a track/hold amplifier, a 7-bit flash A/D converter, a 7-bit D/A converter, a differential amplifier, and a 2-channel multiplexer. The remaining functions are timing and control circuits, digital buffers and registers, and dc voltage references.

These components implement a 2-step A/D conversion algorithm, whose operation is quite straight-forward. First, the conversion cycle is initiated with the receipt of an Encode Command. This causes the timing circuit to place the track/hold in the HOLD mode, storing the voltage at its analog input. Then, the flash A/D converter generates a coarse encode of the sampled voltage. Its 7-bit coarse encode output is stored temporarily in the MSB register. At the same time, the coarse 7-bit word is input to the DAC, which converts it to an analog voltage. The differential amplifier subtracts the voltage representing the coarse encode from the sampled input and scales it up to the correct full scale range. Next, the flash A/D converter generates a fine encode of the scaled difference voltage. The fine encode 7-bit word is stored in the LSB register. Finally, the contents of the 7-bit MSB and LSB registers are combined in the digital error correction circuit to yield a 12-bit output word. This 12-bit word is stored in the output registers. The encoded digital output is available upon application of an Enable signal to the tri-state output buffers.

The entire 2-step conversion can be accomplished in as little as 250 nsec. Since the ADC-00305II has output storage registers, its digital output is available to the user at all times, except for a short interval when it is being updated. A Data Ready output signal is provided to indicate when the digital output is valid.

The ADC-00305II may be configured for any of six (6) different input signal ranges by means of jumper wires between pins. Two bipolar ranges, two positive unipolar, and two negative unipolar input ranges are implemented by using the 2 internal references, along with precision resistors, to scale and offset the input signal.

The positive and negative internal references are made available to the user at output pins. If they are used, care must be taken not to load them beyond their rated outputs, or else converter performance will deteriorate. Residual gain and offset errors may be trimmed to zero, with the addition of external potentiometers.

A number of digital output codes are available from the ADC-00305II (see Table 3). For bipolar analog input signals, the digital output data is coded in Inverted Offset Binary or Inverted Two's Complement. Either of these codes is available, since both the MSB (Bit 1) and its complement are provided as outputs. For either positive unipolar or negative unipolar, the digital output code is Inverted Binary. The Output Data Invert pin (pin 34), when tied to +5V, inverts all of the above codes.

Care must be taken when designing with the ADC-00305II, to achieve its rated performance. This high-speed sampling A/D converter generates high-frequency power-supply and ground currents. For this reason, it is recommended that decoupling capacitors be used on each power supply line and both internal references. High-frequency layout considerations should be kept in mind when designing a printed circuit board for the ADC-00305II. Conductor lengths should be kept to a minimum, and a large-area ground-plane should be used to keep ground impedances as low as possible.

TIMING DIAGRAM

A diagram of typical ADC-00305II timing is shown in figure 2. It is to be noted that the diagram shows the Encode Command repeating at 500 nsec intervals, which corresponds with the minimum conversion time. The Encode Command may be repeated at intervals ≥ 500 nsec and is independent of internal timing.

A conversion cycle is initiated by the application of a positive pulse (50 nsec min) to the Encode Command pin. The rising edge of the Encode Command starts the timing cycle. The internal track/hold is placed in the HOLD mode and MUX Enable makes a LOW to HIGH transition 25 nsec max after the Encode Command leading edge. This delay reflects the aperture delay of the internal track/hold. MUX Enable remains HIGH for approximately 160 nsec before making a transition to LOW. This coincides with the track/hold going into the TRACK mode.

At this point the internal flash A/D converter has completed its second encode and the track/hold can begin to acquire a new analog input. The remaining time in the conversion cycle is associated with delays through the digital sections that follow the flash A/D converter. Approximately 100 nsec after the HIGH to LOW transition of the MUX Enable signal the Data Ready signal makes a HIGH to LOW transition. The Data Ready line stays LOW for 100 nsec, during which time the output register is updated with the new data word. Updating the output data register is accomplished during the first 30 nsec of the interval

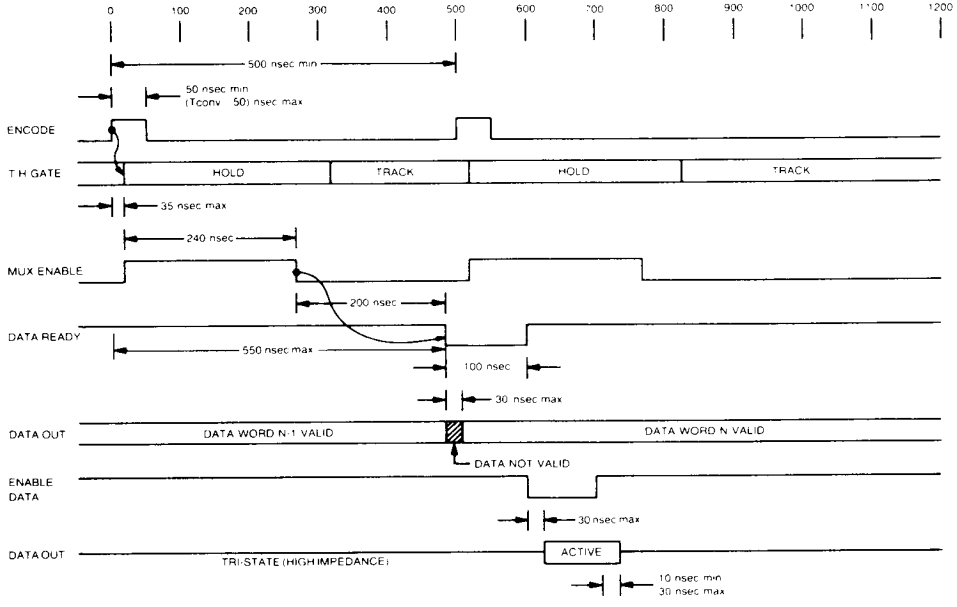


FIGURE 2. ADC-00305II TIMING DIAGRAM

during which the Data Ready line is LOW. Output data is not valid during this 30 nsec interval. ADC-00305II data is valid at all times that the Data Ready line is HIGH and during the final 70 nsec of its 100 nsec LOW interval.

Enable Data, which is active LOW, has a propagation delay of 15 nsec typ., 30 nsec max to active ADC-00305II data output. The LOW to HIGH transition of Enable Data is followed by a 10 nsec min, 30 nsec max tri-state propagation delay as illustrated in figure 2. The HIGH to LOW transition of the MUX Enable signal is passed through a delay chain that eventually generates the negative Data Ready pulse. If no additional Encode Commands are received, the MUX Enable line will remain Low. The timing diagram in figure 2 shows Encode Commands occurring at 500 nsec intervals. Pin 10 must be tied to +5V, enabling operation from dc to 2 MHz.

MUX ENABLE

The ADC-00305II provides a Mux Enable signal (pin 31), whose digital state is coincident with the internal T/H status (see figure 2). This signal can be used to advance the address to a multiplexer in time-division multiplexed applications.

ANALOG INPUT RANGES

The ADC-00305II may by configured for any of six (6) different input signal ranges by means of jumper wires between pins. Two bipolar, two positive unipolar, and two negative unipolar ranges are possible. Table 2, Analog Input Range, lists the jumper connection and appropriate analog input terminal to be used for each configuration. For each analog input range, the absolute maximum input voltage is listed, along with the corresponding input impedance.

OUTPUT CODING

The ADC-00305II provides a number of digital output data codes. For bipolar analog input signals, the digital output data is coded in Inverted Offset Binary or Inverted Two's Complement. Either of these codes is available, since both the MSB (Bit 1) and its complement are provided as outputs. For either positive unipolar or negative unipolar, the digital output code is Inverted Binary. Table 3, Output Coding, lists the output data for various analog inputs for each of the code configurations. The Output Data Invert pin (pin 34), when tied to +5V, inverts all of the above codes.

TABLE 2. ANALOG INPUT RANGE

INPUT RANGE	ABSOLUTE MAX INPUT	INPUT IMPEDANCE (1)	INPUT TERMINAL	JUMPER CONNECTION
±2.5V	±5V	500Ω	PIN 21	PIN 16 to PIN 25
±5V	±10V	1000Ω	PIN 22	PIN 16 to PIN 25
0 to +5V	+10V	500Ω	PIN 21	PIN 25 to PIN 27
0 to +10V	+20V	1000Ω	PIN 22	PIN 25 to PIN 27
0 to −5V	−10V	500Ω	PIN 21	PIN 25 to PIN 26
0 to −10V	−20V	1000Ω	PIN 22	PIN 25 to PIN 26

Note: (1) ± 1.1% at 25°C, ± 50ppm/°C

TABLE 3. OUTPUT CODING (1)

INPUT VOLTAGE	BIPOLAR		POS UNIPOLAR	NEG UNIPOLAR
	Inverted Offset Binary	Inverted Two's Complement	Inverted Binary	Inverted Binary
+FS−1LSB	0000 0000 0000	1000 0000 0000	0000 0000 0000	–
+¾FS	0001 1111 1111	1001 1111 1111	0011 1111 1111	–
+½FS	0011 1111 1111	1011 1111 1111	0111 1111 1111	–
+1LSB	0111 1111 1110	1111 1111 1110	1111 1111 1110	–
0	0111 1111 1111	1111 1111 1111	1111 1111 1111	0000 0000 0000
−1LSB	1000 0000 0000	0000 0000 0000	–	0000 0000 0001
−½FS	1011 1111 1111	0011 1111 1111	–	0111 1111 1111
−¾FS	1101 1111 1111	0111 1111 1111	–	1100 0000 0000
−FS+1LSB	1111 1111 1110	0111 1111 1110	–	1111 1111 1111
−FS	1111 1111 1111	0111 1111 1111	–	–
	B1 thru B12	$\overline{B1}$, B2 thru B12		

Note:
(1)Codes shown for pin 34 (Output Data Invert) open or tied to Ground. When Pin 34 is tied to +5V, all of the above codes are inverted.

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PARALLEL OUTPUT DATA

Bit 1 (MSB) through Bit 12 (LSB), plus complement Bit 1, are the parallel output data lines provided by the ADC-00305II. Each signal can drive a minimum of 3 standard TTL loads. Parallel output data is valid during the time that the Data Ready line is HIGH. If a strobe signal is required to read the parallel output data into a register, the rising edge of the Data Ready signal can drive a minimum of 3 standard TTL loads.

OUTPUT REGISTERS & TRI-STATE BUFFERS

The ADC-00305II has data output storage registers which hold the most recently converted 12-bit word. The data is available at the output at all times, except for the initial 30 nsec of the interval when the Data Ready line is LOW. The ADC-00305II also has tri-state output buffers, for parallel data bus operation. The buffer outputs remain in a high-impedance state until an Enable signal is received. The buffers can be made transparent (constantly enabled) by holding the Enable signal LOW. Where possible the user should avoid digital activity on the tri-stated output during the Track to Hold transition. Should this be unavoidable, an external tri-state buffer should be used for isolation.

LAYOUT PRECAUTIONS

The ADC-00305II high-speed sampling A/D converter generates high-frequency power-supply and ground currents, and is sensitive to coupled signals. High-frequency layout considerations must therefore be kept in mind when designing a printed circuit board for it. All conductor lengths must be kept to a minimum, and a large-area ground-plane must be used to keep ground impedances as low as possible. Analog inputs and digital outputs must be kept separated from each other to minimize crosstalk. Input and output circuits must be kept as close to the A/D converter package as possible. Likewise, the three analog ground pins must be connected to the digital ground pin as close as possible to the hybrid package.

POWER SUPPLY DECOUPLING

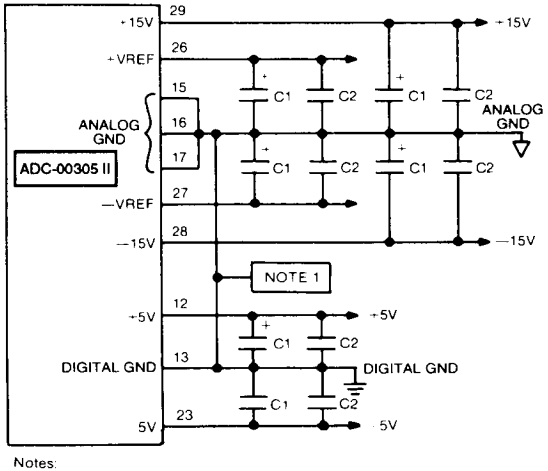
Decoupling capacitors are required on each power supply and both of the internal references to minimize noise. Figure 3 illustrates the recommended decoupling configuration. Each of the lines that is decoupled must have a 10 µF or larger tantalum capacitor in parallel with a 0.01 µF ceramic capacitor. All capacitors must be mounted as close as possible to the hybrid package.

OFFSET AND GAIN TRIMS

Gain and offset errors of the ADC-00305II are factory trimmed to be less than the values listed in Table 1, Specifications. Both gain and offset errors are trimmable to zero, with the use of external potentiometers. This affords the user with flexibility for maximizing performance for critical applications. Figures 4 and 5 show the external trim pot circuit required to trim gain and offset errors to zero. Multi-turn trim pots, with a temperature coefficient of less than 100 ppm/°C, are recommended for best results. If trim pots are not used, gain and offset adjust pins must be connected to analog ground.

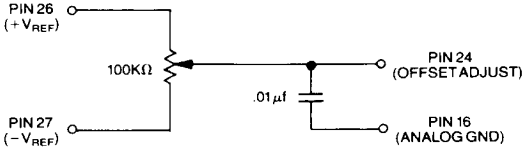
INTERNAL REFERENCE

The ADC-00305II contains +10V and -10V precision internal references, which are made available to the user. Care must be taken to observe the loading limitations on these references, to maintain rated performance. If the external load on either reference exceeds 2 mA, gain and linearity errors will increase. Damage will result from excessive loading.



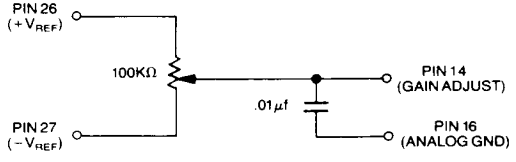
Notes:
(1) Analog ground and digital ground pins are to be connected together with a single short connection very close to the hybrid package.
(2) C1 is a 10µf or larger tantalum capacitor.
(3) C2 is a 0.01µf ceramic capacitor.

FIGURE 3. POWER SUPPLY DECOUPLING



Note:
If offset trim pot is not used, offset adjust (pin 24) must be connected to analog ground (pin 16).

FIGURE 4. OFFSET TRIM



Note:
If gain trim pot is not used, gain adjust (pin 14) must be connected to analog ground (pin 16).

FIGURE 5. GAIN TRIM

TABLE 4. ADC-00305II PIN FUNCTIONS			
PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	Bit 8	21	5V Range In
2	Bit 7	22	10V Range In
3	Bit 6	23	−5 V Supply
4	Bit 5	24	Offset Adjust
5	Bit 4	25	Range Offset
6	Bit 3	26	+10V Ref Out
7	Bit 2	27	−10V Ref Out
8	Bit 1 (MSB)	28	−15V Supply
9	Data Ready	29	+15V Supply
10	+5V Input *	30	NC (Factory Test Point)
11	NC (Factory Test Point)	31	MUX Enable
12	+5 V Supply	32	NC (Factory Test Point)
13	Digital Ground	33	NC (Factory Test Point)
14	Gain Adjust	34	Output Data Invert
15	Analog Ground	35	$\overline{\text{Bit 1}}$ ($\overline{\text{MSB}}$)
16	Analog Ground	36	Enable Data
17	Analog Ground	37	Bit 12 (LSB)
18	Encode Command	38	Bit 11
19	NC (Factory Test Point)	39	Bit 10
20	NC (Factory Test Point)	40	Bit 9

*External jumper to pin 12.

ORDERING INFORMATION

ADC- 00305II

Consult factory for ADC-00305-605 evaluation card.
Socket: Broadline SS-120-T-2 (or Samtec equivalent)

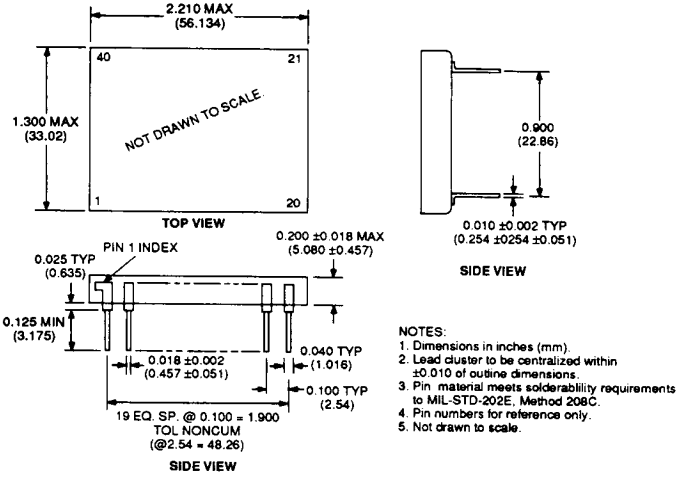


FIGURE 6. ADC-00305II MECHANICAL OUTLINE

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