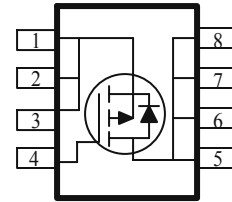


P-Channel 20-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize High Cell Density process. Low $r_{DS(on)}$ assures minimal power loss and conserves energy, making this device ideal for use in power management circuitry. Typical applications are PWMDC-DC converters, power management in portable and battery-powered products such as computers, printers, battery charger, telecommunication power system, and telephones power system.

- Low $r_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Miniature SO-8 Surface Mount Package Saves Board Space
- High power and current handling capability

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ m(Ω)	I_D (A)
-20	20 @ $V_{GS} = -4.5V$	10.2
	29 @ $V_{GS} = -2.5V$	8.5
	54 @ $V_{GS} = -1.8V$	6.2



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)				
Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	-20	V
Gate-Source Voltage		V_{GS}	± 12	
Continuous Drain Current ^a	$T_A = 25^\circ\text{C}$	I_D	10.2	A
	$T_A = 70^\circ\text{C}$		8.2	
Pulsed Drain Current ^b		I_{DM}	± 30	
Continuous Source Current (Diode Conduction) ^a		I_S	-2.3	A
Power Dissipation ^a	$T_A = 25^\circ\text{C}$	P_D	3.1	W
	$T_A = 70^\circ\text{C}$		2	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS				
Parameter		Symbol	Maximum	Units
Maximum Junction-to-Ambient ^a	$t \leq 10 \text{ sec}$	$R_{\theta JA}$	50	$^\circ\text{C/W}$
	Steady State		92	$^\circ\text{C/W}$

Notes

- Surface Mounted on 1" x 1" FR4 Board.
- Pulse width limited by maximum junction temperature

SPECIFICATIONS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Conditions	Limits			Unit
			Min	Typ	Max	
Static						
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = -350\text{ }\mu\text{A}$	-0.7			
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 12\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -16\text{ V}$, $V_{GS} = 0\text{ V}$			-1	μA
		$V_{DS} = -16\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 55^\circ\text{C}$			-10	
On-State Drain Current ^A	$I_{D(on)}$	$V_{DS} = -5\text{ V}$, $V_{GS} = -4.5\text{ V}$	-20			A
Drain-Source On-Resistance ^A	$r_{DS(on)}$	$V_{GS} = -4.5\text{ V}$, $I_D = -10.2\text{ A}$			20	m Ω
		$V_{GS} = -2.5\text{ V}$, $I_D = -8.5\text{ A}$			29	
		$V_{GS} = -1.8\text{ V}$, $I_D = -6.2\text{ A}$			54	
Forward Tranconductance ^A	g_{fs}	$V_{DS} = -10\text{ V}$, $I_D = -10.2\text{ A}$		36		S
Diode Forward Voltage	V_{SD}	$I_S = -2.3\text{ A}$, $V_{GS} = 0\text{ V}$		-0.8		V
Dynamic ^b						
Total Gate Charge	Q_g	$V_{DS} = -10\text{ V}$, $V_{GS} = -5\text{ V}$, $I_D = -10.2\text{ A}$		30		nC
Gate-Source Charge	Q_{gs}			4		
Gate-Drain Charge	Q_{gd}			6		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -10\text{ V}$, $R_L = 15\text{ }\Omega$, $I_D = -1\text{ A}$, $V_{GEN} = -5\text{ V}$, $R_G = 6\Omega$		25		nS
Rise Time	t_r			45		
Turn-Off Delay Time	$t_{d(off)}$			150		
Fall-Time	t_f			70		

Notes

- Pulse test: $PW \leq 300\text{us}$ duty cycle $\leq 2\%$.
- Guaranteed by design, not subject to production testing.

Analog Power (APL) reserves the right to make changes without further notice to any products herein. APL makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does APL assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in APL data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. APL does not convey any license under its patent rights nor the rights of others. APL products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the APL product could create a situation where personal injury or death may occur. Should Buyer purchase or use APL products for any such unintended or unauthorized application, Buyer shall indemnify and hold APL and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that APL was negligent regarding the design or manufacture of the part. APL is an Equal Opportunity/Affirmative Action Employer.

Typical Electrical Characteristics

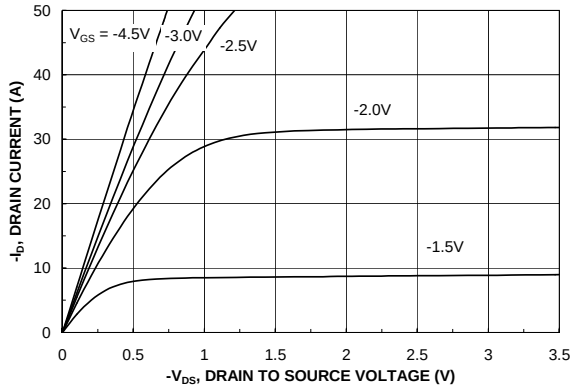


Figure 1. Output Characteristics

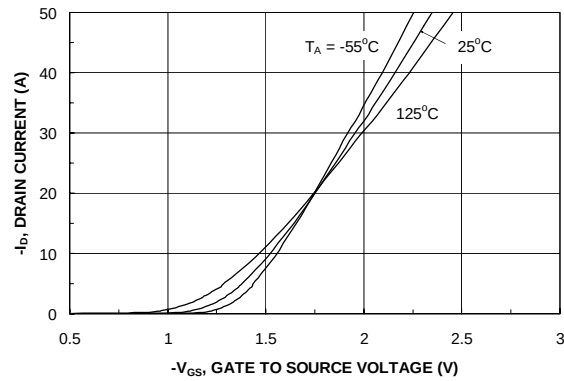


Figure 2. Transfer Characteristics

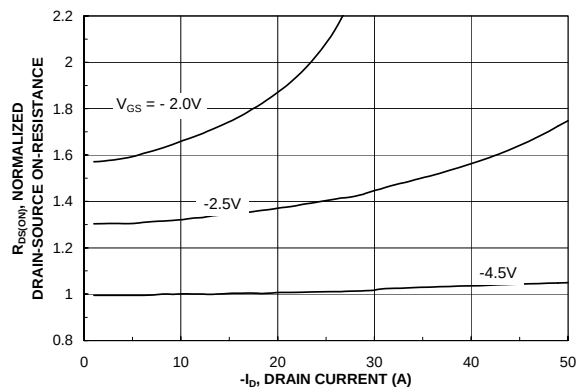


Figure 3. On Resistance vs. Drain Current

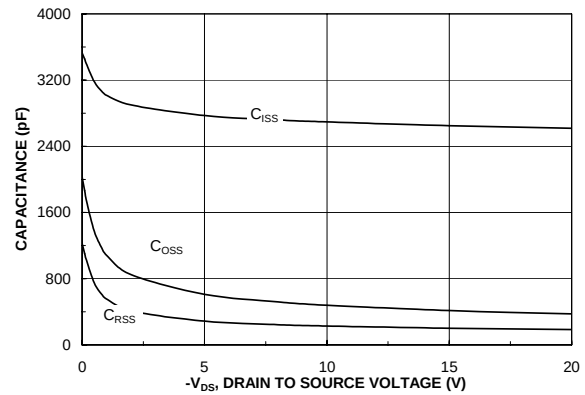


Figure 4. Capacitance

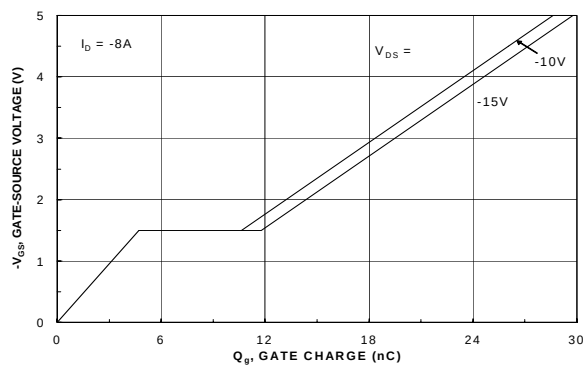


Figure 5. Gate Charge

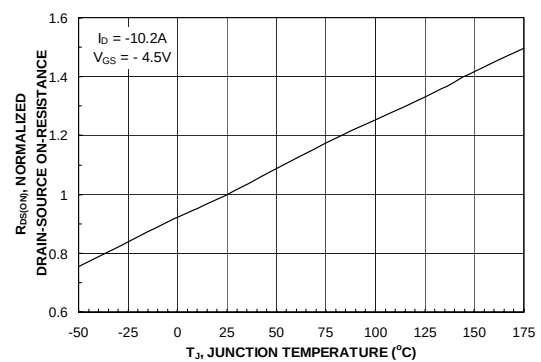


Figure 6. On-Resistance vs. Junction Temperature

Typical Electrical Characteristics

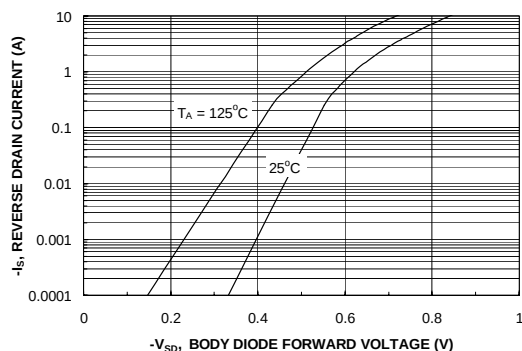


Figure 7. Source-Drain Diode Forward Voltage

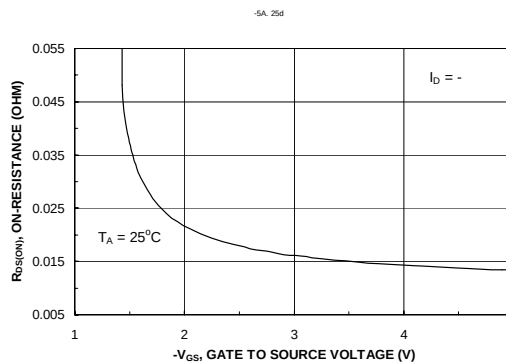


Figure 8. On-Resistance vs. Gate-to-Source Voltage

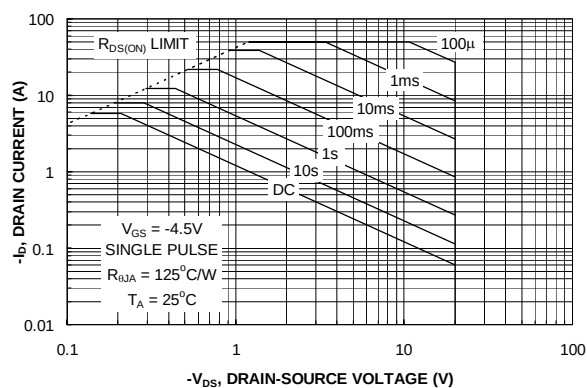


Figure 9. Safe Operating Area

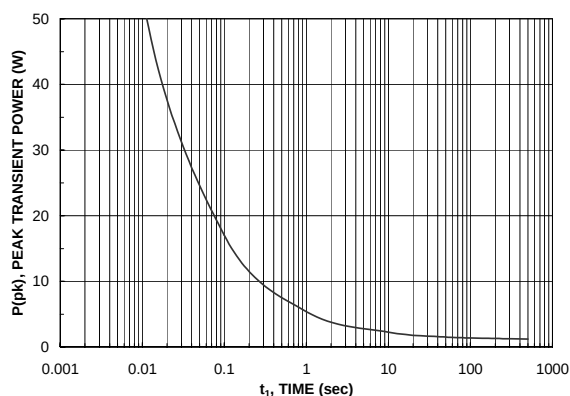


Figure 10. Single Pulse Power, Junction-to-Ambient

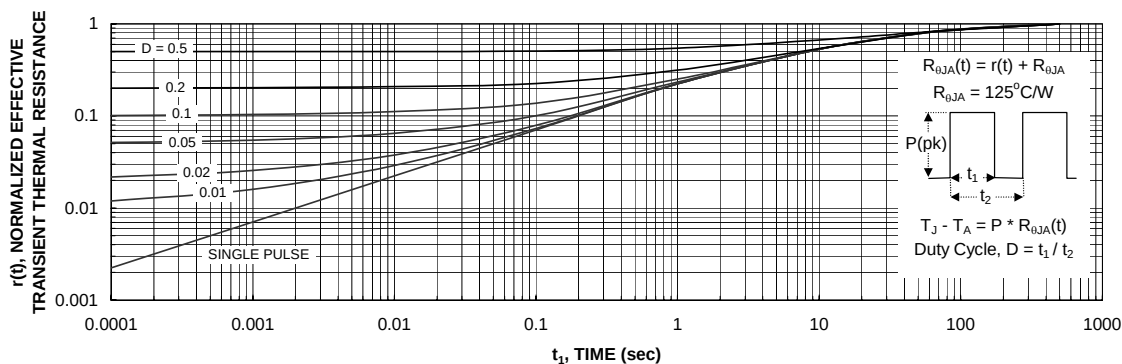
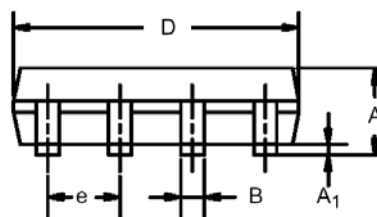
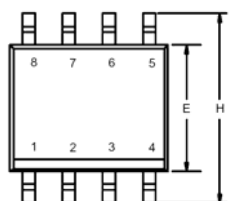


Figure 11. Normalized Thermal Transient Impedance, Junction-to-Ambient

Package Information

SO-8: 8LEAD



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A ₁	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°

