

64-pin CK505 w/Fully Integrated Voltage Regulator + Integrated Series Resistor

Recommended Application:

CK505 compliant clock with fully integrated voltage regulator and Internal series resistor on differential outputs

Output Features:

- 2 - CPU differential low power push-pull pairs
- 9 - SRC differential low power push-pull pairs
- 1 - CPU/SRC selectable differential low power push-pull pair
- 1 - SRC/DOT selectable differential low power push-pull pair
- 5 - PCI, 33MHz
- 1 - PCI_F, 33MHz free running
- 1 - USB, 48MHz
- 1 - REF, 14.318MHz

Key Specifications:

- CPU outputs cycle-cycle jitter < 85ps
- SRC output cycle-cycle jitter < 125ps
- PCI outputs cycle-cycle jitter < 250ps
- +/- 100ppm frequency accuracy on CPU & SRC clocks

Features/Benefits:

- Does not require external pass transistor for voltage regulator
- Integrated 33ohm series resistors on differential outputs, $Z_o=50\Omega$
- Supports spread spectrum modulation, default is 0.5% down spread
- Uses external 14.318MHz crystal, external crystal load caps are required for frequency tuning
- Selectable between one SRC differential push-pull pair and two single-ended outputs

| Pin Configuration | | | |
|-----------------------|----|----|--------------------|
| PCI0/CR#_A | 1 | 64 | SCLK |
| VDDPCI | 2 | 63 | SDATA |
| PCI1/CR#_B | 3 | 62 | REF0/FSLC/TEST_SEL |
| PCI2/TME | 4 | 61 | VDDREF |
| PCI3 | 5 | 60 | X1 |
| PCI4/27_Select | 6 | 59 | X2 |
| PCI_F5/ITP_EN | 7 | 58 | GNDREF |
| GNDPCI | 8 | 57 | FSLB/TEST_MODE |
| VDD48 | 9 | 56 | CK_PWRGD/PD# |
| USB_48MHz/FSLA | 10 | 55 | VDDCPU |
| GND48 | 11 | 54 | CPUTO |
| VDD96_IO | 12 | 53 | CPUC0 |
| SRCT0/DOTT_96 | 13 | 52 | GNDCPU |
| SRCC0/DOTC_96 | 14 | 51 | CPUT1_F |
| GND | 15 | 50 | CPUC1_F |
| VDDPLL3 | 16 | 49 | VDDCPU_IO |
| 27MHz_NonSS/SRCT1/SE1 | 17 | 48 | NC |
| 27MHz_SS/SRCC1/SE2 | 18 | 47 | CPUT2_ITP/SRCT8 |
| GND | 19 | 46 | CPUC2_ITP/SRCC8 |
| VDDPLL3_IO | 20 | 45 | VDDSRC_IO |
| SRCT2/SATAT | 21 | 44 | SRCT7/CR#_F |
| SRCC2/SATAC | 22 | 43 | SRCC7/CR#_E |
| GNDSRC | 23 | 42 | GNDSRC |
| SRCT3/CR#_C | 24 | 41 | SRCT6 |
| SRCC3/CR#_D | 25 | 40 | SRCC6 |
| VDDSRC_IO | 26 | 39 | VDDSRC |
| SRCT4 | 27 | 38 | PCI_STOP# |
| SRCC4 | 28 | 37 | CPU_STOP# |
| GNDSRC | 29 | 36 | VDDSRC_IO |
| SRCT9 | 30 | 35 | SRCC10 |
| SRCC9 | 31 | 34 | SRCT10 |
| SRCC11/CR#_G | 32 | 33 | SRCT11/CR#_H |

64-TSSOP

* Internal Pull-Up Resistor

** Internal Pull-Down Resistor

64-TSSOP

| 27_Select (power on latch) | 0 | 1 |
|----------------------------|----------------------------------|---|
| Pin13/14 & Pin17/18 | DOT96, LCD_SS Byte1 bit7 = 1. | SRCC0, 27MHz Non SS & SS Byte1 bit7 = 0. |

Table 1: CPU Frequency Select Table

| FS _L C ² B0b7 | FS _L B ¹ B0b6 | FS _L A ¹ B0b5 | CPU MHz | SRC MHz | PCI MHz | REF MHz | USB MHz | DOT MHz |
|--|--|--|------------|------------|------------|------------|------------|------------|
| 0 | 0 | 0 | 266.66 | 100.00 | 33.33 | 14.318 | 48.00 | 96.00 |
| 0 | 0 | 1 | 133.33 | | | | | |
| 0 | 1 | 0 | 200.00 | | | | | |
| 0 | 1 | 1 | 166.66 | | | | | |
| 1 | 0 | 0 | 333.33 | | | | | |
| 1 | 0 | 1 | 100.00 | | | | | |
| 1 | 1 | 0 | 400.00 | | | | | |
| 1 | 1 | 1 | Reserved | | | | | |

1. FS_LA and FS_LB are low-threshold inputs. Please see V_{IL_FS} and V_{IH_FS} specifications in the Input/Supply/Common Output Parameters Table for correct values.

Also refer to the Test Clarification Table.

2. FS_LC is a three-level input. Please see the V_{IL_FS} and V_{IH_FS} specifications in the Input/Supply/Common Output Parameters Table for correct values.



TSSOP Pin Description

| PIN # | PIN NAME | TYPE | DESCRIPTION |
|-------|----------------|------|---|
| 1 | PCI0/CR#_A | I/O | 3.3V PCI clock output or Clock Request control A for either SRC0 or SRC2 pair The power-up default is PCI0 output, but this pin may also be used as a Clock Request control of SRC pair 0 or SRC pair 2 via SMBus. Before configuring this pin as a Clock Request Pin, the PCI output must first be disabled in byte 2, bit 0 of SMBus address space. After the PCI output is disabled (high-Z), the pin can then be set to serve as a Clock Request pin for either SRC pair 2 or pair 0 using the CR#_A_EN bit located in byte 5 of SMBUs address space. Byte 5, bit 7 0 = PCI0 enabled (default) 1 = CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1 = CR#_A controls SRC2 pair |
| 2 | VDDPCI | PWR | Power supply pin for the PCI outputs, 3.3V nominal |
| 3 | PCI1/CR#_B | I/O | 3.3V PCI clock output/Clock Request control B for either SRC1 or SRC4 pair The power-up default is PCI1 output, but this pin may also be used as a Clock Request control of SRC pair 1 or SRC pair 4 via SMBus. Before configuring this pin as a Clock Request Pin, the PCI output must first be disabled in byte 2, bit 1 of SMBus address space. After the PCI output is disabled (high-Z), the pin can then be set to serve as a Clock Request pin for either SRC pair 1 or pair 4 using the CR#_B_EN bit located in byte 5 of SMBUs address space. Byte 5, bit 5 0 = PCI1 enabled (default) 1 = CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1 = CR#_B controls SRC4 pair |
| 4 | PCI2/TME | I/O | 3.3V PCI clock output / Trusted Mode Enable (TME) Latched Input. This pin is sampled on power-up as follows 0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed After being sampled on power-up, this pin becomes a 3.3V PCI Output |
| 5 | PCI3 | OUT | 3.3V PCI clock output. |
| 6 | PCI4/27_Select | I/O | 3.3V PCI clock output / 27MHz mode select for pin17, 18 strap. On powerup, the logic value on this pin determines the power-up default of DOT_96/SRC0 and 27MHz/SRC1 output and the function table for the pin17 and pin18. |
| 7 | PCI_F5/ITP_EN | I/O | Free running PCI clock output and ITP/SRC8 enable strap. This output is not affected by the state of the PCI_STOP# pin. On powerup, the state of this pin determines whether pins 46 and 47 are an ITP or SRC pair. 0 = SRC8/SRC8# 1 = ITP/ITP# |
| 8 | GNDPCI | PWR | Ground for PCI clocks. |
| 9 | VDD48 | PWR | Power supply for USB clock, nominal 3.3V. |
| 10 | USB_48MHz/FSLA | I/O | Fixed 48MHz USB clock output. 3.3V/ 3.3V tolerant input for CPU frequency selection. Refer to input electrical characteristics for Vil_FS and Vih_FS values. |
| 11 | GND48 | PWR | Ground pin for the 48MHz outputs. |
| 12 | VDD96_IO | PWR | 1.05V to 3.3V from external power supply |
| 13 | DOTT_96/SRCT0 | OUT | True clock of SRC or DOT96. The power-up default function depends on 27_Select, 1= SRC0, 0=DOT96 |
| 14 | DOTC_96/SRCC0 | OUT | Complement clock of SRC or DOT96. The power-up default function depends on 27_Select, 1= SRC0, 0=DOT96 |
| 15 | GND | PWR | Ground pin for the DOT96 clocks. |
| 16 | VDD | PWR | Power supply for SRC / SE1 and SE2 clocks, 3.3V nominal. |



TSSOP Pin Description (Continued)

| PIN # | PIN NAME | TYPE | DESCRIPTION |
|-------|-----------------------|------|---|
| 17 | 27MHz_NonSS/SRCT1/SE1 | OUT | True clock of differential SRC1 clock pair / 3.3V single-ended output. 27_Select determines the power-up default, 1=27MHz non-spread SE clock, 0 = LCD_SST 100MHz differential clock. See table 2 for more information. |
| 18 | 27MHz_SS/SRCC1/SE2 | OUT | Complement clock of differential SRC1 clock pair / 3.3V single-ended output. 27_Select determines the power-up default, 1=27MHz spread SE clock, 0 = LCD_SSC 100MHz differential clock. See table 2 for more information. |
| 19 | GND | PWR | Ground pin for SRC / SE1 and SE2 clocks, PLL3. |
| 20 | VDDPLL3_IO | PWR | 1.05V to 3.3V from external power supply |
| 21 | SRCT2/SATAT | OUT | True clock of differential SRC/SATA clock pair. |
| 22 | SRCC2/SATAC | OUT | Complement clock of differential SRC/SATA clock pair. |
| 23 | GNDSRC | PWR | Ground pin for SRC clocks. |
| 24 | SRCT3/CR#_C | I/O | True clock of differential SRC clock pair/ Clock Request control C for either SRC0 or SRC2 pair The power-up default is SRCCLK3 output, but this pin may also be used as a Clock Request control of SRC pair 0 or SRC pair 2 via SMBus. Before configuring this pin as a Clock Request Pin, the SRC3 output must first be disabled in byte 4, bit 7 of SMBus address space . After the SRC3 output is disabled, the pin can then be set to serve as a Clock Request pin for either SRC pair 2 or pair 0 using the CR#_C_EN bit located in byte 5 of SMBUs address space. Byte 5, bit 3 0 = SRC3 enabled (default) 1= CR#_C enabled. Byte 5, bit 2 controls whether CR#_C controls SRC0 or SRC2 pair Byte 5, bit 2 0 = CR#_C controls SRC0 pair (default), 1= CR#_C controls SRC2 pair |
| 25 | SRCC3/CR#_D | I/O | Complementary clock of differential SRC clock pair/ Clock Request control D for either SRC1 or SRC4 pair The power-up default is SRCCLK3 output, but this pin may also be used as a Clock Request control of SRC pair 1 or SRC pair 4 via SMBus. Before configuring this pin as a Clock Request Pin, the SRC3 output must first be disabled in byte 4, bit 7 of SMBus address space . After the SRC3 output is disabled, the pin can then be set to serve as a Clock Request pin for either SRC pair 1 or pair 4 using the CR#_D_EN bit located in byte 5 of SMBUs address space. Byte 5, bit 1 0 = SRC3 enabled (default) 1= CR#_D enabled. Byte 5, bit 0 controls whether CR#_D controls SRC1 or SRC4 pair Byte 5, bit 0 0 = CR#_D controls SRC1 pair (default), 1= CR#_D controls SRC4 pair |
| 26 | VDDSRC_IO | PWR | 1.05V to 3.3V from external power supply |
| 27 | SRCT4 | I/O | True clock of differential SRC clock pair 4 |
| 28 | SRCC4 | I/O | Complement clock of differential SRC clock pair 4 |
| 29 | GNDSRC | PWR | Ground pin for SRC clocks. |
| 30 | SRCT9 | OUT | True clock of differential SRC clock pair. |
| 31 | SRCC9 | OUT | Complement clock of differential SRC clock pair. |
| 32 | SRCC11/CR#_G | I/O | SRC11 complement /Clock Request control for SRC9 pair The power-up default is SRC11#, but this pin may also be used as a Clock Request control of SRC9 via SMBus. Before configuring this pin as a Clock Request Pin, the SRC11 output pair must first be disabled in byte 3, bit 7 of SMBus configuration space After the SRC11 output is disabled (high-Z), the pin can then be set to serve as a Clock Request for SRC9 pair using byte 6, bit 5 of SMBus configuration space Byte 6, bit 5 0 = SRC11# enabled (default) 1= CR#_G controls SRC9 |



TSSOP Pin Description (Continued)

| PIN # | PIN NAME | TYPE | DESCRIPTION |
|-------|-----------------|------|---|
| 33 | SRCT11/CR#_H | I/O | SRC11 true or Clock Request control H for SRC10 pair The power-up default is SRC11, but this pin may also be used as a Clock Request control of SRC10 via SMBus. Before configuring this pin as a Clock Request Pin, the SRC11 output pair must first be disabled in byte 3, bit 7 of SMBus configuration space After the SRC11 output is disabled (high-Z), the pin can then be set to serve as a Clock Request for SRC10 pair using byte 6, bit 4 of SMBus configuration space Byte 6, bit 4 0 = SRC11 enabled (default) 1 = CR#_H controls SRC10. |
| 34 | SRCT10 | OUT | True clock of differential SRC clock pair. |
| 35 | SRCC10 | OUT | Complement clock of differential SRC clock pair. |
| 36 | VDDSRC_IO | PWR | 1.05V to 3.3V from external power supply |
| 37 | CPU_STOP# | IN | Stops all CPU Clocks, except those set to be free running clocks. In AMT mode 3 bits are shifted in from the ICH to set the FSC, FSB, FSA values |
| 38 | PCI_STOP# | IN | Stops all PCI Clocks, except those set to be free running clocks. In AMT mode 3 bits are shifted in from the ICH to set the FSC, FSB, FSA values |
| 39 | VDDSRC | PWR | VDD pin for SRC Pre-drivers, 3.3V nominal |
| 40 | SRCC6 | OUT | Complement clock of low power differential SRC clock pair. |
| 41 | SRCT6 | OUT | True clock of low power differential SRC clock pair. |
| 42 | GNDSRC | PWR | Ground for SRC clocks |
| 43 | SRCC7/CR#_E | I/O | SRC7 complement or Clock Request control E for SRC6 pair The power-up default is SRC7#, but this pin may also be used as a Clock Request control of SRC6 via SMBus. Before configuring this pin as a Clock Request Pin, the SRC7 output pair must first be disabled in byte 3, bit 3 of SMBus configuration space . After the SRC output is disabled (high-Z), the pin can then be set to serve as a Clock Request for SRC6 pair using byte 6, bit 7 of SMBus configuration space Byte 6, bit 7 0 = SRC7# enabled (default) 1 = CR#_E controls SRC6. |
| 44 | SRCT7/CR#_F | I/O | SRC7 true or Clock Request control 8 for SRC8 pair The power-up default is SRC7, but this pin may also be used as a Clock Request control of SRC8 via SMBus. Before configuring this pin as a Clock Request Pin, the SRC7 output pair must first be disabled in byte 3, bit 3 of SMBus configuration space After the SRC output is disabled (high-Z), the pin can then be set to serve as a Clock Request for SRC8 pair using byte 6, bit 6 of SMBus configuration space Byte 6, bit 6 0 = SRC7# enabled (default) 1 = CR#_F controls SRC8. |
| 45 | VDDSRC_IO | PWR | 1.05V to 3.3V from external power supply |
| 46 | CPUC2_ITP/SRCC8 | OUT | Complement clock of low power differential CPU2/Complement clock of differential SRC pair. The function of this pin is determined by the latched input value on pin 7, PCIF5/ITP_EN on powerup. The function is as follows: Pin 7 latched input Value 0 = SRC8# 1 = ITP# |
| 47 | CPUT2_ITP/SRCT8 | OUT | True clock of low power differential CPU2/True clock of differential SRC pair. The function of this pin is determined by the latched input value on pin 7, PCIF5/ITP_EN on powerup. The function is as follows: Pin 7 latched input Value 0 = SRC8 1 = ITP |
| 48 | NC | N/A | No Connect |

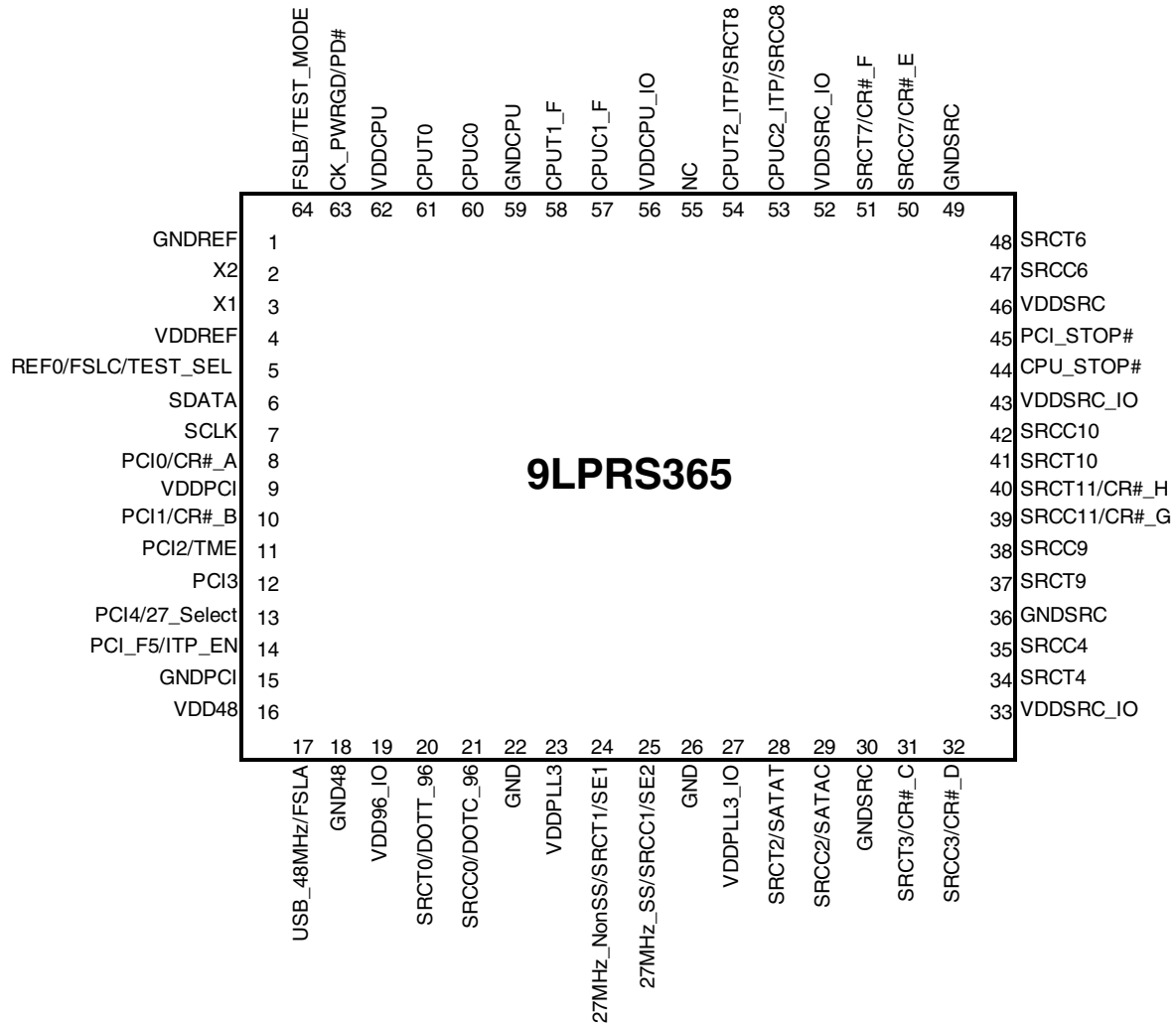


TSSOP Pin Description (Continued)

| PIN # | PIN NAME | TYPE | DESCRIPTION |
|-------|--------------------|------|--|
| 49 | VDDCPU_IO | PWR | 1.05V to 3.3V from external power supply |
| 50 | CPUC1_F | OUT | Complement clock of low power differential CPU clock pair. This clock will be free-running during iAMT. |
| 51 | CPUT1_F | OUT | True clock of low power differential CPU clock pair. This clock will be free-running during iAMT. |
| 52 | GNDCPU | PWR | Ground Pin for CPU Outputs |
| 53 | CPUC0 | OUT | Complement clock of low power differential CPU clock pair. |
| 54 | CPUT0 | OUT | True clock of low power differential CPU clock pair. |
| 55 | VDDCPU | PWR | Power Supply 3.3V nominal. |
| 56 | CK_PWRGD/PD# | IN | Notifies CK505 to sample latched inputs, or iAMT entry/exit, or PWRDWN# mode |
| 57 | FSLB/TEST_MODE | IN | 3.3V tolerant input for CPU frequency selection. Refer to input electrical characteristics for Vi_FS and Vih_FS values. TEST_MODE is a real time input to select between Hi-Z and REF/N divider mode while in test mode. Refer to Test Clarification Table. |
| 58 | GNDREF | PWR | Ground pin for crystal oscillator circuit |
| 59 | X2 | OUT | Crystal output, nominally 14.318MHz. |
| 60 | X1 | IN | Crystal input, Nominally 14.318MHz. |
| 61 | VDDREF | PWR | Power pin for the REF outputs, 3.3V nominal. |
| 62 | REF0/FSLC/TEST_SEL | I/O | 3.3V 14.318MHz reference clock/3.3V tolerant low threshold input for CPU frequency selection. Refer to input electrical characteristics for Vi_FS and Vih_FS values/ TEST_SEL: 3-level latched input to enable test mode. Refer to Test Clarification Table. |
| 63 | SDATA | I/O | Data pin for SMBus circuitry, 5V tolerant. |
| 64 | SCLK | IN | Clock pin of SMBus circuitry, 5V tolerant. |



Pin Configuration



64-pin MLF

64-MLF

| 27_Select (power on latch) | 0 | 1 |
|----------------------------|---------------------------------|---|
| Pin20/21 & Pin24/25 | DOT96, LCD_SS Byte1 bit7 = 1 | SRC0, 27MHz Non SS & SS Byte1 bit7= 0. |

MLF Pin Description

| PIN # | PIN NAME | TYPE | DESCRIPTION |
|-------|--------------------|------|--|
| 1 | GNDREF | PWR | Ground pin for crystal oscillator circuit |
| 2 | X2 | OUT | Crystal output, nominally 14.318MHz. |
| 3 | X1 | IN | Crystal input, Nominally 14.318MHz. |
| 4 | VDDREF | PWR | Power pin for the REF outputs, 3.3V nominal. |
| 5 | REF0/FSLC/TEST_SEL | I/O | 3.3V 14.318MHz reference clock/3.3V tolerant low threshold input for CPU frequency selection. Refer to input electrical characteristics for V_{il_FS} and V_{ih_FS} values/ TEST_SEL: 3-level latched input to enable test mode. Refer to Test Clarification Table. |
| 6 | SDATA | I/O | Data pin for SMBus circuitry, 5V tolerant. |
| 7 | SCLK | IN | Clock pin of SMBus circuitry, 5V tolerant. |
| 8 | PCI0/CR#_A | I/O | 3.3V PCI clock output or Clock Request control A for either SRC0 or SRC2 pair The power-up default is PCI0 output, but this pin may also be used as a Clock Request control of SRC pair 0 or SRC pair 2 via SMBus. Before configuring this pin as a Clock Request Pin, the PCI output must first be disabled in byte 2, bit 0 of SMBus address space . After the PCI output is disabled (high-Z), the pin can then be set to serve as a Clock Request pin for either SRC pair 2 or pair 0 using the CR#_A_EN bit located in byte 5 of SMBUs address space. Byte 5, bit 7 0 = PCI0 enabled (default) 1= CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1= CR#_A controls SRC2 pair |
| 9 | VDDPCI | PWR | Power supply pin for the PCI outputs, 3.3V nominal |
| 10 | PCI1/CR#_B | I/O | 3.3V PCI clock output/Clock Request control B for either SRC1 or SRC4 pair The power-up default is PCI1 output, but this pin may also be used as a Clock Request control of SRC pair 1 or SRC pair 4 via SMBus. Before configuring this pin as a Clock Request Pin, the PCI output must first be disabled in byte 2, bit 1 of SMBus address space . After the PCI output is disabled (high-Z), the pin can then be set to serve as a Clock Request pin for either SRC pair 1 or pair 4 using the CR#_B_EN bit located in byte 5 of SMBUs address space. Byte 5, bit 5 0 = PCI1 enabled (default) 1= CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1= CR#_B controls SRC4 pair |
| 11 | PCI2/TME | I/O | 3.3V PCI clock output / Trusted Mode Enable (TME) Latched Input. This pin is sampled on power-up as follows 0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC <u>NOT</u> allowed After being sampled on power-up, this pin becomes a 3.3V PCI Output |
| 12 | PCI3 | OUT | 3.3V PCI clock output. |
| 13 | PCI4/27_Select | I/O | 3.3V PCI clock output / 27MH mode select for pin24, 25 strap. On powerup, the logic value on this pin determines the power-up default of DOT_96/SRC0 and 27MHz/SRC1 output and the function talbe for the pin24 and pin25. |
| 14 | PCI_F5/ITP_EN | I/O | Free running PCI clock output and ITP/SRC8 enable strap. This output is not affected by the state of the PCI_STOP# pin. On powerup, the state of this pin determines whether pins 53 and 54 are an ITP or SRC pair. 0 =SRC8/SRC8# 1 = ITP/ITP# |
| 15 | GNDPCI | PWR | Ground for PCI clocks. |
| 16 | VDD48 | PWR | Power supply for USB clock, nominal 3.3V. |

MLF Pin Description (Continued)

| PIN # | PIN NAME | TYPE | DESCRIPTION |
|-------|-----------------------|------|---|
| 17 | USB_48MHz/FSLA | I/O | Fixed 48MHz USB clock output. 3.3V/ 3.3V tolerant input for CPU frequency selection. Refer to input electrical characteristics for Vil_FS and Vih_FS values. |
| 18 | GND48 | PWR | Ground pin for the 48MHz outputs. |
| 19 | VDD96_IO | PWR | 1.05V to 3.3V from external power supply |
| 20 | DOTT_96/SRCT0 | OUT | True clock of SRC or DOT96. The power-up default function depends on 27_Select, 1= SRC0, 0=DOT96 |
| 21 | DOTC_96/SRCC0 | OUT | Complement clock of SRC or DOT96. The power-up default function depends on 27_Select, 1= SRC0, 0=DOT96 |
| 22 | GND | PWR | Ground pin for the DOT96 clocks. |
| 23 | VDD | PWR | Power supply for SRC / SE1 and SE2 clocks, 3.3V nominal. |
| 24 | 27MHz_NonSS/SRCT1/SE1 | OUT | True clock of differential SRC1 clock pair / 3.3V single-ended output. 27_Select determines the power-up default, 1=27MHz non-spread SE clock, 0 = LCD_SST 100MHz differential clock. See table 2 for more information. |
| 25 | 27MHz_SS/SRCC1/SE2 | OUT | Complement clock of differential SRC1 clock pair / 3.3V single-ended output. 27_Select determines the power-up default, 1=27MHz spread SE clock, 0 = LCD_SSC 100MHz differential clock. See table 2 for more information. |
| 26 | GND | PWR | Ground pin for SRC / SE1 and SE2 clocks, PLL3. |
| 27 | VDDPLL3_IO | PWR | 1.05V to 3.3V from external power supply |
| 28 | SRCT2/SATAT | OUT | True clock of differential SRC/SATA clock pair. |
| 29 | SRCC2/SATAC | OUT | Complement clock of differential SRC/SATA clock pair. |
| 30 | GNDSRC | PWR | Ground pin for SRC clocks. |
| 31 | SRCT3/CR#_C | I/O | <p>True clock of differential SRC clock pair/ Clock Request control C for either SRC0 or SRC2 pair The power-up default is SRCCLK3 output, but this pin may also be used as a Clock Request control of SRC pair 0 or SRC pair 2 via SMBus. Before configuring this pin as a Clock Request Pin, the SRC3 output must first be disabled in byte 4, bit 7 of SMBus address space . After the SRC3 output is disabled, the pin can then be set to serve as a Clock Request pin for either SRC pair 2 or pair 0 using the CR#_C_EN bit located in byte 5 of SMBUs address space.</p> <p>Byte 5, bit 3 0 = SRC3 enabled (default) 1= CR#_C enabled. Byte 5, bit 2 controls whether CR#_C controls SRC0 or SRC2 pair</p> <p>Byte 5, bit 2 0 = CR#_C controls SRC0 pair (default), 1= CR#_C controls SRC2 pair</p> |
| 32 | SRCC3/CR#_D | I/O | <p>Complementary clock of differential SRC clock pair/ Clock Request control D for either SRC1 or SRC4 pair The power-up default is SRCCLK3 output, but this pin may also be used as a Clock Request control of SRC pair 1 or SRC pair 4 via SMBus. Before configuring this pin as a Clock Request Pin, the SRC3 output must first be disabled in byte 4, bit 7 of SMBus address space . After the SRC3 output is disabled, the pin can then be set to serve as a Clock Request pin for either SRC pair 1 or pair 4 using the CR#_D_EN bit located in byte 5 of SMBUs address space.</p> <p>Byte 5, bit 1 0 = SRC3 enabled (default) 1= CR#_D enabled. Byte 5, bit 0 controls whether CR#_D controls SRC1 or SRC4 pair</p> <p>Byte 5, bit 0 0 = CR#_D controls SRC1 pair (default), 1= CR#_D controls SRC4 pair</p> |

MLF Pin Description (Continued)

| PIN # | PIN NAME | TYPE | DESCRIPTION |
|-------|--------------|------|--|
| 33 | VDDSRC_IO | PWR | 1.05V to 3.3V from external power supply |
| 34 | SRCT4 | I/O | True clock of differential SRC clock pair 4 |
| 35 | SRCC4 | I/O | Complement clock of differential SRC clock pair 4 |
| 36 | GNDSRC | PWR | Ground pin for SRC clocks. |
| 37 | SRCT9 | OUT | True clock of differential SRC clock pair. |
| 38 | SRCC9 | OUT | Complement clock of differential SRC clock pair. |
| 39 | SRCC11/CR#_G | I/O | <p>SRC11 complement /Clock Request control for SRC9 pair The power-up default is SRC11#, but this pin may also be used as a Clock Request control of SRC9 via SMBus. Before configuring this pin as a Clock Request Pin, the SRC11 output pair must first be disabled in byte 3, bit 7 of SMBus configuration space After the SRC11 output is disabled (high-Z), the pin can then be set to serve as a Clock Request for SRC9 pair using byte 6, bit 5 of SMBus configuration space</p> <p>Byte 6, bit 5 0 = SRC11# enabled (default) 1 = CR#_G controls SRC9</p> |
| 40 | SRCT11/CR#_H | I/O | <p>SRC11 true or Clock Request control H for SRC10 pair The power-up default is SRC11, but this pin may also be used as a Clock Request control of SRC10 via SMBus. Before configuring this pin as a Clock Request Pin, the SRC11 output pair must first be disabled in byte 3, bit 7 of SMBus configuration space After the SRC11 output is disabled (high-Z), the pin can then be set to serve as a Clock Request for SRC10 pair using byte 6, bit 4 of SMBus configuration space</p> <p>Byte 6, bit 4 0 = SRC11 enabled (default) 1 = CR#_H controls SRC10.</p> |
| 41 | SRCT10 | OUT | True clock of differential SRC clock pair. |
| 42 | SRCC10 | OUT | Complement clock of differential SRC clock pair. |
| 43 | VDDSRC_IO | PWR | 1.05V to 3.3V from external power supply |
| 44 | CPU_STOP# | IN | Stops all CPU Clocks, except those set to be free running clocks. In AMT mode 3 bits are shifted in from the ICH to set the FSC, FSB, FSA values |
| 45 | PCI_STOP# | IN | Stops all PCI Clocks, except those set to be free running clocks. In AMT mode 3 bits are shifted in from the ICH to set the FSC, FSB, FSA values |
| 46 | VDDSRC | PWR | VDD pin for SRC Pre-drivers, 3.3V nominal |
| 47 | SRCC6 | OUT | Complement clock of low power differential SRC clock pair. |
| 48 | SRCT6 | OUT | True clock of low power differential SRC clock pair. |

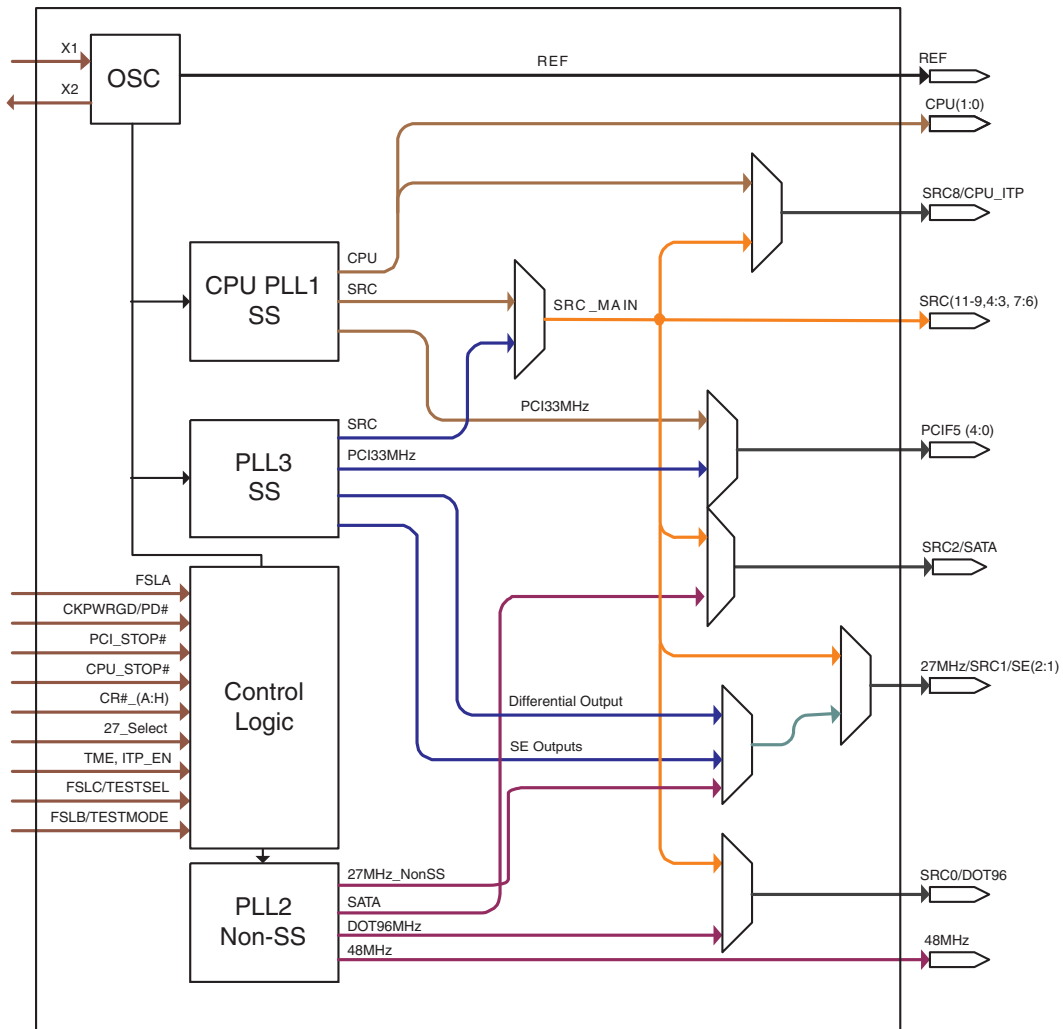
MLF Pin Description (Continued)

| PIN # | PIN NAME | TYPE | DESCRIPTION |
|-------|-----------------|------|--|
| 49 | GNDSRC | PWR | Ground for SRC clocks |
| 50 | SRCC7/CR#_E | I/O | SRC7 complement or Clock Request control E for SRC6 pair The power-up default is SRC7#, but this pin may also be used as a Clock Request control of SRC6 via SMBus. Before configuring this pin as a Clock Request Pin, the SRC7 output pair must first be disabled in byte 3, bit 3 of SMBus configuration space. After the SRC output is disabled (high-Z), the pin can then be set to serve as a Clock Request for SRC6 pair using byte 6, bit 7 of SMBus configuration space Byte 6, bit 7 0 = SRC7# enabled (default) 1 = CR#_E controls SRC6. |
| 51 | SRCT7/CR#_F | I/O | SRC7 true or Clock Request control 8 for SRC8 pair The power-up default is SRC7, but this pin may also be used as a Clock Request control of SRC8 via SMBus. Before configuring this pin as a Clock Request Pin, the SRC7 output pair must first be disabled in byte 3, bit 3 of SMBus configuration space. After the SRC output is disabled (high-Z), the pin can then be set to serve as a Clock Request for SRC8 pair using byte 6, bit 6 of SMBus configuration space Byte 6, bit 6 0 = SRC7# enabled (default) 1 = CR#_F controls SRC8. |
| 52 | VDDSRC_IO | PWR | 1.05V to 3.3V from external power supply |
| 53 | CPUC2_ITP/SRCC8 | OUT | Complement clock of low power differential CPU2/Complement clock of differential SRC pair. The function of this pin is determined by the latched input value on pin 7, PCIF5/ITP_EN on powerup. The function is as follows: Pin 7 latched input Value 0 = SRC8# 1 = ITP# |
| 54 | CPUT2_ITP/SRCT8 | OUT | True clock of low power differential CPU2/True clock of differential SRC pair. The function of this pin is determined by the latched input value on pin 7, PCIF5/ITP_EN on powerup. The function is as follows: Pin 7 latched input Value 0 = SRC8 1 = ITP |
| 55 | NC | N/A | No Connect |
| 56 | VDDCPU_IO | PWR | 1.05V to 3.3V from external power supply |
| 57 | CPUC1_F | OUT | Complement clock of low power differential CPU clock pair. This clock will be free-running during iAMT. |
| 58 | CPUT1_F | OUT | True clock of low power differential CPU clock pair. This clock will be free-running during iAMT. |
| 59 | GNDCPU | PWR | Ground Pin for CPU Outputs |
| 60 | CPUC0 | OUT | Complement clock of low power differential CPU clock pair. |
| 61 | CPUT0 | OUT | True clock of low power differential CPU clock pair. |
| 62 | VDDCPU | PWR | Power Supply 3.3V nominal. |
| 63 | CK_PWRGD/PD# | IN | Notifies CK505 to sample latched inputs, or iAMT entry/exit, or PWRDWN# mode |
| 64 | FSLB/TEST_MODE | IN | 3.3V tolerant input for CPU frequency selection. Refer to input electrical characteristics for V_{iL_FS} and V_{iH_FS} values. TEST_MODE is a real time input to select between Hi-Z and REF/N divider mode while in test mode. Refer to Test Clarification Table. |

General Description

ICS9LPRS365 follows Intel CK505 Yellow Cover specification. This clock synthesizer provides a single chip solution for next generation P4 Intel processors and Intel chipsets. ICS9LPRS365 is driven with a 14.318MHz crystal. It also provides a tight ppm accuracy output for Serial ATA and PCI-Express support.

Block Diagram



Power Groups

| Pin Number | | Description | |
|------------|------------|----------------------|-------------------|
| VDD | GND | | |
| 49 | 52 | CPUCLK | Low power outputs |
| 55 | 52 | Master Clock, Analog | |
| 26, 36, 45 | 23, 29, 42 | SRCCLK | Low power outputs |
| 39 | 23, 29, 42 | | PLL 1 |
| 20 | 19 | PLL3/SE | Low power outputs |
| 16 | 19 | | PLL 3 |
| 12 | 11 | DOT 96Mhz | Low power outputs |
| 9 | 11 | USB 48 | |
| 61 | 58 | Xtal, REF | |
| 2 | 8 | PCICLK | |

Absolute Maximum Ratings

| PARAMETER | SYMBOL | CONDITIONS | MIN | MAX | UNITS | Notes |
|------------------------|-------------------|-------------------------------------|-----------|-----|-------|-------|
| Maximum Supply Voltage | VDDxxx | Core/Logic Supply | | 4.6 | V | 1,2 |
| Maximum Supply Voltage | VDDxxx_IO | Low Voltage Differential I/O Supply | | 3.8 | V | 1,2 |
| Maximum Input Voltage | V _{IH} | 3.3V LVCMOS Inputs | | 4.6 | V | 1,2,3 |
| Minimum Input Voltage | V _{IL} | Any Input | GND - 0.5 | | V | 1,2 |
| Storage Temperature | T _s | - | -65 | 150 | °C | 1,2 |
| Case Temperature | T _{case} | - | | 115 | °C | 1,2 |
| Input ESD protection | ESD prot | Human Body Model | 2000 | | V | 1,2 |

¹Guaranteed by design and characterization, not 100% tested in production.

²Operation under these conditions is neither implied, nor guaranteed.

³Maximum input voltage is not to exceed maximum VDD

Electrical Characteristics - Input/Supply/Common Output Parameters

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYPICAL | MAX | UNITS | Notes |
|--|-------------------------|--|-----------------------|---------|-----------------------|-------|-------|
| Ambient Operating Temp | T _{ambient} | - | 0 | | 70 | °C | 1 |
| Supply Voltage | VDDxxx | Supply Voltage | 3.135 | | 3.465 | V | 1 |
| Supply Voltage | VDDxxx_IO | Low-Voltage Differential I/O Supply | 1 | | 3.465 | V | 1 |
| Input High Voltage | V _{IHSE} | Single-ended inputs | 2 | | V _{DD} + 0.3 | V | 1 |
| Input Low Voltage | V _{ILSE} | Single-ended inputs | V _{SS} - 0.3 | | 0.8 | V | 1 |
| Input Leakage Current | I _{IN} | V _{IN} = V _{DD} , V _{IN} = GND | -5 | | 5 | uA | 1 |
| Input Leakage Current | I _{INRES} | Inputs with pull or pull down resistors V _{IN} = V _{DD} , V _{IN} = GND | -200 | | 200 | uA | 1 |
| Output High Voltage | V _{OHSE} | Single-ended outputs, I _{OH} = -1mA | 2.4 | | | V | 1 |
| Output Low Voltage | V _{OLSE} | Single-ended outputs, I _{OL} = 1 mA | | | 0.4 | V | 1 |
| Output High Voltage | V _{OHDF} | Differential Outputs, I _{OH} = TBD mA | 0.7 | | 0.9 | V | 1 |
| Output Low Voltage | V _{OLDF} | Differential Outputs, I _{OL} = TBD mA | | | 0.4 | V | 1 |
| Low Threshold Input-High Voltage (Test Mode) | V _{IH_FS_TEST} | 3.3 V +/-5% | 2 | | V _{DD} + 0.3 | V | 1 |
| Low Threshold Input-High Voltage | V _{IH_FS} | 3.3 V +/-5% | 0.7 | | 1.5 | V | 1 |
| Low Threshold Input-Low Voltage | V _{IL_FS} | 3.3 V +/-5% | V _{SS} - 0.3 | | 0.35 | V | 1 |
| Operating Supply Current | I _{DD_DEFAULT} | 3.3V supply, PLL3 off | | 95 | 250 | mA | 1 |
| | I _{DD_PLL3DIF} | 3.3V supply, PLL3 Differential Out | | 106 | 250 | mA | 1 |
| | I _{DD_PLL3SE} | 3.3V supply, PLL3 Single-ended Out | | 101 | 250 | mA | 1 |
| | I _{DD_IO} | 0.8V supply, Differential IO current, all outputs enabled | 25 | 32 | 80 | mA | 1 |
| Power Down Current | I _{DD_PD3.3} | 3.3V supply, Power Down Mode | | 26 | 30 | mA | 1 |
| | I _{DD_PDIO} | 0.8V IO supply, Power Down Mode | | 0.23 | 0.5 | mA | 1 |
| iAMT Mode Current | I _{DD_IAMT3.3} | 3.3V supply, iAMT Mode | | 47 | 80 | mA | 1 |
| | I _{DD_IAMT0.8} | 0.8V IO supply, iAMT Mode | | 5 | 10 | mA | 1 |
| Input Frequency | F _i | V _{DD} = 3.3 V | | | 14.318 | MHz | 1 |
| Pin Inductance | L _{pin} | | | | 7 | nH | 1 |
| Input Capacitance | C _{IN} | Logic Inputs | 1.5 | | 5 | pF | 1 |
| | C _{OUT} | Output pin capacitance | | | 6 | pF | 1 |
| | C _{INX} | X1 & X2 pins | | | 5 | pF | 1 |
| Spread Spectrum Modulation Frequency | f _{SSMOD} | Triangular Modulation | 30 | | 33 | kHz | 1 |

*T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%

¹Guaranteed by design and characterization, not 100% tested in production.

Electrical Characteristics - SMBus Interface

| PARAMETER | SYMBOL | CONDITIONS | MIN | MAX | UNITS | Notes |
|---|--------------------|---|-----|------|-------|-------|
| SMBus Voltage | V_{DD} | | 2.7 | 5.5 | V | 1 |
| Low-level Output Voltage | $V_{OL\text{SMB}}$ | @ I_{PULLUP} | | 0.4 | V | 1 |
| Current sinking at $V_{OL\text{SMB}} = 0.4\text{ V}$ | I_{PULLUP} | SMB Data Pin | 4 | | mA | 1 |
| SCLK/SDATA Clock/Data Rise Time | T_{RI2C} | (Max $V_{IL} - 0.15$) to (Min $V_{IH} + 0.15$) | | 1000 | ns | 1 |
| SCLK/SDATA Clock/Data Fall Time | T_{FI2C} | (Min $V_{IH} + 0.15$) to (Max $V_{IL} - 0.15$) | | 300 | ns | 1 |
| Maximum SMBus Operating Frequency | F_{SMBUS} | Block Mode | | 100 | kHz | 1 |

¹Guaranteed by design and characterization, not 100% tested in production.

AC Electrical Characteristics - Input/Common Parameters

| PARAMETER | SYMBOL | CONDITIONS | MIN | MAX | UNITS | Notes |
|-------------------|--------------------|---|-----|-----|-------|-------|
| Clk Stabilization | T_{STAB} | From VDD Power-Up or de-assertion of PD# to 1st clock | | 1.8 | ms | 1 |
| Tdrive_SRC | T_{DRSRC} | SRC output enable after PCI_STOP# de-assertion | | 15 | ns | 1,2 |
| Tdrive_PD# | T_{DRPD} | Differential output enable after PD# de-assertion | | 300 | us | 1 |
| Tdrive_CPU | T_{DRSRC} | CPU output enable after CPU_STOP# de-assertion | | 10 | ns | 1,2 |
| Tfall_PD# | T_{FALL} | Fall/rise time of PD#, PCI_STOP# and CPU_STOP# inputs | | 5 | ns | 1,2 |
| Trise_PD# | T_{RISE} | | | 5 | ns | 1,2 |

¹Guaranteed by design and characterization, not 100% tested in production.

²Optional. Only applies when PCI_STOP# and/or CPU_STOP# is present.

AC Electrical Characteristics - Low Power Differential Outputs

| PARAMETER | SYMBOL | CONDITIONS | MIN | MAX | UNITS | NOTES |
|-----------------------------|------------------------------|--------------------------|------|------|-------|-------|
| Rising Edge Slew Rate | t_{SLR} | Differential Measurement | 2.5 | 8 | V/ns | 1,2 |
| Falling Edge Slew Rate | t_{FLR} | Differential Measurement | 2.5 | 8 | V/ns | 1,2 |
| Slew Rate Variation | t_{SLVAR} | Single-ended Measurement | | 20 | % | 1 |
| Maximum Output Voltage | V_{HIGH} | Includes overshoot | | 1150 | mV | 1 |
| Minimum Output Voltage | V_{LOW} | Includes undershoot | -300 | | mV | 1 |
| Differential Voltage Swing | V_{SWING} | Differential Measurement | 300 | | mV | 1 |
| Crossing Point Voltage | V_{XABS} | Single-ended Measurement | 300 | 550 | mV | 1,3,4 |
| Crossing Point Variation | V_{XABSVAR} | Single-ended Measurement | | 140 | mV | 1,3,5 |
| Duty Cycle | D_{CYC} | Differential Measurement | 45 | 55 | % | 1 |
| CPU Jitter - Cycle to Cycle | CPUJ_{C2C} | Differential Measurement | | 85 | ps | 1 |
| SRC Jitter - Cycle to Cycle | SRCJ_{C2C} | Differential Measurement | | 125 | ps | 1 |
| DOT Jitter - Cycle to Cycle | DOTJ_{C2C} | Differential Measurement | | 250 | ps | 1 |
| CPU[1:0] Skew | $\text{CPU}_{\text{SKEW10}}$ | Differential Measurement | | 100 | ps | 1 |
| CPU[2..ITP:0] Skew | $\text{CPU}_{\text{SKEW20}}$ | Differential Measurement | | 150 | ps | 1 |
| SRC[10:0] Skew | SRC_{SKEW} | Differential Measurement | | TBD | ps | 1 |

* $T_A = 0 - 70^\circ\text{C}$; $V_{DD} = 3.3\text{ V} \pm 5\%$; $C_L = 5\text{pF}$, $R_S = 22\Omega$ (unless specified otherwise.)

¹Guaranteed by design and characterization, not 100% tested in production.

²Slew rate measured through V_{swing} centered around differential zero

³ V_{xabs} is defined as the voltage where $\text{CLK} = \text{CLK}\#$

⁴Only applies to the differential rising edge (CLK rising and CLK# falling)

⁵Defined as the total variation of all crossing voltages of CLK rising and CLK# falling. Matching applies to rising edge rate of CLK and falling edge of CLK#.

Electrical Characteristics - PCICLK/PCICLK_F

| PARAMETER | SYMBOL | CONDITIONS | MIN | MAX | UNITS | NOTES |
|---------------------------|----------------------|--|-------------|----------|-------|-------|
| Long Accuracy | ppm | see T _{period} min-max values | -300 | 300 | ppm | 1,2 |
| Clock period | T _{period} | 33.33MHz output nominal | 29.99100 | 30.00900 | ns | 2 |
| | | 33.33MHz output spread | | 30.15980 | ns | 2 |
| Absolute min/max period | T _{abs} | 33.33MHz output nominal/spread | 29.49100 | 30.65980 | ns | 2 |
| Output High Voltage | V _{OH} | I _{OH} = -1 mA | 2.4 | | V | 1 |
| Output Low Voltage | V _{OL} | I _{OL} = 1 mA | | 0.4 | V | 1 |
| Output High Current | I _{OH} | V _{OH} @ MIN = 1.0 V | -33 | | mA | 1 |
| | | V _{OH} @ MAX = 3.135 V | | -33 | mA | 1 |
| Output Low Current | I _{OL} | V _{OL} @ MIN = 1.95 V | 30 | | mA | 1 |
| | | V _{OL} @ MAX = 0.4 V | | 38 | mA | 1 |
| Rising Edge Slew Rate | t _{SLR} | Measured from 0.8 to 2.0 V | 1 | 4 | V/ns | 1 |
| Falling Edge Slew Rate | t _{FLR} | Measured from 2.0 to 0.8 V | 1 | 4 | V/ns | 1 |
| Duty Cycle | d _{TI} | V _T = 1.5 V | 45 | 55 | % | 1 |
| Skew | t _{skew} | V _T = 1.5 V | | 250 | ps | 1 |
| Intentional PCI-PCI delay | t _{delay} | V _T = 1.5 V | 200 nominal | | ps | 1,3 |
| Jitter, Cycle to cycle | t _{jyc-cyc} | V _T = 1.5 V | | 500 | ps | 1 |

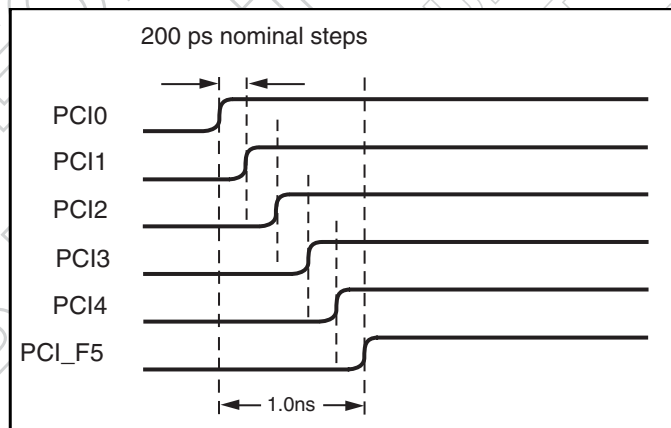
*T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%

¹Guaranteed by design and characterization, not 100% tested in production.

²All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

³See PCI Clock-to-Clock Delay Figure

Intentional PCI Clock to Clock Delay



Electrical Characteristics - USB48MHz

| PARAMETER | SYMBOL | CONDITIONS | MIN | MAX | UNITS | NOTES |
|-------------------------|---------------|---|----------|----------|-------|-------|
| Long Accuracy | ppm | see Tperiod min-max values | -100 | 100 | ppm | 1,2 |
| Clock period | T_{period} | 48.00MHz output nominal | 20.83125 | 20.83542 | ns | 2 |
| Absolute min/max period | T_{abs} | 48.00MHz output nominal | 20.48130 | 21.18540 | ns | 2 |
| Output High Voltage | V_{OH} | $I_{OH} = -1 \text{ mA}$ | 2.4 | | V | 1 |
| Output Low Voltage | V_{OL} | $I_{OL} = 1 \text{ mA}$ | | 0.4 | V | 1 |
| Output High Current | I_{OH} | $V_{OH} @ \text{MIN} = 1.0 \text{ V}$ | -29 | | mA | 1 |
| | | $V_{OH} @ \text{MAX} = 3.135 \text{ V}$ | | -23 | mA | 1 |
| Output Low Current | I_{OL} | $V_{OL} @ \text{MIN} = 1.95 \text{ V}$ | 29 | | mA | 1 |
| | | $V_{OL} @ \text{MAX} = 0.4 \text{ V}$ | | 27 | mA | 1 |
| Rising Edge Slew Rate | t_{SLR} | Measured from 0.8 to 2.0 V | 1 | 2 | V/ns | 1 |
| Falling Edge Slew Rate | t_{FLR} | Measured from 2.0 to 0.8 V | 1 | 2 | V/ns | 1 |
| Duty Cycle | d_{TT} | $V_T = 1.5 \text{ V}$ | 45 | 55 | % | 1 |
| Jitter, Cycle to cycle | $t_{cyc-cyc}$ | $V_T = 1.5 \text{ V}$ | | 350 | ps | 1 |

¹ Guaranteed by design and characterization, not 100% tested in production.

² All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

Electrical Characteristics - SE 24.576MHz

| PARAMETER | SYMBOL | CONDITIONS | MIN | MAX | UNITS | NOTES |
|------------------------|---------------|---|----------|----------|-------|-------|
| Long Accuracy | ppm | see Tperiod min-max values | -300 | 300 | ppm | 1,2 |
| Clock period | T_{period} | 24.576MHz output nominal | 40.70231 | 40.67790 | ns | 2 |
| Output High Voltage | V_{OH} | $I_{OH} = -1 \text{ mA}$ | 2.4 | | V | 1 |
| Output Low Voltage | V_{OL} | $I_{OL} = 1 \text{ mA}$ | | 0.4 | V | 1 |
| Output High Current | I_{OH} | $V_{OH} @ \text{MIN} = 1.0 \text{ V}$ | -29 | | mA | 1 |
| | | $V_{OH} @ \text{MAX} = 3.135 \text{ V}$ | | -23 | mA | 1 |
| Output Low Current | I_{OL} | $V_{OL} @ \text{MIN} = 1.95 \text{ V}$ | 29 | | mA | 1 |
| | | $V_{OL} @ \text{MAX} = 0.4 \text{ V}$ | | 27 | mA | 1 |
| Rising Edge Slew Rate | t_{SLR} | Measured from 0.8 to 2.0 V | 1 | 4 | V/ns | 1 |
| Falling Edge Slew Rate | t_{FLR} | Measured from 2.0 to 0.8 V | 1 | 4 | V/ns | 1 |
| Duty Cycle | d_{TT} | $V_T = 1.5 \text{ V}$ | 45 | 55 | % | 1 |
| Jitter, Cycle to cycle | $t_{cyc-cyc}$ | $V_T = 1.5 \text{ V}$ | | 500 | ps | 1 |

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%

¹ Guaranteed by design and characterization, not 100% tested in production.

² All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

Electrical Characteristics - REF-14.318MHz

| PARAMETER | SYMBOL | CONDITIONS | MIN | MAX | UNITS | Notes |
|-------------------------|----------------------|---|---------|----------|-------|-------|
| Long Accuracy | ppm | see T _{period} min-max values | -300 | 300 | ppm | 1,2 |
| Clock period | T _{period} | 14.318MHz output nominal | 69.8203 | 69.8622 | ns | 2 |
| Absolute min/max period | T _{abs} | 14.318MHz output nominal | 69.8203 | 70.86224 | ns | 2 |
| Output High Voltage | V _{OH} | I _{OH} = -1 mA | 2.4 | | V | 1 |
| Output Low Voltage | V _{OL} | I _{OL} = 1 mA | | 0.4 | V | 1 |
| Output High Current | I _{OH} | V _{OH} @ MIN = 1.0 V, V _{OH} @ MAX = 3.135 V | -33 | -33 | mA | 1 |
| Output Low Current | I _{OL} | V _{OL} @ MIN = 1.95 V, V _{OL} @ MAX = 0.4 V | 30 | 38 | mA | 1 |
| Rising Edge Slew Rate | t _{SLR} | Measured from 0.8 to 2.0 V | 1 | 4 | V/ns | 1 |
| Falling Edge Slew Rate | t _{FLR} | Measured from 2.0 to 0.8 V | 1 | 4 | V/ns | 1 |
| Duty Cycle | d _{tt} | V _T = 1.5 V | 45 | 55 | % | 1 |
| Jitter | t _{jcy-cyc} | V _T = 1.5 V | | 1000 | ps | 1 |

¹ Guaranteed by design and characterization, not 100% tested in production.

² All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

Preferred drive strengths using CK505 clock sources.

Transmission lines to load do not share series resistors.

Desktop (Z_o=50Ω) and mobile (Z_o=55Ω) have the same drive strength.

| D.C. Drive Strength | Number of Loads to Drive | Match Point for N & P Voltage / Current (mA) | Number of Loads Actually Driven. [Z _o =55Ω] | | |
|---------------------|--------------------------|--|--|--------------------------|--------------------------|
| | | | 1 Load R _s = | 2 Loads R _s = | 3 Loads R _s = |
| | 1 | 0.56 / 33 (17Ω) | 33Ω [39Ω] | - | - |
| | 2 | 0.92 / 66 (14Ω) | 39Ω [43Ω] | 22Ω [27Ω] | - |
| | 3 | 1.15 / 99 (11.6Ω) | 43Ω [43Ω] | 27Ω [33Ω] | 15Ω [22Ω] |



Table 1: CPU Frequency Select Table

| FS _L C ² B0b7 | FS _L B ¹ B0b6 | FS _L A ¹ B0b5 | CPU MHz | SRC MHz | PCI MHz | REF MHz | USB MHz | DOT MHz |
|--|--|--|------------|------------|------------|------------|------------|------------|
| 0 | 0 | 0 | 266.66 | 100.00 | 33.33 | 14.318 | 48.00 | 96.00 |
| 0 | 0 | 1 | 133.33 | | | | | |
| 0 | 1 | 0 | 200.00 | | | | | |
| 0 | 1 | 1 | 166.66 | | | | | |
| 1 | 0 | 0 | 333.33 | | | | | |
| 1 | 0 | 1 | 100.00 | | | | | |
| 1 | 1 | 0 | 400.00 | | | | | |
| 1 | 1 | 1 | Reserved | | | | | |

- FS_LA and FS_LB are low-threshold inputs. Please see V_{IL_FS} and V_{IH_FS} specifications in the Input/Supply/Common Output Parameters Table for correct values.
Also refer to the Test Clarification Table.
- FS_LC is a three-level input. Please see the V_{IL_FS} and V_{IH_FS} specifications in the Input/Supply/Common Output Parameters Table for correct values.

Table 2: PLL3 Quick Configuration

| B1b4 | B1b3 | B1b2 | B1b1 | Pin17 (TSSOP) / Pin24 (MLF) | Pin18 (TSSOP) / Pin25 (MLF) | Spread | Comment |
|------|------|------|------|--------------------------------|--------------------------------|------------------|------------------------------------|
| | | | | MHz | MHz | % | |
| 0 | 0 | 0 | 0 | PLL 3 disabled | | | |
| 0 | 0 | 0 | 1 | 100.00 | 100.00 | 0.5% Down Spread | SRCCLK1 from SRC_MAIN |
| 0 | 0 | 1 | 0 | 100.00 | 100.00 | 0.5% Down Spread | Only SRCCLK1 from PLL3 |
| 0 | 0 | 1 | 1 | 100.00 | 100.00 | 1% Down Spread | Only SRCCLK1 from PLL3 |
| 0 | 1 | 0 | 0 | 100.00 | 100.00 | 1.5% Down Spread | Only SRCCLK1 from PLL3 |
| 0 | 1 | 0 | 1 | 100.00 | 100.00 | 2% Down Spread | Only SRCCLK1 from PLL3 |
| 0 | 1 | 1 | 0 | 100.00 | 100.00 | 2.5% Down Spread | Only SRCCLK1 from PLL3 |
| 0 | 1 | 1 | 1 | N/A | N/A | N/A | N/A |
| 1 | 0 | 0 | 0 | 24.576 | 24.576 | None | 24.576Mhz on SE1 and SE2 |
| 1 | 0 | 0 | 1 | 24.576 | 98.304 | None | 24.576Mhz on SE1, 98.304Mhz on SE2 |
| 1 | 0 | 1 | 0 | 98.304 | 98.304 | None | 98.304Mhz on SE1 and SE2 |
| 1 | 0 | 1 | 1 | 27.000 | 27.000 | None | 27Mhz on SE1 and SE2 |
| 1 | 1 | 0 | 0 | 25.000 | 25.000 | None | 25Mhz on SE1 and SE2 |
| 1 | 1 | 0 | 1 | N/A | N/A | N/A | N/A |
| 1 | 1 | 1 | 0 | N/A | N/A | N/A | N/A |
| 1 | 1 | 1 | 1 | N/A | N/A | N/A | N/A |



Table 3: IO_Vout select table

| B9b2 | B9b1 | B9b0 | IO_Vout |
|------|------|------|---------|
| 0 | 0 | 0 | 0.3V |
| 0 | 0 | 1 | 0.4V |
| 0 | 1 | 0 | 0.5V |
| 0 | 1 | 1 | 0.6V |
| 1 | 0 | 0 | 0.7V |
| 1 | 0 | 1 | 0.8V |
| 1 | 1 | 0 | 0.9V |
| 1 | 1 | 1 | 1.0V |

CPU Power Management Table

| PD# | CPU_STOP# | PCI_STOP# | CR# | SMBus Register OE | CPU1 | CPU1# | CPU(0,2) | CPU(0,2)# |
|-----------|-----------|-----------|-----|-------------------|---------|---------|----------|-----------|
| 1 | 1 | 1 | X | Enable | Running | Running | Running | Running |
| 0 | X | X | X | Enable | Low/20K | Low | Low/20K | Low |
| 1 | 0 | X | X | Enable | High | Low | High | Low |
| 1 | X | X | X | Disable | Low/20K | Low | Low/20K | Low |
| M1 | | | | | Running | Running | Low/20K | Low |

SRC, LCD, DOT Power Management Table

| PD# | CPU_STOP# | PCI_STOP# | CR# | SMBus Register OE | SRC/LCD | SRC#/LCD# | SRC/LCD | SRC#/LCD# | DOT | DOT# |
|-----------|-----------|-----------|-----|-------------------|----------|-----------|---------------------------|-----------|---------|---------|
| | | | | | Free-Run | | PCI Stoppable/CR Selected | | | |
| 1 | X | 1 | 0 | Enable | Running | Running | Running | Running | Running | Running |
| 0 | X | X | X | Enable | Low/20K | Low | Low/20K | Low | Low/20K | Low |
| 1 | X | 0 | X | Enable | Running | Running | High | Low | Running | Running |
| 1 | X | X | 1 | Enable | Running | Running | Low/20K | Low | Running | Running |
| 1 | X | X | X | Disable | Low/20K | Low | Low/20K | Low | Low/20K | Low |
| M1 | | | | | Low/20K | Low | Low/20K | Low | Low/20K | Low |

Singled-ended Power Management Table

| PD# | CPU_STOP# | PCI_STOP# | CR# | SMBus Register OE | PCIF/PCI | PCIF/PCI | USB | REF |
|-----------|-----------|-----------|-----|-------------------|----------|-----------|---------|---------|
| | | | | | Free-run | Stoppable | | |
| 1 | X | 1 | X | Enable | Running | Running | Running | Running |
| 0 | X | X | X | Enable | Low | Low | Low | Low |
| 1 | X | 0 | X | Enable | Running | Low | Running | Running |
| 1 | X | X | X | Disable | Low | Low | Low | Low |
| M1 | | | | | Low | Low | Low | Low |

General SMBus serial interface information for the ICS9LPRS365

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2_(H)
- ICS clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- ICS clock will **acknowledge**
- Controller (host) sends the data byte count = X
- ICS clock will **acknowledge**
- Controller (host) starts sending **Byte N through Byte N + X - 1**
- ICS clock will **acknowledge** each byte **one at a time**
- Controller (host) sends a Stop bit

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address D2_(H)
- ICS clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- ICS clock will **acknowledge**
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address D3_(H)
- ICS clock will **acknowledge**
- ICS clock will send the data byte count = X
- ICS clock sends **Byte N + X - 1**
- ICS clock sends **Byte 0 through byte X (if X_(H) was written to byte 8).**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

| Index Block Write Operation | | |
|---------------------------------|-----------|----------------------|
| Controller (Host) | | ICS (Slave/Receiver) |
| T | starT bit | |
| Slave Address D2 _(H) | | |
| WR | WRite | |
| | | ACK |
| Beginning Byte = N | | |
| | | ACK |
| Data Byte Count = X | | |
| | | ACK |
| Beginning Byte N | | X Byte |
| ○ | | |
| ○ | | |
| ○ | | |
| Byte N + X - 1 | | |
| | | ACK |
| P | stoP bit | |

| Index Block Read Operation | | |
|---------------------------------|-----------------|----------------------|
| Controller (Host) | | ICS (Slave/Receiver) |
| T | starT bit | |
| Slave Address D2 _(H) | | |
| WR | WRite | |
| | | ACK |
| Beginning Byte = N | | |
| | | ACK |
| RT | Repeat starT | |
| Slave Address D3 _(H) | | |
| RD | ReaD | |
| | | ACK |
| | | Data Byte Count = X |
| ACK | | X Byte |
| ACK | | |
| ○ | | |
| ○ | | |
| ○ | | |
| | | Byte N + X - 1 |
| N | Not acknowledge | |
| P | stoP bit | |

Byte 0 FS Readback and PLL Selection Register

| Bit | Pin | Name | Description | Type | 0 | 1 | Default |
|-----|-----|--------------|--|-----------------|--|---------------------|---------|
| 7 | - | FSLC | CPU Freq. Sel. Bit (Most Significant) | R | See Table 1 : CPU Frequency Select Table | | Latch |
| 6 | - | FSLB | CPU Freq. Sel. Bit | R | | | Latch |
| 5 | - | FSLA | CPU Freq. Sel. Bit (Least Significant) | R | | | Latch |
| 4 | - | iAMT_EN | Set via SMBus or dynamically by CK505 if detects dynamic M1 | RW (Sticky Bit) | Legacy Mode | iAMT Enabled | 0 |
| 3 | | Reserved | Reserved | RW | | | 0 |
| 2 | - | SRC_Main_SEL | Select source for SRC Main | RW | SRC Main = PLL1 | SRC Main = PLL3 | 0 |
| 1 | - | SATA_SEL | Select source for SATA clock | RW | SATA = SRC_Main | SATA = PLL2 | 0 |
| 0 | - | PD_Restore | If config saved, on deassert return to last known state else clear all config as if cold power on and go to latches open state | RW | Configuration Not Saved | Configuration Saved | 1 |

Byte 1 DOT96 Select and PLL3 Quick Config Register

| Bit | Pin | Name | Description | Type | 0 | 1 | Default |
|-----|-------|--------------|--------------------------------|------|---|---------------|---------|
| 7 | 13/14 | SRC0_SEL | Select SRC0 or DOT96 | R | SRC0 | DOT96 | Note 1 |
| 6 | - | PLL1_SSC_SEL | Select 0.5% down or center SSC | RW | Down spread | Center spread | 0 |
| 5 | | Reserved | | RW | | | 0 |
| 4 | 17/18 | PLL3_CF3 | PLL3 Quick Config Bit 3 | RW | See Table 2: pin17, 18 Configuration Only applies if Byte 0, bit 2 = 0. | | 0 |
| 3 | | PLL3_CF2 | PLL3 Quick Config Bit 2 | RW | | | 0 |
| 2 | | PLL3_CF1 | PLL3 Quick Config Bit 1 | RW | | | 1 |
| 1 | | PLL3_CF0 | PLL3 Quick Config Bit 0 | RW | | | 0 |
| 0 | | PCI_SEL | PCI_SEL | RW | PCI from PLL1 | PCI from PLL3 | 1 |

Note 1 : When 27_Select pin = 0, B1b7 PWD = 1, , when 27_Select pin = 1, PWD = 0

Byte 2 Output Enable Register

| Bit | Pin | Name | Description | Type | 0 | 1 | Default |
|-----|-----|---------|---|------|-----------------|----------------|---------|
| 7 | | REF_OE | Output enable for REF, if disabled output is tri-stated | RW | Output Disabled | Output Enabled | 1 |
| 6 | | USB_OE | Output enable for USB | RW | Output Disabled | Output Enabled | 1 |
| 5 | | PCI5_OE | Output enable for PCI5 | RW | Output Disabled | Output Enabled | 1 |
| 4 | | PCI4_OE | Output enable for PCI4 | RW | Output Disabled | Output Enabled | 1 |
| 3 | | PCI3_OE | Output enable for PCI3 | RW | Output Disabled | Output Enabled | 1 |
| 2 | | PCI2_OE | Output enable for PCI2 | RW | Output Disabled | Output Enabled | 1 |
| 1 | | PCI1_OE | Output enable for PCI1 | RW | Output Disabled | Output Enabled | 1 |
| 0 | | PCI0_OE | Output enable for PCI0 | RW | Output Disabled | Output Enabled | 1 |

Byte 3 Output Enable Register

| Bit | Pin | Name | Description | Type | 0 | 1 | Default |
|-----|-----|-------------|-------------------------------|------|-----------------|----------------|---------|
| 7 | | SRC11_OE | Output enable for SRC11 | RW | Output Disabled | Output Enabled | 1 |
| 6 | | SRC10_OE | Output enable for SRC10 | RW | Output Disabled | Output Enabled | 1 |
| 5 | | SRC9_OE | Output enable for SRC9 | RW | Output Disabled | Output Enabled | 1 |
| 4 | | SRC8/ITP_OE | Output enable for SRC8 or ITP | RW | Output Disabled | Output Enabled | 1 |
| 3 | | SRC7_OE | Output enable for SRC7 | RW | Output Disabled | Output Enabled | 1 |
| 2 | | SRC6_OE | Output enable for SRC6 | RW | Output Disabled | Output Enabled | 1 |
| 1 | | Reserved | Reserved | RW | Output Disabled | Output Enabled | 1 |
| 0 | | SRC4_OE | Output enable for SRC4 | RW | Output Disabled | Output Enabled | 1 |

Byte 4 Output Enable and Spread Spectrum Disable Register

| Bit | Pin | Name | Description | Type | 0 | 1 | Default |
|-----|-----|---------------|---------------------------------|------|-----------------|----------------|---------|
| 7 | | SRC3_OE | Output enable for SRC3 | RW | Output Disabled | Output Enabled | 1 |
| 6 | | SATA/SRC2_OE | Output enable for SATA/SRC2 | RW | Output Disabled | Output Enabled | 1 |
| 5 | | SRC1_OE | Output enable for SRC1 | RW | Output Disabled | Output Enabled | 1 |
| 4 | | SRC0/DOT96_OE | Output enable for SRC0/DOT96 | RW | Output Disabled | Output Enabled | 1 |
| 3 | | CPU1_OE | Output enable for CPU1 | RW | Output Disabled | Output Enabled | 1 |
| 2 | | CPU0_OE | Output enable for CPU0 | RW | Output Disabled | Output Enabled | 1 |
| 1 | | PLL1_SSC_ON | Enable PLL1's spread modulation | RW | Spread Disabled | Spread Enabled | 1 |
| 0 | | PLL3_SSC_ON | Enable PLL3's spread modulation | RW | Spread Disabled | Spread Enabled | 1 |

Byte 5 Clock Request Enable/Configuration Register

| Bit | Pin | Name | Description | Type | 0 | 1 | Default |
|-----|-----|-----------|--|------|---------------|---------------|---------|
| 7 | | CR#_A_EN | Enable CR#_A (clk req), PCI0_OE must be = 0 for this bit to take effect | RW | Disable CR#_A | Enable CR#_A | 0 |
| 6 | | CR#_A_SEL | Sets CR#_A to control either SRC0 or SRC2 | RW | CR#_A -> SRC0 | CR#_A -> SRC2 | 0 |
| 5 | | CR#_B_EN | Enable CR#_B (clk req) | RW | Disable CR#_B | Enable CR#_B | 0 |
| 4 | | CR#_B_SEL | Sets CR#_B -> SRC1 or SRC4 | RW | CR#_B -> SRC1 | CR#_B -> SRC4 | 0 |
| 3 | | CR#_C_EN | Enable CR#_C (clk req) | RW | Disable CR#_C | Enable CR#_C | 0 |
| 2 | | CR#_C_SEL | Sets CR#_C -> SRC0 or SRC2 | RW | CR#_C -> SRC0 | CR#_C -> SRC2 | 0 |
| 1 | | CR#_D_EN | Enable CR#_D (clk req) | RW | Disable CR#_D | Enable CR#_D | 0 |
| 0 | | CR#_D_SEL | Sets CR#_D -> SRC1 or SRC4 | RW | CR#_D -> SRC1 | CR#_D -> SRC4 | 0 |

Byte 6 Clock Request Enable/Configuration and Stop Control Register

| Bit | Pin | Name | Description | Type | 0 | 1 | Default |
|-----|-----|---------------|-------------------------------------|------|---------------|--------------------------------------|---------|
| 7 | | CR#_E_EN | Enable CR#_E (clk req) -> SRC6 | RW | Disable CR#_E | Enable CR#_E | 0 |
| 6 | | CR#_F_EN | Enable CR#_F (clk req) -> SRC8 | RW | Disable CR#_F | Enable CR#_F | 0 |
| 5 | | CR#_G_EN | Enable CR#_G (clk req) -> SRC9 | RW | Disable CR#_G | Enable CR#_G | 0 |
| 4 | | CR#_H_EN | Enable CR#_H (clk req) -> SRC10 | RW | Disable CR#_H | Enable CR#_H | 0 |
| 3 | | Reserved | Reserved | RW | | | 0 |
| 2 | | Reserved | Reserved | RW | | | 0 |
| 1 | | SSCD_STP_CRTL | If set, LCD_SS stops with PCI_STOP# | RW | Free Running | Stops with PCI_STOP# assertion | 0 |
| 0 | | SRC_STP_CRTL | If set, SRCs stop with PCI_STOP# | RW | Free Running | Stops with PCI_STOP# assertion | 0 |

Byte 7 Vendor ID/ Revision ID

| Bit | Pin | Name | Description | Type | 0 | 1 | Default |
|-----|-----|-----------------|----------------------------------|------|-----------------|---|---------|
| 7 | | Rev Code Bit 3 | Revision ID | R | Vendor specific | | 0 |
| 6 | | Rev Code Bit 2 | | R | | | 0 |
| 5 | | Rev Code Bit 1 | | R | | | 1 |
| 4 | | Rev Code Bit 0 | | R | | | 0 |
| 3 | | Vendor ID bit 3 | Vendor ID ICS is 0001, binary | R | | | 0 |
| 2 | | Vendor ID bit 2 | | R | | | 0 |
| 1 | | Vendor ID bit 1 | | R | | | 0 |
| 0 | | Vendor ID bit 0 | | R | | | 1 |

Byte 8 Device ID and Output Enable Register

| Bit | Pin | Name | Description | Type | 0 | 1 | Default |
|-----|-----|------------|--|------|---------------------|---------|--------------------------|
| 7 | | Device_ID3 | Table of Device identifier codes, used for differentiating between CK505 package options, etc. | R | See Device ID Table | | 1 |
| 6 | | Device_ID2 | | R | | | 1 |
| 5 | | Device_ID1 | | R | | | 0 |
| 4 | | Device_ID0 | | R | | | 1 |
| 3 | | Reserved | Reserved | RW | - | - | 0 |
| 2 | | Reserved | Reserved | RW | - | - | 0 |
| 1 | | SE1_OE | Output enable for SE1 | RW | Disabled | Enabled | 27_Select power on latch |
| 0 | | SE2_OE | Output enable for SE2 | RW | Disabled | Enabled | 27_Select power on latch |

Byte 9 Output Control Register

| Bit | Pin | Name | Description | Type | 0 | 1 | Default |
|-----|-----|------------------|---|------|--|--------------------------------|---------|
| 7 | | PCIF5_STOP_EN | Allows control of PCIF5 with assertion of PCI_STOP# | RW | Free running | Stops with PCI_STOP# assertion | 0 |
| 6 | | TME_Readback | Trusted Mode Enable (TME) strap status | R | normal operation | no overclocking | 0 |
| 5 | | REF_Strength | Sets the REF output drive strength | RW | 1X (2Loads) | 2X (3 Loads) | 1 |
| 4 | | Test Mode Select | Allows test select, ignores REF/FSC/TestSel | RW | Outputs HI-Z | Outputs = REF/N | 0 |
| 3 | | Test Mode Entry | Allows entry into test mode, ignores FSB/TestMode | RW | Normal operation | Test mode | 0 |
| 2 | | IO_VOUT2 | IO Output Voltage Select (Most Significant Bit) | RW | See Table 3: V_IO Selection (Default is 0.8V) | | 1 |
| 1 | | IO_VOUT1 | IO Output Voltage Select | RW | | | 0 |
| 0 | | IO_VOUT0 | IO Output Voltage Select (Least Significant Bit) | RW | | | 1 |

Byte 10 Free-Running Control Register

| Bit | Pin | Name | Description | Type | 0 | 1 | Default |
|-----|-----|---------------------------|---|------|-------------------|-------------|-----------------|
| 7 | | 27_Select Latch read back | Readback of 27_Select latch | R | Dot96/ LCD_SS /SE | SRC0/ 27MHz | 27_Select latch |
| 6 | | Reserved | Reserved | RW | - | - | 1 |
| 5 | | Reserved | Reserved | RW | - | - | 1 |
| 4 | | CPU1_AMT_EN | M1 mode clk enable | RW | Disable | Enable | 1 |
| 3 | | Reserved | Reserved | RW | - | - | 1 |
| 2 | | CPU 2 Stop Enable | Enables control of CPU2 with CPU_STOP# | RW | Free Running | Stoppable | 1 |
| 1 | | CPU 1 Stop Enable | Enables control of CPU1 with CPU_STOP# | RW | Free Running | Stoppable | 1 |
| 0 | | CPU 0 Stop Enable | Enables control of CPU 0 with CPU_STOP# | RW | Free Running | Stoppable | 1 |

Byte 11 Strength Control Register

| Bit | Pin | Name | Description | Type | 0 | 1 | Default |
|-----|-----|----------|-------------|----------|----|----|---------|
| 7 | | 48MHz | Reserved | RW | 1x | 2x | 0 |
| 6 | | PCIF5 | | RW | 1x | 2x | 0 |
| 5 | | PCI4 | | RW | 1x | 2x | 0 |
| 4 | | PCI3 | | RW | 1x | 2x | 0 |
| 3 | | PCI2 | | RW | 1x | 2x | 0 |
| 2 | | PCI1 | | RW | 1x | 2x | 0 |
| 1 | | PCI0 | | RW | 1x | 2x | 0 |
| 0 | | Reserved | | Reserved | RW | - | - |



Byte 12 Byte Count Register

| Bit | Pin | Name | Description | Type | 0 | 1 | Default |
|-----|-----|----------|--|------|---|---|---------|
| 7 | | Reserved | | RW | | | 0 |
| 6 | | Reserved | | RW | | | 0 |
| 5 | | BC5 | Read Back byte count register, max bytes = 32 | RW | | | 0 |
| 4 | | BC4 | | RW | | | 0 |
| 3 | | BC3 | | RW | | | 1 |
| 2 | | BC2 | | RW | | | 1 |
| 1 | | BC1 | | RW | | | 0 |
| 0 | | BC0 | | RW | | | 1 |

Byte 13 VCO Frequency Control Register PLL1

| Bit | Pin | Name | Description | Type | 0 | 1 | Default |
|-----|-----|--------|--|------|---|---|---------|
| 7 | | N Div8 | N Divider 8 | RW | - | - | X |
| 6 | | N Div9 | N Divider 9 | RW | - | - | X |
| 5 | | M Div5 | The decimal representation of M Div (5:0) is equal to reference divider value. Default at power up = latch-in or Byte 0 Rom table. | RW | - | - | X |
| 4 | | M Div4 | | RW | - | - | X |
| 3 | | M Div3 | | RW | - | - | X |
| 2 | | M Div2 | | RW | - | - | X |
| 1 | | M Div1 | | RW | - | - | X |
| 0 | | M Div0 | | RW | - | - | X |

Byte 14 VCO Frequency Control Register PLL1

| Bit | Pin | Name | Description | Type | 0 | 1 | Default |
|-----|-----|--------|--|------|---|---|---------|
| 7 | | N Div7 | The decimal representation of N Div (9:0) is equal to VCO divider value. Default at power up = latch-in or Byte 0 Rom table. | RW | - | - | X |
| 6 | | N Div6 | | RW | - | - | X |
| 5 | | N Div5 | | RW | - | - | X |
| 4 | | N Div4 | | RW | - | - | X |
| 3 | | N Div3 | | RW | - | - | X |
| 2 | | N Div2 | | RW | - | - | X |
| 1 | | N Div1 | | RW | - | - | X |
| 0 | | N Div0 | | RW | - | - | X |

Byte 15 Spread Spectrum Control Register PLL1

| Bit | Pin | Name | Description | Type | 0 | 1 | Default |
|-----|-----|------|--|------|---|---|---------|
| 7 | | SSP7 | These Spread Spectrum bits will program the spread percentage. Contact ICS for the correct values. | RW | - | - | X |
| 6 | | SSP6 | | RW | - | - | X |
| 5 | | SSP5 | | RW | - | - | X |
| 4 | | SSP4 | | RW | - | - | X |
| 3 | | SSP3 | | RW | - | - | X |
| 2 | | SSP2 | | RW | - | - | X |
| 1 | | SSP1 | | RW | - | - | X |
| 0 | | SSP0 | | RW | - | - | X |

Byte 16 Spread Spectrum Control Register PLL1

| Bit | Pin | Name | Description | Type | 0 | 1 | Default |
|-----|-----|----------|--|------|---|---|---------|
| 7 | | Reserved | Reserved | RW | - | - | 0 |
| 6 | | SSP14 | These Spread Spectrum bits will program the spread percentage. Contact ICS for the correct values. | RW | - | - | x |
| 5 | | SSP13 | | RW | - | - | X |
| 4 | | SSP12 | | RW | - | - | X |
| 3 | | SSP11 | | RW | - | - | X |
| 2 | | SSP10 | | RW | - | - | X |
| 1 | | SSP9 | | RW | - | - | X |
| 0 | | SSP8 | | RW | - | - | X |



Byte 17 VCO Frequency Control Register PLL3

| Bit | Pin | Name | Description | Type | 0 | 1 | Default |
|-----|-----|--------|--|------|---|---|---------|
| 7 | | N Div8 | N Divider 8 | RW | - | - | X |
| 6 | | N Div9 | N Divider 9 | RW | - | - | X |
| 5 | | M Div5 | The decimal representation of M Div (5:0) is equal to reference divider value. Default at power up = latch-in or Byte 0 Rom table. | RW | - | - | X |
| 4 | | M Div4 | | RW | - | - | X |
| 3 | | M Div3 | | RW | - | - | X |
| 2 | | M Div2 | | RW | - | - | X |
| 1 | | M Div1 | | RW | - | - | X |
| 0 | | M Div0 | | RW | - | - | X |

Byte 18 VCO Frequency Control Register PLL3

| Bit | Pin | Name | Description | Type | 0 | 1 | Default |
|-----|-----|--------|--|------|---|---|---------|
| 7 | | N Div7 | The decimal representation of N Div (9:0) is equal to VCO divider value. Default at power up = latch-in or Byte 0 Rom table. | RW | - | - | X |
| 6 | | N Div6 | | RW | - | - | X |
| 5 | | N Div5 | | RW | - | - | X |
| 4 | | N Div4 | | RW | - | - | X |
| 3 | | N Div3 | | RW | - | - | X |
| 2 | | N Div2 | | RW | - | - | X |
| 1 | | N Div1 | | RW | - | - | X |
| 0 | | N Div0 | | RW | - | - | X |

Byte 19 Spread Spectrum Control Register PLL3

| Bit | Pin | Name | Description | Type | 0 | 1 | Default |
|-----|-----|------|--|------|---|---|---------|
| 7 | | SSP7 | These Spread Spectrum bits will program the spread percentage. Contact ICS for the correct values. | RW | - | - | X |
| 6 | | SSP6 | | RW | - | - | X |
| 5 | | SSP5 | | RW | - | - | X |
| 4 | | SSP4 | | RW | - | - | X |
| 3 | | SSP3 | | RW | - | - | X |
| 2 | | SSP2 | | RW | - | - | X |
| 1 | | SSP1 | | RW | - | - | X |
| 0 | | SSP0 | | RW | - | - | X |

Byte 20 Spread Spectrum Control Register PLL3

| Bit | Pin | Name | Description | Type | 0 | 1 | Default |
|-----|-----|----------|--|------|---|---|---------|
| 7 | | Reserved | Reserved | RW | - | - | 0 |
| 6 | | SSP14 | These Spread Spectrum bits will program the spread percentage. Contact ICS for the correct values. | RW | - | - | x |
| 5 | | SSP13 | | RW | - | - | X |
| 4 | | SSP12 | | RW | - | - | X |
| 3 | | SSP11 | | RW | - | - | X |
| 2 | | SSP10 | | RW | - | - | X |
| 1 | | SSP9 | | RW | - | - | X |
| 0 | | SSP8 | | RW | - | - | X |

Byte 21 M/N Enables

| Bit | Pin | Name | Description | RW | 0 | 1 | Default |
|-----|-----|------------|------------------------|----|---------|--------|---------|
| 7 | | Reserved | | RW | | | 0 |
| 6 | | Reserved | | RW | | | 0 |
| 5 | | Reserved | | RW | | | 0 |
| 4 | | Reserved | | RW | | | 0 |
| 3 | | Reserved | | RW | | | 0 |
| 2 | | Reserved | | RW | | | 0 |
| 1 | | M/N Enable | CPU PLL M/N Enable | RW | Disable | Enable | 0 |
| 0 | | M/N Enable | SRC/PCI PLL M/N Enable | RW | Disable | Enable | 0 |

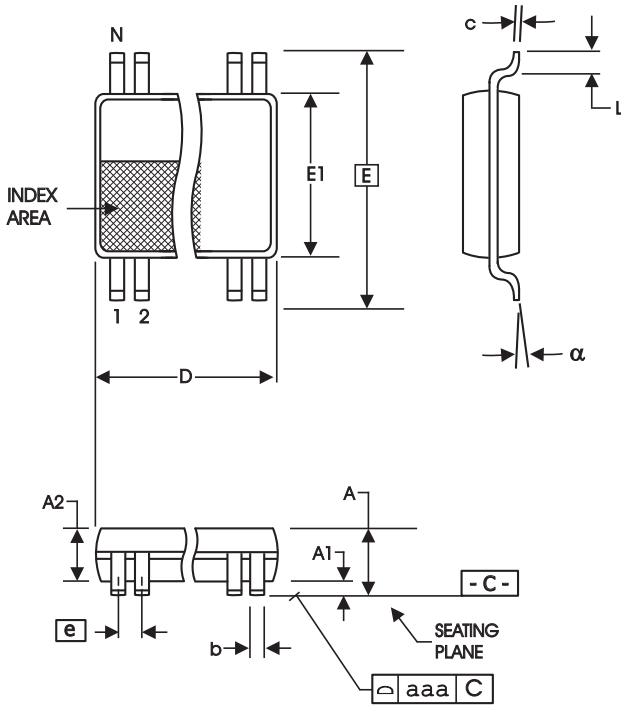
*These bits are disabled if TME is latched to 1

Test Clarification Table

| Comments | HW | | SW | | OUTPUT |
|--|-----------------------------|------------------------------|---------------------------|--------------------------|--------|
| | FSLC/ TEST_SEL HW PIN | FSLB/ TEST_MODE HW PIN | TEST ENTRY BIT B9b3 | REF/N or HI-Z B9b4 | |
| | <2.0V | X | 0 | 0 | NORMAL |
| Power-up w/ TEST_SEL = 1 to enter test mode | >2.0V | 0 | X | 0 | HI-Z |
| Cycle power to disable test mode | >2.0V | 0 | X | 1 | REF/N |
| FSLC./TEST_SEL -->3-level latched input | >2.0V | 1 | X | 0 | REF/N |
| If power-up w/ V>2.0V then use TEST_SEL | | | | | |
| If power-up w/ V<2.0V then use FSLC | >2.0V | 1 | X | 1 | REF/N |
| FSLB/TEST_MODE -->low Vth input | | | | | |
| TEST_MODE is a real time input | | | | | |
| If TEST_SEL HW pin is 0 during power-up, test mode can be invoked through B9b3. | <2.0V | X | 1 | 0 | HI-Z |
| If test mode is invoked by B9b3, only B9b4 is used to select HI-Z or REF/N | <2.0V | X | 1 | 1 | REF/N |
| FSLB/TEST_Mode pin is not used. | | | | | |
| Cycle power to disable test mode, one shot control | | | | | |

B9b3: 1= ENTER TEST MODE, Default = 0 (NORMAL OPERATION)

B9b4: 1= REF/N, Default = 0 (HI-Z)



**6.10 mm. Body, 0.50 mm. Pitch TSSOP
(240 mil) (20 mil)**

| SYMBOL | In Millimeters COMMON DIMENSIONS | | In Inches COMMON DIMENSIONS | |
|----------|-------------------------------------|------|--------------------------------|------|
| | MIN | MAX | MIN | MAX |
| A | -- | 1.20 | -- | .047 |
| A1 | 0.05 | 0.15 | .002 | .006 |
| A2 | 0.80 | 1.05 | .032 | .041 |
| b | 0.17 | 0.27 | .007 | .011 |
| c | 0.09 | 0.20 | .0035 | .008 |
| D | SEE VARIATIONS | | SEE VARIATIONS | |
| E | 8.10 BASIC | | 0.319 BASIC | |
| E1 | 6.00 | 6.20 | .236 | .244 |
| e | 0.50 BASIC | | 0.020 BASIC | |
| L | 0.45 | 0.75 | .018 | .030 |
| N | SEE VARIATIONS | | SEE VARIATIONS | |
| α | 0° | 8° | 0° | 8° |
| aaa | -- | 0.10 | -- | .004 |

VARIATIONS

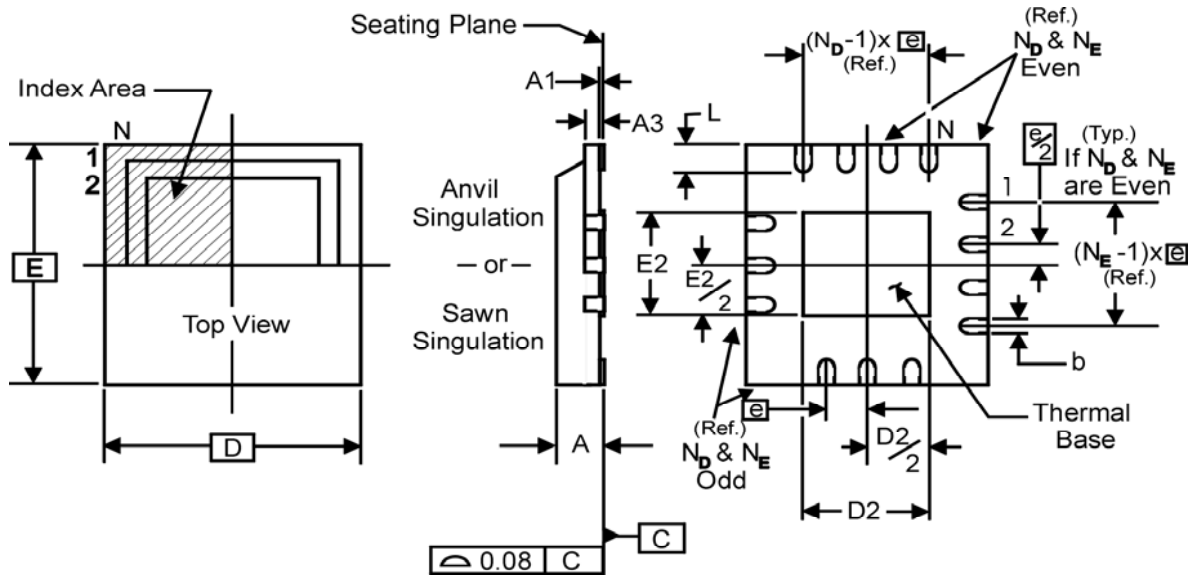
| N | D mm. | | D (inch) | |
|----|-------|-------|----------|------|
| | MIN | MAX | MIN | MAX |
| 64 | 16.90 | 17.10 | .665 | .673 |

Reference Doc.: JEDEC Publication 95, MO-153

10-0039

Marking Diagram





**THERMALLY ENHANCED, VERY THIN, FINE PITCH
QUAD FLAT / NO LEAD PLASTIC PACKAGE**

DIMENSIONS

| | |
|-------|----|
| | |
| N | 64 |
| N_D | 16 |
| N_E | 16 |

OPTION 1 DIMENSIONS (mm)

| SYMBOL | MIN. | MAX. |
|----------------|----------------|------|
| A | 0.8 | 1.0 |
| A1 | 0 | 0.05 |
| A3 | 0.25 Reference | |
| b | 0.18 | 0.3 |
| e | 0.50 BASIC | |
| D x E BASIC | 9.00 x 9.00 | |
| D2 MIN. / MAX. | 7.00 | 7.25 |
| E2 MIN. / MAX. | 7.00 | 7.25 |
| L MIN. / MAX. | 0.30 | 0.50 |

OPTION 2 DIMENSIONS (mm)

| SYMBOL | MIN. | MAX. |
|----------------|----------------|------|
| A | 0.8 | 1.0 |
| A1 | 0 | 0.05 |
| A3 | 0.25 Reference | |
| b | 0.18 | 0.3 |
| e | 0.50 BASIC | |
| D x E BASIC | 9.00 x 9.00 | |
| D2 MIN. / MAX. | 6.00 | 6.25 |
| E2 MIN. / MAX. | 6.00 | 6.25 |
| L MIN. / MAX. | 0.30 | 0.50 |

Marking Diagram



Ordering Information

| Part/Order Number | Marking | Shipping Packaging | Package | Temperature |
|-------------------|-------------|--------------------|----------|-------------|
| 9LPRS365BGLF | See page 26 | Tubes | 64-TSSOP | 0 to +70° C |
| 9LPRS365BGLFT | | Tape and Reel | | |
| 9LPRS365BKL F | See page 27 | Tubes | 64-VQFN | |
| 9LPRS365BKLFT | | Tape and Reel | | |



Revision History

| Rev. | Issue Date | Description | Page # |
|------|------------|--|---------------------|
| 0.1 | 4/5/2006 | Initial Release | - |
| 0.2 | 7/11/2006 | Updated Electrical Characteristics. | 12 |
| 0.3 | 8/25/2006 | 1. Updated pin description and I2C. | 2-5, 7-10, 22-23 |
| 0.4 | 10/25/2006 | Added Byte 21. | 23 |
| 0.5 | 11/22/2006 | 1. Updated pin description of pin #33 (TSSOP) and pin #40 (QFN) 2. Updated B1b0 in I2C. | 4,9, 19 |
| 0.6 | 11/29/2006 | Updated DS to reflect revision C changes | Various |
| 0.65 | 3/7/2007 | Updated Features/Benefits. | 1 |
| 0.7 | 3/9/2007 | Updated Supply currents in Electrical Characteristics. | 12 |
| 0.8 | 3/20/2007 | Updated Byte 5 bit 7 description in the I2C | 20 |
| 0.9 | 4/3/2007 | Updated B[11,21] in the I2C | 23 |
| 0.91 | 5/21/2007 | Removed Pull-up/Pull-Down footnotes. | 1 |
| 0.92 | 7/16/2007 | Updated Case Temperature in Electrical Characteristics. | 12 |
| 0.93 | 4/8/2008 | 1. Updated MLF ordering Information. 2. Reformatted Dimensions Tables. | 26 |
| 0.94 | 6/3/2008 | Updated Pin Description and SMBUS. | Various |
| 0.95 | 9/18/2008 | Updated Electrical Characteristics. | Various |
| 0.96 | 12/12/2008 | Added DS-Loading table. | 16 |
| 0.97 | 1/28/2009 | Update Table2, SMBus Byte1 table, added 27_Select tables for TSSOP and MLF | Various |
| 0.98 | 4/1/2009 | Update SEL27 and ITP_EN pin descriptions. | Various |
| 0.99 | 9/9/2009 | Added updated ordering information table and marking diagrams. | 26, 27 |