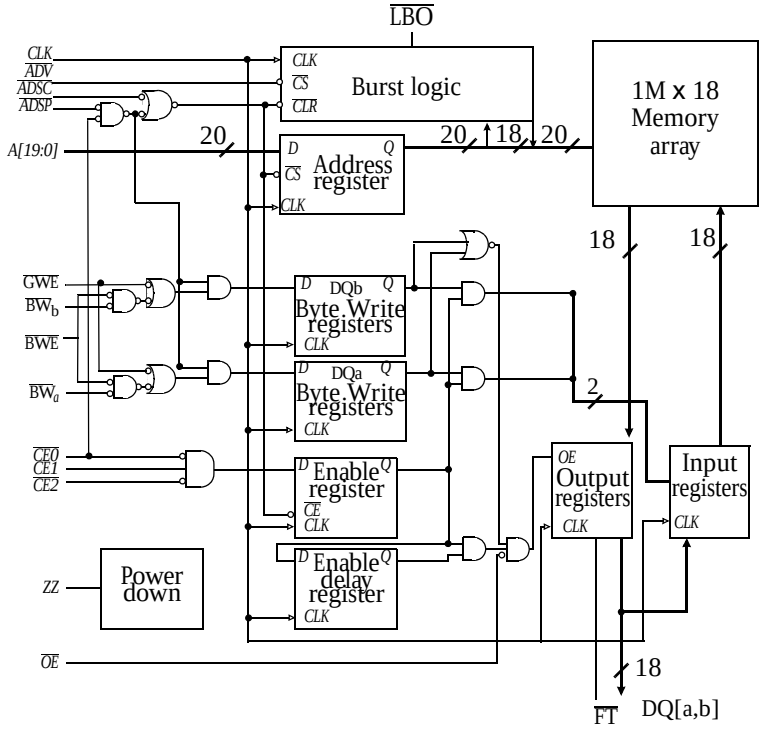
2.5V 1M x 18 pipelined burst synchronous SRAM

Features

- Organization: 1,048,576 x18 bits
- Fast clock speeds to 250MHz in LVTTL/LVCMOS
- Fast clock to data access: 2.6/2.8/3/3.4 ns
- Fast $\overline{OE}$ access time: 2.6/2.8/3/3.4 ns
- Fully synchronous register-to-register operation
- Single register flow-through mode
- Single-cycle deselect
- Asynchronous output enable control
- Available 100-pin TQFP and 165-ball BGA packages
- Byte write enables
- Multiple chip enables for easy expansion
- 2.5V core power supply
- NTD™ pipelined architecture available (AS7C251MNTD18A, AS7C25512NTD32A/ AS7C25512NTD36A)

Logic block diagram

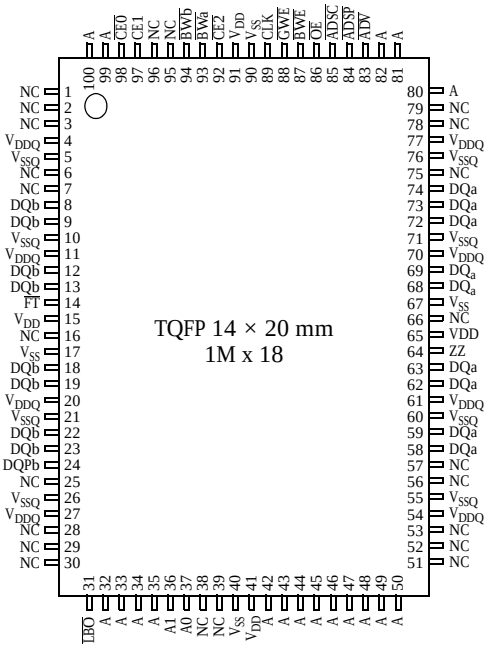


Selection guide

	-250	-225	-200	-166	Units
Minimum cycle time	4	4.4	5	6	ns
Maximum clock frequency	250	225	200	166	MHz
Maximum pipelined clock access time	2.6	2.8	3.0	3.4	ns
Maximum operating current	425	400	370	340	mA
Maximum standby current	110	110	110	90	mA
Maximum CMOS standby current (DC)	70	70	70	70	mA

Pin and ball designations

Pin configuration for 100-pin TQFP



Ball assignments for 165-ball BGA

	1	2	3	4	5	6	7	8	9	10	11
A	NC	A	$\overline{CE0}$	$\overline{BWb}$	NC	$\overline{CE2}$	$\overline{BWE}$	$\overline{ADSC}$	$\overline{ADV}$	A	A
B	NC	A	CE1	NC	$\overline{BWa}$	CLK	$\overline{GWE}$	$\overline{OE}$	$\overline{ADSP}$	A	NC
C	NC	NC	VDDQ	VSS	VSS	VSS	VSS	VSS	VDDQ	NC	DQPa
D	NC	DQb	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	DQa
E	NC	DQb	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	DQa
F	NC	DQb	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	DQa
G	NC	DQb	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	DQa
H	$\overline{FT}$	NC	NC	VDD	VSS	VSS	VSS	VDD	NC	NC	ZZ
J	DQb	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	NC
K	DQb	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	NC
L	DQb	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	NC
M	DQb	NC	VDDQ	VDD	VSS	VSS	NC	VDD	VDDQ	DQa	NC
N	DQPb	NC	VDDQ	VSS	NC	A	VSS	VSS	VDDQ	NC	NC
P	NC	NC	A	A	TDI	A1[1]	TDO	A	A	A	A
R	$\overline{LBO}$	NC	A	A	TMS	A0[1]	TCK	A	A	A	A

1 A0 and A1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.

Functional description

The AS7C251MPFS18A is a high-performance CMOS 16-Mbit synchronous Static Random Access Memory (SRAM) device organized as 1,048,576 words X 18 bits and incorporates a two-stage register-register pipeline for highest frequency on any given technology.

Fast cycle times of 4/4.4/5/6 ns with clock access times (t_{CD}) of 2.6/2.8/3/3.4 ns enable 250, 225, 200, and 166 MHz bus frequencies. Three chip enable ($\overline{CE}$) inputs permit easy memory expansion. Burst operation is initiated in one of two ways: the controller address strobe ($\overline{ADSC}$), or the processor address strobe ($\overline{ADSP}$). The burst advance pin ($\overline{ADV}$) allows subsequent internally generated burst addresses.

Read cycles are initiated with $\overline{ADSP}$ (regardless of $\overline{WE}$ and $\overline{ADSC}$) using the new external address clocked into the on-chip address register when $\overline{ADSP}$ is sampled low, the chip enables are sampled active, and the output buffer is enabled with $\overline{OE}$. In a read operation, the data accessed by the current address registered in the address registers by the positive edge of CLK is carried to the data-out registers and driven on the output pins on the next positive edge of CLK. $\overline{ADV}$ is ignored on the clock edge that samples $\overline{ADSP}$ asserted, but it is sampled on all subsequent clock edges. Address is incremented internally for the next access of the burst when $\overline{ADV}$ is sampled low and both address strobes are high. Burst mode is selectable with the $\overline{LBO}$ input. With $\overline{LBO}$ unconnected or driven high, burst operations use an interleaved count sequence. With $\overline{LBO}$ driven low, the device uses a linear count sequence.

Write cycles are performed by disabling the output buffers with $\overline{OE}$ and asserting a write command. A global write enable $\overline{GWE}$ writes all 18 bits regardless of the state of individual $\overline{BW[a,b]}$ inputs. Alternately, when $\overline{GWE}$ is high, one or more bytes may be written by asserting $\overline{BWE}$ and the appropriate individual byte $\overline{BWn}$ signals.

$\overline{BWn}$ is ignored on the clock edge that samples $\overline{ADSP}$ low, but it is sampled on all subsequent clock edges. Output buffers are disabled when $\overline{BWn}$ is sampled low, regardless of $\overline{OE}$. Data is clocked into the data input register when $\overline{BWn}$ is sampled low. Address is incremented internally to the next burst address if $\overline{BWn}$ and $\overline{ADV}$ are sampled low.

Read or write cycles may also be initiated with $\overline{ADSC}$ instead of $\overline{ADSP}$. The differences between cycles initiated with $\overline{ADSC}$ and $\overline{ADSP}$ follow.

- $\overline{ADSP}$ must be sampled high when $\overline{ADSC}$ is sampled low to initiate a cycle with $\overline{ADSC}$.
- $\overline{WE}$ signals are sampled on the clock edge that samples $\overline{ADSC}$ low (and $\overline{ADSP}$ high).
- Master chip enable $\overline{CE0}$ blocks $\overline{ADSP}$, but not $\overline{ADSC}$.

The AS7C251MPFS18A family operates from a core 2.5V power supply. These devices are available in a 100-pin TQFP and 165-ball BGA.

TQFP and BGA capacitance

Parameter	Symbol	Signals	Test conditions	Max	Unit
Input capacitance	C_{IN}	Address and control pins	V_{IN} = 0V	5	pF
I/O capacitance	$C_{I/O}$	I/O pins	V_{IN} = V_{OUT}	7	pF

Signal descriptions

Signal	I/O	Properties	Description
CLK	I	CLOCK	Clock. All inputs except $\overline{OE}$, $\overline{FT}$, ZZ, and $\overline{LBO}$ are synchronous to this clock.
A0–A17	I	SYNC	Address. Sampled when all chip enables are active and when $\overline{ADSC}$ or $\overline{ADSP}$ are asserted.
DQ[a,b]	I/O	SYNC	Data. Driven as output when the chip is enabled and when $\overline{OE}$ is active.
$\overline{CE0}$	I	SYNC	Master chip enable. Sampled on clock edges when $\overline{ADSP}$ or $\overline{ADSC}$ is active. When $\overline{CE0}$ is inactive, $\overline{ADSP}$ is blocked. Refer to the "Synchronous truth table" for more information.
CE1, $\overline{CE2}$	I	SYNC	Synchronous chip enables. Active high and active low, respectively. Sampled on clock edges when $\overline{ADSC}$ is active or when $\overline{CE0}$ and $\overline{ADSP}$ are active.
$\overline{ADSP}$	I	SYNC	Address strobe processor. Asserted low to load a new bus address or to enter standby mode.
$\overline{ADSC}$	I	SYNC	Address strobe controller. Asserted low to load a new address or to enter standby mode.
$\overline{ADV}$	I	SYNC	Advance. Asserted low to continue burst read/write.
$\overline{GWE}$	I	SYNC	Global write enable. Asserted low to write all 32/36 and 18 bits. When high, $\overline{BWE}$ and $\overline{BW[a,b]}$ control write enable.
$\overline{BWE}$	I	SYNC	Byte write enable. Asserted low with $\overline{GWE}$ high to enable effect of $\overline{BW[a,b]}$ inputs.
$\overline{BW[a,b]}$	I	SYNC	Write enables. Used to control write of individual bytes when $\overline{GWE}$ is high and $\overline{BWE}$ is low. If any of $\overline{BW[a,b]}$ is active with $\overline{GWE}$ high and $\overline{BWE}$ low, the cycle is a write cycle. If all $\overline{BW[AB]}$ are inactive, the cycle is a read cycle.
$\overline{OE}$	I	ASYNC	Asynchronous output enable. I/O pins are driven when $\overline{OE}$ is active and the chip is in read mode.
$\overline{LBO}$	I	STATIC	Count mode. When driven high, count sequence follows Intel XOR convention. When driven low, count sequence follows linear convention. *This signal is internally pulled high.*[18]
TDO	O	SYNC	Serial data-out to the JTAG circuit. Delivers data on the negative edge of TCK (BGA only).
TDI	I	SYNC	Serial data-in to the JTAG circuit. Sampled on the rising edge of TCK (BGA only).
TMS	I	SYNC	This pin controls the Test Access Port state machine. Sampled on the rising edge of TCK (BGA only).
TCK	O	SYNC	Serial data-out to the JTAG circuit. Delivers data on the negative edge of TCK (BGA only).
$\overline{FT}$	I	STATIC	Flow-through mode.When low, enables single register flow-through mode. Connect to V_{DD} if unused or for pipelined operation.
ZZ	I	ASYNC	Sleep. Places device in low power mode; data is retained. Connect to GND if unused.

Write enable truth table (per byte)

Function	$\overline{GWE}$	$\overline{BWE}$	$\overline{BWa}$	$\overline{BWb}$
Write all bytes (a, b)	L	X	X	X
	H	L	L	L
Write byte a	H	L	L	H
Write byte b	H	L	H	L
Read	H	H	X	X
	H	L	H	H

Key: X = don't care; L = low; H = high; $\overline{BWE}$, $\overline{BWn}$ = internal write signal

Synchronous truth table

$\overline{CE0}$	CE1	$\overline{CE2}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{BWn}$[1]	$\overline{OE}$	Address accessed	CLK	Operation	DQ
H	X	X	X	L	X	X	X	NA	L to H	Deselect	Hi–Z
L	L	X	L	X	X	X	X	NA	L to H	Deselect	Hi–Z
L	L	X	H	L	X	X	X	NA	L to H	Deselect	Hi–Z
L	X	H	L	X	X	X	X	NA	L to H	Deselect	Hi–Z
L	X	H	H	L	X	X	X	NA	L to H	Deselect	Hi–Z
L	H	L	L	X	X	X	L	External	L to H	Begin read	Hi–Z[2]
L	H	L	L	X	X	X	H	External	L to H	Begin read	Hi–Z
L	H	L	H	L	X	F	L	External	L to H	Begin read	Hi–Z[2]
L	H	L	H	L	X	F	H	External	L to H	Begin read	Hi–Z
X	X	X	H	H	L	F	L	Next	L to H	Continue read	Q
X	X	X	H	H	L	F	H	Next	L to H	Continue read	Hi–Z
X	X	X	H	H	H	F	L	Current	L to H	Suspend read	Q
X	X	X	H	H	H	F	H	Current	L to H	Suspend read	Hi–Z
H	X	X	X	H	L	F	L	Next	L to H	Continue read	Q
H	X	X	X	H	L	F	H	Next	L to H	Continue read	Hi–Z
H	X	X	X	H	H	F	L	Current	L to H	Suspend read	Q
H	X	X	X	H	H	F	H	Current	L to H	Suspend read	Hi–Z
L	H	L	H	L	X	T	X	External	L to H	Begin write	D[3]
X	X	X	H	H	L	T	X	Next	L to H	Continue write	D
H	X	X	X	H	L	T	X	Next	L to H	Continue write	D
X	X	X	H	H	H	T	X	Current	L to H	Suspend write	D
H	X	X	X	H	H	T	X	Current	L to H	Suspend write	D

1 See “Write enable truth table” on page 4 for more information.
2 Q in flow-through mode.
3 For a write operation following a read operation, $\overline{OE}$ must be high before the input data set up time and must be held high throughout the input hold time

Key: X = don’t care, L = low, H = high

TQFP and BGA thermal resistance

Description		Symbol	Typical	Units	Conditions
Thermal resistance (junction to ambient)[1]	1 layer	θ_{JA}	40	°C/W	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51
	4 layer	θ_{JA}	22	°C/W	
Thermal resistance (junction to top of case)[1]		θ_{JC}	8	°C/W	

1 This parameter is sampled.

Absolute maximum ratings

Parameter	Symbol	Min	Max	Unit
Power supply voltage relative to GND	V_{DD}, V_{DDQ}	–0.3	+3.6	V
Input voltage relative to GND (input pins)	V_{IN}	–0.3	V_{DD} + 0.3	V
Input voltage relative to GND (I/O pins)	V_{IN}	–0.3	V_{DDQ} + 0.3	V
Power dissipation	P_D	–	1.8	W
DC output current	I_{OUT}	–	20 mA	mA
Storage temperature (plastic)	T_{stg}	–65	+150	°C
Temperature under bias	T_{bias}	–65	+135	°C

Note: Stresses greater than those listed in this table may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect reliability.

Recommended operating conditions

Parameter		Symbol	Min	Nominal	Max	Unit
Supply voltage		V_{DD}, V_{DDQ}	2.375	2.5	2.625	V
		V_{SS}	0.0	0.0	0.0	
Input voltages	Address and control pins	V_{IH}	2.0	–	V_{DD} + 0.3	V
		V_{IL}	–0.3[1]	–	0.4	
	I/O pins	V_{IH}	2.0	–	V_{DDQ} + 0.3	V
		V_{IL}	–0.3[1]	–	0.4	
Ambient operating temperature		T_A	0	–	70	°C

1 V_{IL} min = –2.0V for pulse width less than 0.2 × t_{RC}.

DC electrical characteristics

Parameter	Sym	Test conditions	–250		–225		–200		–166		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
Input leakage current[1]	$\lvert I_{LI} \rvert$	V_{DD} = Max, V_{IN} = GND to V_{DD}	–	2	–	2	–	2	–	2	µA
Output leakage current	$\lvert I_{LO} \rvert$	$\overline{OE} \geq V_{IH}$, V_{DD} = Max, V_{OUT} = GND to V_{DD}	–1	1	–1	1	–1	1	–1	1	µA
Operating power supply current[2]	I_{CC} (Pipelined)	$\overline{CE0} = V_{IL}$, CE1 = V_{IH}, $\overline{CE2} = V_{IL}$, f = f_{Max}, I_{OUT} = 0 mA	–	425	–	400	–	370	–	340	mA
Operating power supply current	I_{CC} (Flow-through)		–	250	–	225	–	200	–	175	mA
Standby power supply current	I_{SB}	Deselected, f = f_{Max}, ZZ ≤ V_{IL}	–	110	–	110	–	110	–	90	mA
	I_{SB1}	Deselected, f = 0, ZZ ≤ 0.2V all V_{IN} ≤ 0.2V or ≥ (V_{DD}, V_{DDQ}) – 0.2V	–	70	–	70	–	70	–	70	
	I_{SB2}	Deselected, f = f_{Max}, ZZ ≥ (V_{DD}, V_{DDQ})– 0.2V All V_{IN} ≤ V_{IL} or ≥ V_{IH}	–	30	–	30	–	30	–	30	
Output voltage	V_{OL}	I_{OL} = 2 mA, V_{DDQ} = 2.65V	–	0.7	–	0.7	–	0.7	–	0.7	V
	V_{OH}	I_{OH} = –2 mA, V_{DDQ} = 2.35V	1.7	–	1.7	–	1.7	–	1.7	–	

1 $\overline{LBO}$ pin has an internal pull-up, and input leakage = ±10 µa.
2 I_{CC} given with no output loading. ICC increases with faster cycle times and greater output loading.

Timing characteristics over operating range

Parameter	Sym	–250		–225		–200		–166		Unit	Notes[1]
		Min	Max	Min	Max	Min	Max	Min	Max		
Clock frequency	f_{Max}	–	250	–	225	–	200	–	166	MHz	
Cycle time (pipelined mode)	t_{CYC}	4	–	4.4	–	5	–	6	–	ns	
Cycle time (flow-through mode)	t_{CYCF}	6.5	–	6.9	–	7.5	–	8.5	–	ns	
Clock access time (pipelined mode)	t_{CD}	–	2.6	–	2.8	–	3.0	–	3.4	ns	
Clock access time (flow-through mode)	t_{CDF}	–	6.5	–	6.9	–	7.5	–	8.5	ns	
Output enable low to data valid	t_{OE}	–	2.6	–	2.8	–	3.0	–	3.4	ns	
Clock high to output low Z	t_{LZC}	0	–	0	–	0	–	0	–	ns	2, 3, 4
Data output invalid from clock high	t_{OH}	1.5	–	1.5	–	1.5	–	1.5	–	ns	2
Output enable low to output low Z	t_{LZOE}	0	–	0	–	0	–	0	–	ns	2, 3, 4
Output enable high to output high Z	t_{HZOE}	–	2.6	–	2.8	–	3.0	–	3.4	ns	2, 3, 4
Clock high to output high Z	t_{HZC}	–	2.6	–	2.8	–	3.0	–	3.4	ns	2, 3, 4
Output enable high to invalid output	t_{OHOE}	0	–		–	0	–	0	–	ns	
Clock high pulse width	t_{CH}	1.5	-	1.8	–	1.8	–	2.1	–	ns	5
Clock low pulse width	t_{CL}	1.5	-	1.8	–	1.8	–	2.2	–	ns	5
Address setup to clock high	t_{AS}	1.2	-	1.4	–	1.4	–	1.5	–	ns	6
Data setup to clock high	t_{DS}	1.2	-	1.4	–	1.4	–	1.5	–	ns	6
Write setup to clock high	t_{WS}	1.2	-	1.4	–	1.4	–	1.5	–	ns	6, 7
Chip select setup to clock high	t_{CSS}	1.2	-	1.4	–	1.4	–	1.5	–	ns	6, 8
Address hold from clock high	t_{AH}	0.3	-	0.4	–	0.4	–	0.5	–	ns	6
Data hold from clock high	t_{DH}	0.3	-	0.4	–	0.4	–	0.5	–	ns	6
Write hold from clock high	t_{WH}	0.3	-	0.4	–	0.4	–	0.5	–	ns	6, 7
Chip select hold from clock high	t_{CSH}	0.3	-	0.4	–	0.4	–	0.5	–	ns	6, 8
$\overline{ADV}$ setup to clock high	t_{ADVS}	1.2	-	1.4	–	1.4	–	1.5	–	ns	6
$\overline{ADSP}$ setup to clock high	t_{ADSPS}	1.2	-	1.4	–	1.4	–	1.5	–	ns	6
$\overline{ADSC}$ setup to clock high	t_{ADSCS}	1.2	-	1.4	–	1.4	–	1.5	–	ns	6
$\overline{ADV}$ hold from clock high	t_{ADVH}	0.3	-	0.4	–	0.4	–	0.5	–	ns	6
$\overline{ADSP}$ hold from clock high	t_{ADSPH}	0.3	-	0.4	–	0.4	–	0.5	–	ns	6
$\overline{ADSC}$ hold from clock high	t_{ADSCH}	0.3	-	0.4	–	0.4	–	0.5	–	ns	6

1 See “Notes” on page 19.

IEEE 1149.1 serial boundary scan (JTAG)

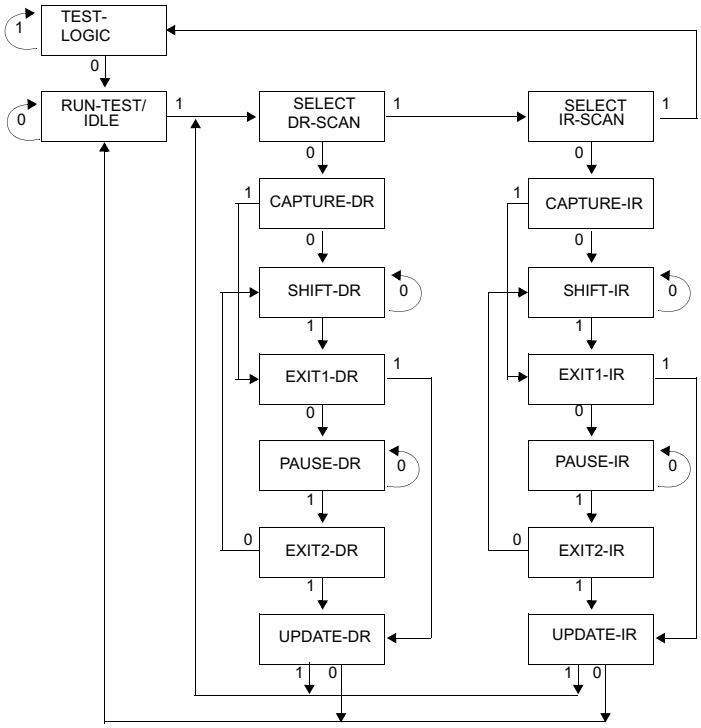
The SRAM incorporates a serial boundary scan test access port (TAP). The port operates in accordance with IEEE Standard 1149.1-1990 but does not have the set of functions required for full 1149.1 compliance. The inclusion of these functions would place an added delay in the critical speed path of the SRAM. The TAP controller functionality does not conflict with the operation of other devices using 1149.1 fully compliant TAPs. It uses JEDEC-standard 2.5V I/O logic levels.

The SRAM contains a TAP controller, instruction register, boundary scan register, bypass register, and ID register.

Disabling the JTAG feature

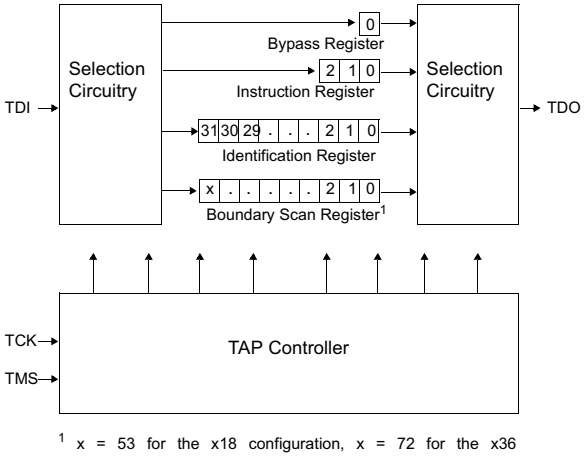
If the JTAG function is not being implemented, its pins/balls can be left unconnected. At power-up, the device will come up in a reset state which will not interfere with the operation of the device.

TAP controller state diagram



Note: The 0 or 1 next to each state represents the value of TMS at the rising edge of TCK.

TAP controller block diagram



1 x = 53 for the x18 configuration, x = 72 for the x36

Test access port (TAP)

Test clock (TCK)

The test clock is used with only the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

Test mode select (TMS)

The TAP controller receives commands from TMS input. It is sampled on the rising edge of TCK. You can leave this pin/ball unconnected if the TAP is not used. The pin/ball is pulled up internally, resulting in a logic high level.

Test data-in (TDI)

The TDI pin/ball serially inputs information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. For information on loading the instruction register, see the TAP Controller State Diagram. TDI is internally pulled up and can be unconnected if the TAP is unused in an application. TDI is connected to the most significant bit (MSB) of any register. (See the TAP Controller Block Diagram.)

Test data-out (TDO)

The TDO output pin/ball serially clocks data-out from the registers. The output is active depending upon the current state of the TAP state machine. The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register. (See the TAP Controller State Diagram.)

Performing a TAP RESET

You can perform a RESET by forcing TMS high (V_{DD}) for five rising edges of TCK. This RESET does not affect the operation of the SRAM and can be performed while the SRAM is operating.

At power-up, the TAP is reset internally to ensure that TDO comes up in a high-Z state.

TAP registers

Registers are connected between the TDI and TDO pins/balls. They allow data to be scanned into and out of the SRAM test circuitry. Only one register can be selected at a time through the instruction register. Data is serially loaded into the TDI pin/ball on the rising edge of TCK. Data is output on the TDO pin/ball on the falling edge of TCK.

Instruction register

You can serially load three-bit instructions into the instruction register. The register is loaded when it is placed between the TDI and TDO pins/balls as shown in the TAP Controller Block Diagram. The instruction register is loaded with the IDCODE instruction at power up and also if the controller is placed in a reset state, as described in the previous section.

When the TAP controller is in the Capture-IR state, the two least significant bits are loaded with a binary “01” pattern to allow for fault isolation of the board-level series test data path.

Bypass register

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain chips. The bypass register is a single-bit register that can be placed between the TDI and TDO pins/balls. This allows data to be shifted through the SRAM with minimal delay. The bypass register is set low (Vss) when the BYPASS instruction is executed.

Boundary scan register

The boundary scan register is connected to all the input and bidirectional pins/balls on the SRAM. The x36 configuration has a 72-bit-long register and the x18 configuration has a 53-bit-long register.

The boundary scan register is loaded with the contents of the RAM I/O ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO pins/balls when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/RELOAD, and SAMPLE Z instructions can be used to capture the contents of the I/O ring.

The boundary scan order table shows the order in which the bits are connected. Each bit corresponds to one of the bumps on the SRAM package. The most significant bit (MSB) of the register is connected to TDI, and the least significant bit (LSB) is connected to TDO.

Identification (ID) register

The ID register has a vendor code and other information described in the Identification Register Definitions table. The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state.

TAP instruction set

Eight different instructions are possible with the 3-bit instruction register. All combinations are listed in the Instruction Codes table. Three of these instructions are reserved and should not be used.

Note that the TAP controller used in this SRAM is not fully compliant to the 1149.1 convention because some of the mandatory 1149.1 instructions are not fully implemented. The TAP controller cannot be used to load address, data, or control signals into the SRAM and cannot preload the I/O buffers. The SRAM does not implement the 1149.1 commands EXTEST or INTEST or the PRELOAD portion of SAMPLE/PRELOAD. Instead, it performs a capture of the I/O ring when these instructions are executed.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO pins/balls. To execute the instruction once it is shifted in, the TAP controller needs to be moved into the Update-IR state.

EXTEST

The EXTEST instruction, which executes whenever the instruction register is loaded with all 0s, is not implemented in this SRAM TAP controller. The TAP controller, however, does recognize an all-0 instruction. When an EXTEST instruction is loaded into the instruction register, the SRAM responds as if a SAMPLE/PRELOAD instruction has been loaded. Unlike the SAMPLE/PRELOAD instruction, EXTEST places the SRAM outputs in a high-Z state.

EXTEST is a mandatory 1149.1 instruction. this device, therefore, is not compliant with 1149.1.

IDCODE

The IDCODE instruction is loaded into the instruction register upon power-up or whenever the TAP controller is given a test logic reset state. The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the instruction register. It also places the instruction register between the TDI and TDO pins/balls and allows the IDCODE to be shifted out of the device when the TAP controller enters the Shift-DR state.

SAMPLE Z

The SAMPLE Z instruction causes the boundary scan register to be connected between the TDI and TDO pins/balls when the TAP controller is in a Shift-DR state. It also places all SRAM outputs into a high-Z state.

SAMPLE/PRELOAD

When the SAMPLE/PRELOAD instruction is loaded into the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the inputs and bidirectional pins/balls is captured in the boundary scan register. Note that the SAMPLE/PRELOAD is a 1149.1 mandatory instruction, but the PRELOAD portion of this instruction is not implemented in this device. The TAP controller, therefore, is not fully 1149.1 compliant.

Be aware that the TAP controller clock can operate only at a frequency up to 10 Mhz, while the SRAM clock operates more than an order of magnitude faster. Because there is a large difference in the clock frequencies, it is possible that during the Capture-DR state, an input or output can undergo a transition. The TAP may then try to capture a signal while in transition (metastable state). This will not harm the device, but there is no guarantee as to the value that will be captured. Repeatable results may not be possible.

To guarantee that the boundary scan register captures the correct value of a signal, the SRAM signal must be stabilized long enough to meet the TAP controller's capture setup plus hold time (^{t}CS plus ^{t}CH). The SRAM clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is an issue, it is possible to capture all other signals and ignore the value of the CK and CK# captured in the boundary scan register.

Once the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO pins.

Note that since the PRELOAD part of the command is not implemented, putting the TAP to the Update-DR state while performing a SAMPLE/PRELOAD instruction will have the same effect as the Pause-DR command.

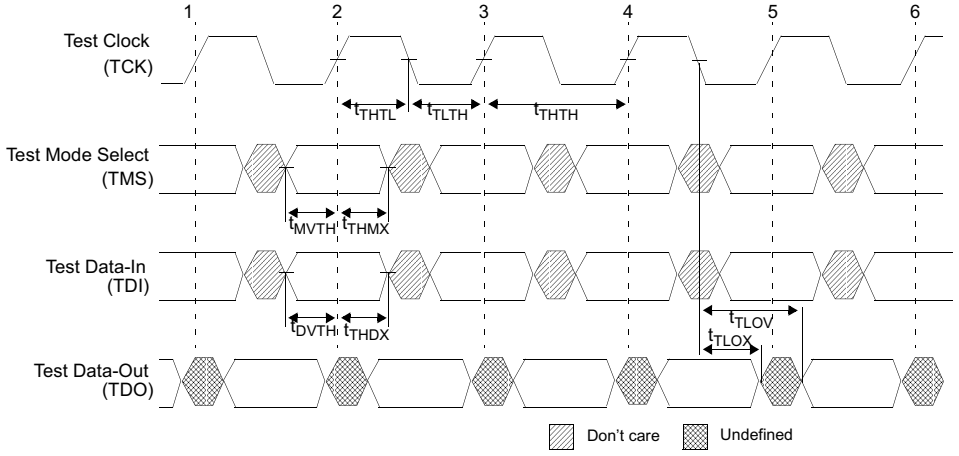
BYPASS

The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board. When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between TDI and TDO.

Reserved

Do not use a reserved instruction.These instructions are not implemented but are reserved for future use.

TAP timing diagram



TAP AC electrical characteristics

For notes 1 and 2, $+10^{o}C \leq T_J \leq +110^{o}C$ and $+2.4V \leq V_{DD} \leq +2.6V$.

Description	Symbol	Min	Max	Units
Clock				
Clock cycle time	^{t}THTH	100		ns
Clock frequency	^{f}TF		10	MHz
Clock high time	^{t}THTL	40		ns
Clock low time	^{t}TLTH	40		ns
Output Times				
TCK low to TDO unknown	^{t}TLOX	0		ns
TCK low to TDO valid	^{t}TLOV		20	ns
TDI valid to TCK high	^{t}DVTH	10		ns
TCK high to TDI invalid	^{t}THDX	10		ns
Setup Times				
TMS setup	^{t}MVTH	10		ns
Capture setup	^{t}CS[1]	10		ns
Hold Times				
TMS hold	^{t}THMX	10		ns
Capture hold	^{t}CH[1]	10		ns

1 ^{t}CS and ^{t}CH refer to the setup and hold time requirements of latching data from the boundary scan register.

2 Test conditions are specified using the load in the figure TAP AC output load equivalent.

TAP AC test conditions

Input pulse levels. . . . . Vss to 2.5V

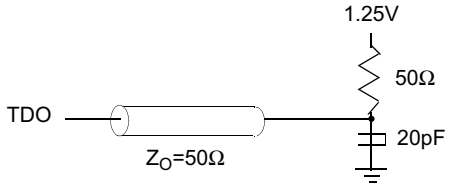
Input rise and fall times. . . . . 1 ns

Input timing reference levels. 1.25V

Output reference levels 1.25V

Test load termination supply voltage. . . . 1.25V

TAP AC output load equivalent



TAP DC electrical characteristics and operating conditions

(+10°C ≤ T_J ≤ +110°C and +2.4V ≤ V_{DD} ≤ +2.6V unless otherwise noted)

Description	Conditions	Symbol	Min	Max	Units	Notes
Input high (logic 1) voltage		V_{IH}	1.7	V_{DD} + 0.3	V	1, 2
Input low (logic 0) voltage		V_{IL}	-0.3	0.7	V	1, 2
Input leakage current	0V ≤ V_{IN} ≤ V_{DD}	IL_I	-5.0	5.0	µA	
Output leakage current	Outputs disabled, 0V ≤ V_{IN} ≤ V_{DDQ}(DQx)	IL_O	-5.0	5.0	µA	
Output low voltage	I_{OLC} = 100µA	V_{OL1}		0.2	V	1
Output low voltage	I_{OLT} = 2mA	V_{OL2}		0.7	V	1
Output high voltage	I_{OHS} = -100µA	V_{OH1}	2.1		V	1
Output high voltage	I_{OHT} = -2mA	V_{OH2}	1.7		V	1

1. All voltage referenced to V_{SS}(GND).
2. Overshoot: V_{IH}(AC) ≤ V_{DD} + 1.5V for t ≤ $^tKHKH/2$

   Undershoot: V_{IL}(AC) ≥ -0.5 for t ≤ $^tKHKH/2$

   Power-up: V_{IH} ≤ +2.6V and V_{DD} ≤ 2.4V and V_{DDQ} ≤ 1.4V for t ≤ 200ms

   During normal operation, V_{DDQ} must not exceed V_{DD} Control input signals (such as $\overline{LD}$, R/$\overline{W}$, etc.) may not have pulsed widths less than t_{KHKL}(Min) or operate at frequencies exceeding f_{KF}(Max).

Identification register definitions

Instruction field	1M x 18	Description
Revision number (31:28)	xxxx	Reserved for version number.
Device depth (27:23)	xxxxx	Defines the depth of 1Mb words.
Device width (22:18)	xxxxx	Defines the width of x18 bits.
Device ID (17:12)	xxxxxx	Reserved for future use.
JEDEC ID code (11:1)	00000110100	Allows unique identification of SRAM vendor.
ID register presence indicator (0)	1	Indicates the presence of an ID register.

Scan register sizes

Register name	Bit size	
Instruction	3	
Bypass	1	
ID	32	
Boundary scan	x18:53	x36:72

Instruction codes

Instruction	Code	Description
EXTEST	000	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all SRAM outputs to high-Z state. This instruction is not 1149.1-compliant.
IDCODE	001	Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operations.
SAMPLE Z	010	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all SRAM output drivers to a high-Z state.
Reserved	011	Do not use. This instruction is reserved for future use.
SAMPLE/PRELOAD	100	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Does not affect SRAM operation. This instruction does not implement 1149.1 preload function and is therefore not 1149.1-compliant.
Reserved	101	Do not use. This instruction is reserved for future use.
Reserved	110	Do not use. This instruction is reserved for future use.
BYPASS	111	Places the bypass register between TDI and TDO. This operation does not affect SRAM operations.

165-ball BGA boundary scan order (x18)

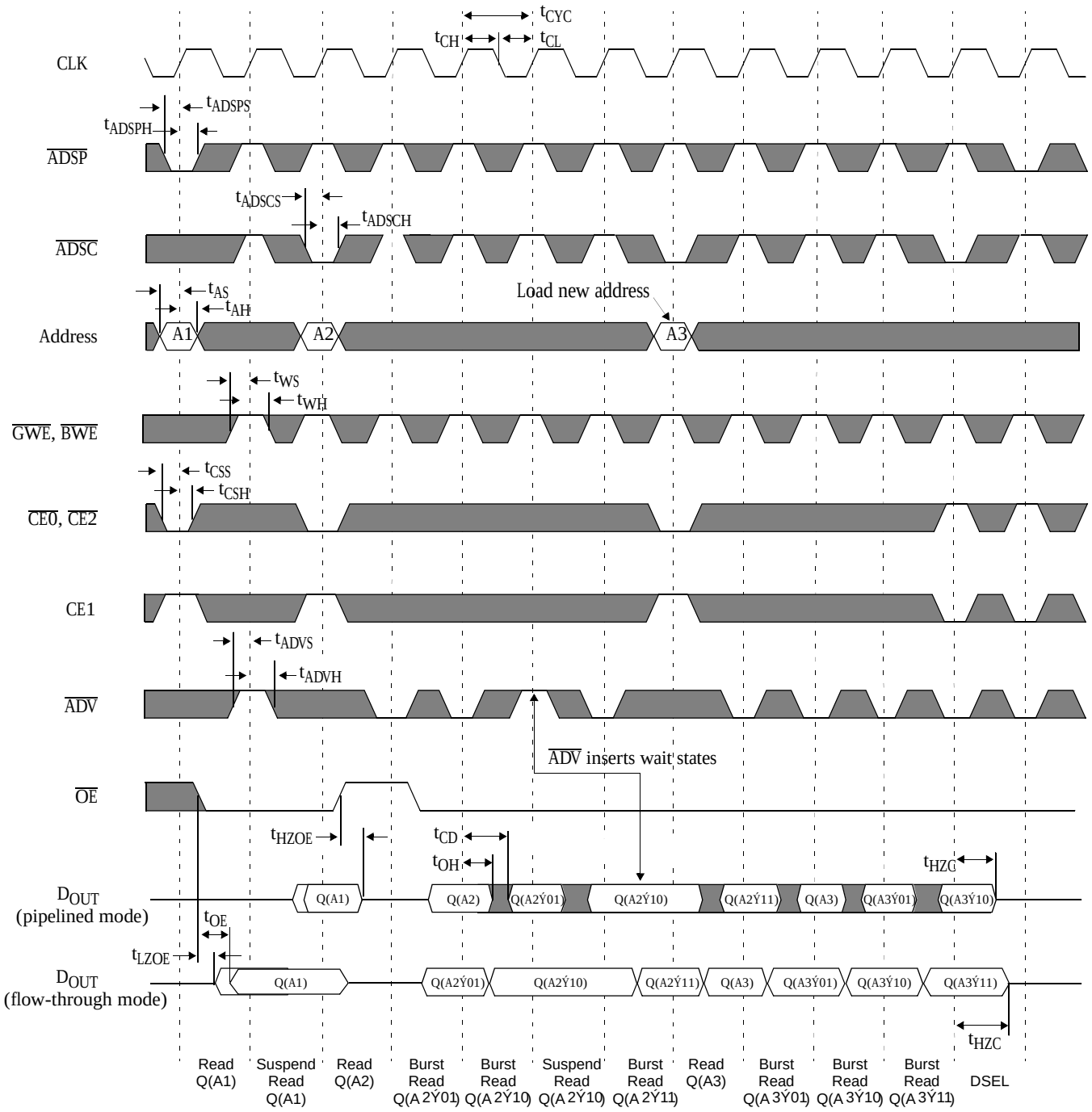
Bit #s	Signal Name	Ball ID
1	SA	11P
2	SA	6N
3	SA	8P
4	SA	8R
5	SA	9R
6	SA	9P
7	SA	10P
8	SA	10R
9	SA	11R
10	DQa	10M
11	DQa	10L
12	DQa	10K
13	DQa	10J
14	ZZ	11H
15	DQa	11G
16	DQa	11F
17	DQa	11E
18	DQa	11D
19	DQPa	11C
20	SA	11A
21	SA	10A
22	SA	10B
23	$\overline{\text{ADV}}$	9A
24	$\overline{\text{ADSP}}$	9B
25	$\overline{\text{ADSC}}$	8A
26	$\overline{\text{OE}}$	8B
27	$\overline{\text{BWE}}$	7A

Bit #s	Signal Name	Ball ID
28	$\overline{\text{GWE}}$	7B
29	CLK	6B
30	$\overline{\text{CE2}}$	6A
31	$\overline{\text{BWa}}$	5B
32	$\overline{\text{BWb}}$	4A
33	CE1	3B
34	$\overline{\text{CE0}}$	3A
35	SA	2A
36	SA	2B
37	DQb	2D
38	DQb	2E
39	DQb	2F
40	DQb	2G
41	$\overline{\text{FT}}$	1H
42	DQb	1J
43	DQb	1K
44	DQb	1L
45	DQb	1M
46	DQPb	1N
47	$\overline{\text{LBO}}$	1R
48	SA	3P
49	SA	3R
50	SA	4R
51	SA	4P
52	SA1	6P
53	SA0	6R

Key to switching waveforms

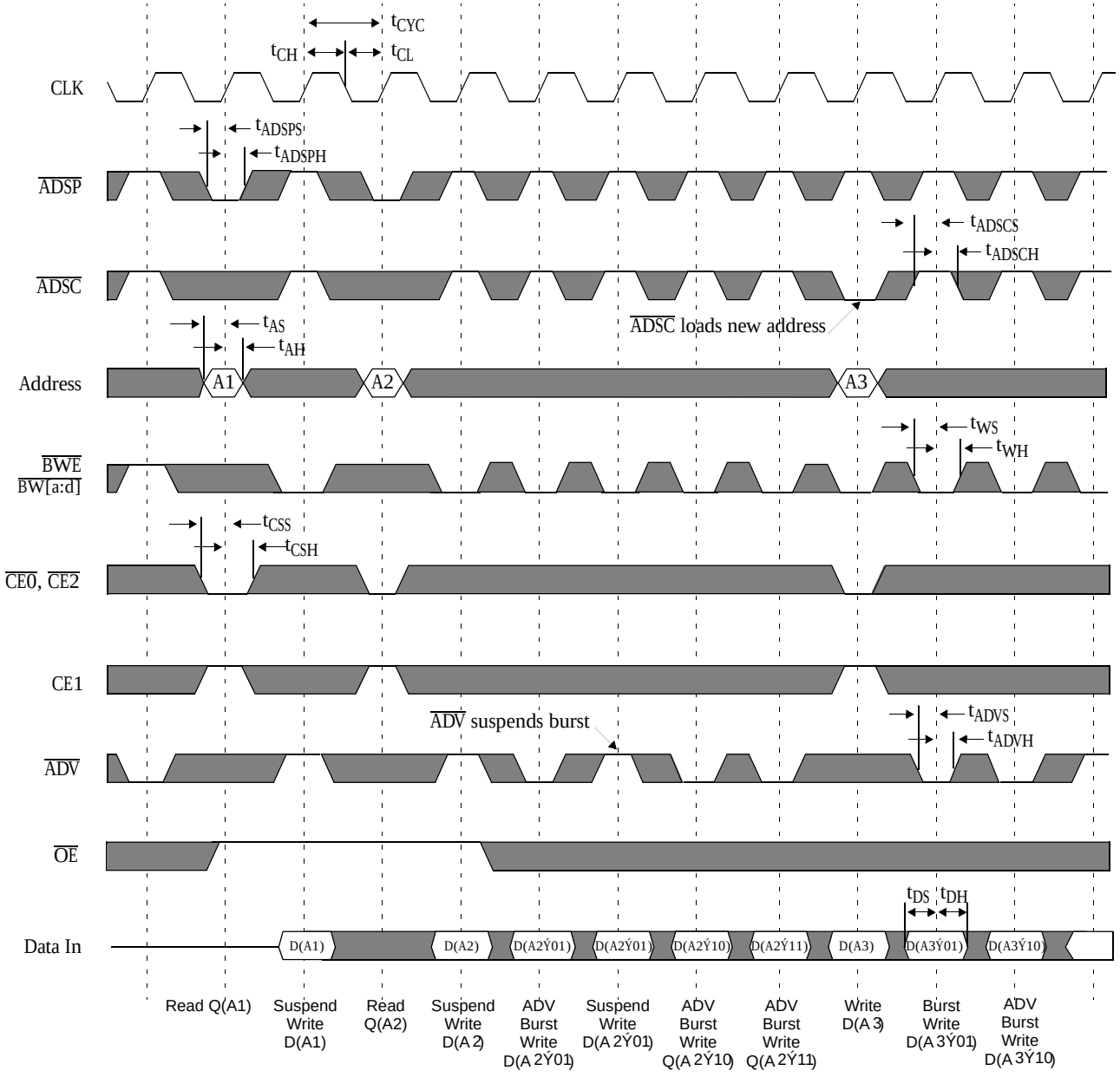
Rising input Falling input Undefined / don't care

Timing waveform of read cycle



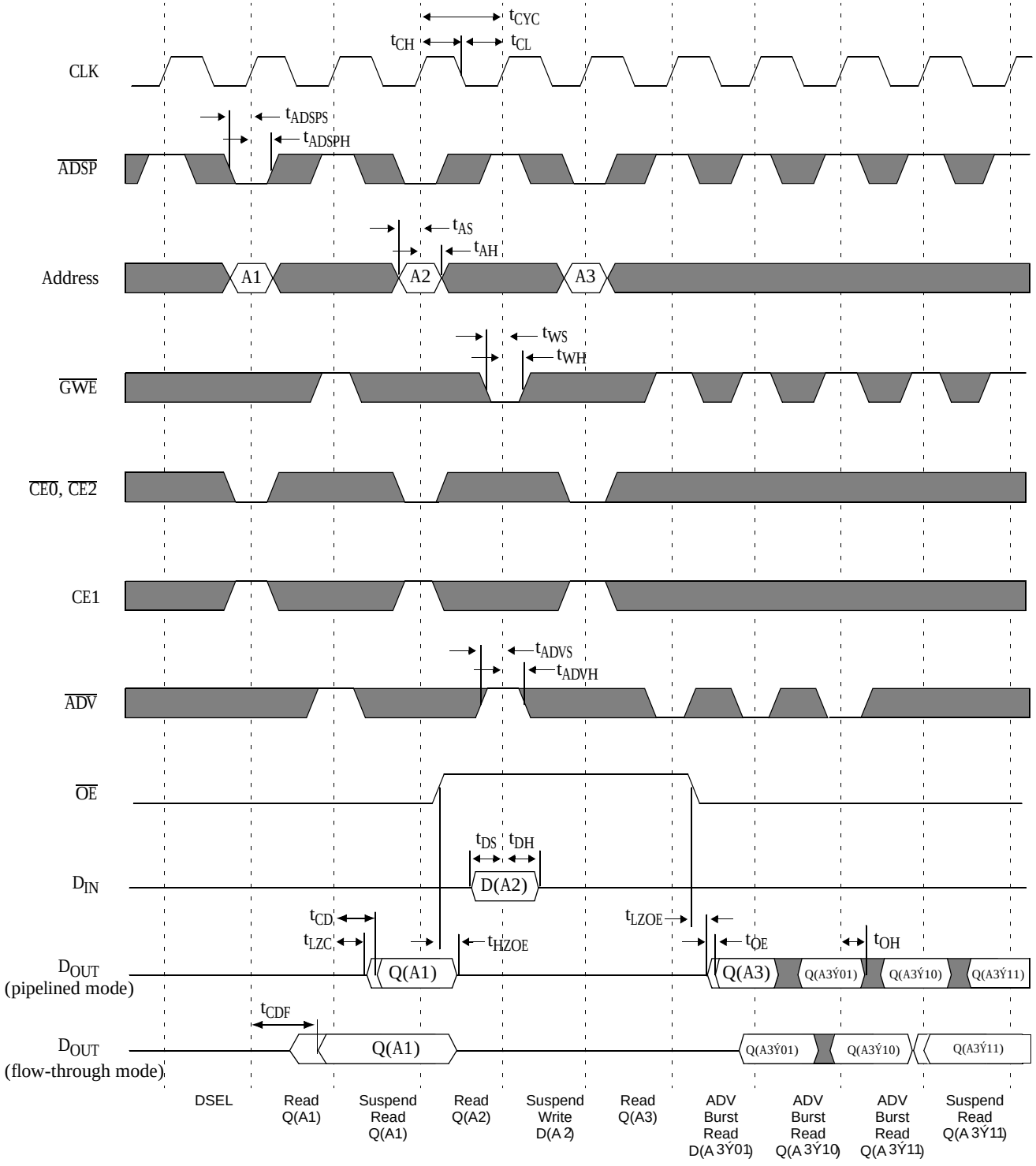
Note: Ý = XOR when $\overline{LBO}$ = high / no connect; Ý = ADD when $\overline{LBO}$ = low.
$\overline{BW[a:b]}$ is don't care.

Timing waveform of write cycle



Note: Ý = XOR when $\overline{LBO}$ = high/no connect; Ý = ADD when $\overline{LBO}$ = low.

Timing waveform of read/write cycle



Note: Ý = XOR when $\overline{LBO}$ = high/no connect; Ý = ADD when $\overline{LBO}$ = low.

AC test conditions

- Output load: For t_{LZC}, t_{LZOE}, t_{HZOE}, t_{HZC}, see Figure C. For all others, see Figure B.
- Input pulse level: GND to 3V. See Figure A.
- Input rise and fall time (measured at 0.3V and 2.7V): 2 ns. See Figure A.
- Input and output timing reference levels: 1.5V.

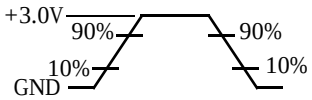


Figure A: Input waveform

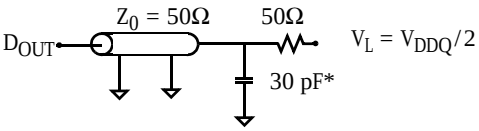


Figure B: Output load (A)

Thevenin equivalent:

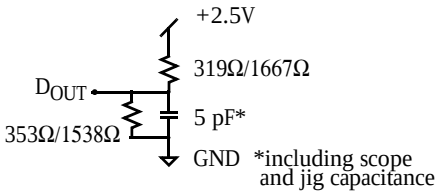


Figure C: Output load(B)

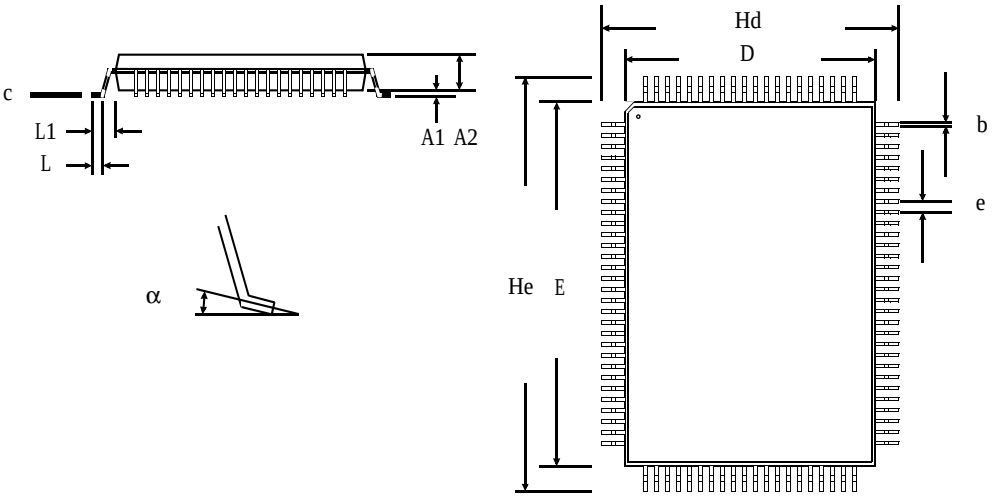
Notes

1 For test conditions, see "AC Test Conditions", Figures A, B, and C.
2 This parameter is measured with output load condition in Figure C.
3 This parameter is sampled but not 100% tested.
4 t_{HZOE} is less than t_{LZOE}, and t_{HZC} is less than t_{LZC} at any given temperature and voltage.
5 t_{CH} is measured as high above VIH, and t_{CL} is measured as low below VIL.
6 This is a synchronous device. All addresses must meet the specified setup and hold times for all rising edges of CLK. All other synchronous inputs must meet the setup and hold times for all rising edges of CLK when chip is enabled.
7 Write refers to $\overline{GWE}$, $\overline{BWE}$, and $\overline{BW[a,b]}$.
8 Chip select refers to $\overline{CE0}$, CE1, and $\overline{CE2}$.

Package dimensions

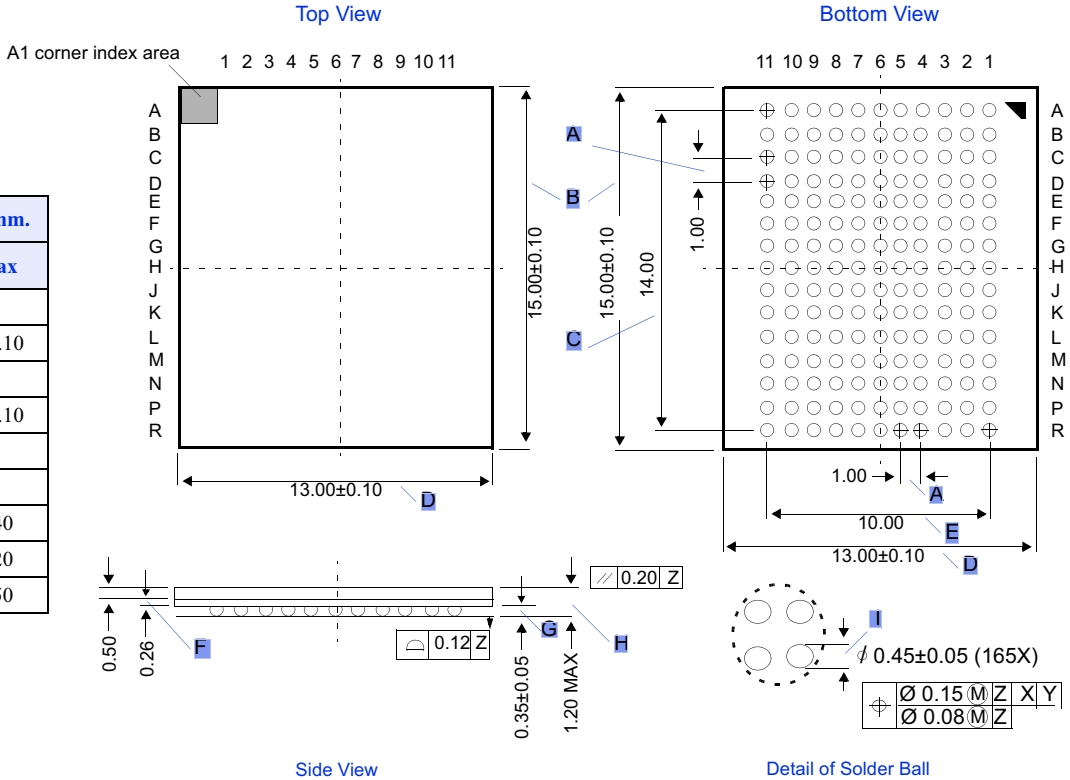
100-pin TQFP (quad flat pack)

	TQFP	
	Min	Max
A1	0.05	0.15
A2	1.35	1.45
b	0.22	0.38
c	0.09	0.20
D	13.90	14.10
E	19.90	20.10
e	0.65 nominal	
Hd	15.90	16.10
He	21.90	22.10
L	0.45	0.75
L1	1.00 nominal	
α	0°	7°
Dimensions in millimeters		



165-ball BGA (ball grid array)

All measurements are in mm.			
	Min	Typ	Max
A		1.00	
B	14.90	15.00	15.10
C		14.00	
D	12.90	13.00	13.10
E		10.00	
F		0.26	
G	0.30	0.35	0.40
H			1.20
I	0.40	0.45	0.50



Ordering information

Package &Width	-250 H MHz	–225 MHz	–200 MHz	–166 MHz
TQFP x18	AS7C251MPFS18A -250TQC	AS7C251MPFS18A -225TQC	AS7C251MPFS18A -200TQC	AS7C251MPFS18A -166TQC
		AS7C251MPFS18A -225TQI	AS7C251MPFS18A -200TQI	AS7C251MPFS18A -166TQI
BGA x18	AS7C251MPFS18A -250BC	AS7C251MPFS18A -225BC	AS7C251MPFS18A -200BC	AS7C251MPFS18A -166BC
		AS7C251MPFS18A -225BI	AS7C251MPFS18A -200BI	AS7C251MPFS18A -166BI

Part numbering guide

AS7C	25	1M	PF	S	18	A	–XXX	TQ or B	C / I
1	2	3	4	5	6	7	8	9	10

1. Alliance Semiconductor SRAM prefix
2. Operating voltage: 25 = 2.5V
3. Organization: 1M
4. Pipelined / flow-through mode (each device works in both modes)
5. Deselect: S = single cycle deselect
6. Organization: 18 = x18
7. Production version: A = first production version
8. Clock speed (MHz)
9. Package type: TQ = TQFP; B = BGA
10. Operating temperature: C = commercial (0° C to 70° C); I = industrial (-40° C to 85° C)