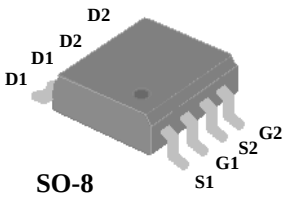
AP4532GM

RoHS-compliant Product

Advanced Power Electronics Corp.

N AND P-CHANNEL ENHANCEMENT MODE POWER MOSFET

- **Simple Drive Requirement**
- **Low On-resistance**
- **Fast Switching Characteristic**



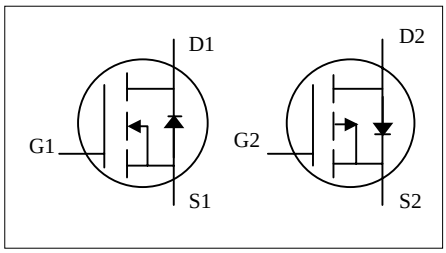
SO-8

N-CH	BV_{DSS}	30V
	$R_{DS(ON)}$	50mΩ
	I_D	5A
P-CH	BV_{DSS}	-30V
	$R_{DS(ON)}$	70mΩ
	I_D	-4A

Description

Advanced Power MOSFETs from APEC provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The SO-8 package is widely preferred for all commercial-industrial surface mount applications and suited for low voltage applications such as DC/DC converters.



Absolute Maximum Ratings

Symbol	Parameter	Rating		Units
		N-channel	P-channel	
V_{DS}	Drain-Source Voltage	30	-30	V
V_{GS}	Gate-Source Voltage	±20	±20	V
I_D@T_A=25℃	Continuous Drain Current[3]	5	-4	A
I_D@T_A=70℃	Continuous Drain Current[3]	4	-3.2	A
I_{DM}	Pulsed Drain Current[1]	20	-20	A
P_D@T_A=25℃	Total Power Dissipation	2		W
	Linear Derating Factor	0.016		W/℃
T_{STG}	Storage Temperature Range	-55 to 150		℃
T_J	Operating Junction Temperature Range	-55 to 150		℃

Thermal Data

Symbol	Parameter	Value	Unit
Rthj-amb	Maximum Thermal Resistance, Junction-ambient[3]	62.5	℃/W

N-CH Electrical Characteristics@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250uA	30	-	-	V
$\Delta BV_{DSS}/\Delta T_j$	Breakdown Voltage Temperature Coefficient	Reference to 25℃, I_D=1mA	-	0.037	-	V/℃
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=10V, I_D=5A	-	-	50	mΩ
		V_{GS}=4.5V, I_D=4.2A	-	-	70	mΩ
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250uA	1	-	3	V
g_{fs}	Forward Transconductance	V_{DS}=10V, I_D=5A	-	8	-	S
I_{DSS}	Drain-Source Leakage Current	V_{DS}=30V, V_{GS}=0V	-	-	1	uA
	Drain-Source Leakage Current (T_j=70°C)	V_{DS}=24V, V_{GS}=0V	-	-	25	uA
I_{GSS}	Gate-Source Leakage	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA
Q_g	Total Gate Charge[2]	I_D=5A	-	10.2	-	nC
Q_{gs}	Gate-Source Charge	V_{DS}=10V	-	1.2	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge	V_{GS}=10V	-	3.4	-	nC
$t_{d(on)}$	Turn-on Delay Time[2]	V_{DS}=10V	-	6	-	ns
t_r	Rise Time	I_D=1A	-	9	-	ns
$t_{d(off)}$	Turn-off Delay Time	R_G=6Ω,V_{GS}=10V	-	15	-	ns
t_f	Fall Time	R_D=10Ω	-	5.5	-	ns
C_{iss}	Input Capacitance	V_{GS}=0V	-	240	-	pF
C_{oss}	Output Capacitance	V_{DS}=25V	-	145	-	pF
C_{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	55	-	pF

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
I_S	Continuous Source Current (Body Diode)	V_D=V_G=0V , V_S=1.2V	-	-	1.7	A
V_{SD}	Forward On Voltage[2]	T_j=25℃, I_S=1.7A, V_{GS}=0V	-	-	1.2	V

P-CH Electrical Characteristics@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250uA	-30	-	-	V
$\Delta BV_{DSS}/\Delta T_j$	Breakdown Voltage Temperature Coefficient	Reference to 25℃, I_D=-1mA	-	-0.028	-	V/℃
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=-10V, I_D=-4A	-	-	70	mΩ
		V_{GS}=-4.5V, I_D=-3A	-	-	90	mΩ
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=-250uA	-1	-	-3	V
g_{fs}	Forward Transconductance	V_{DS}=-10V, I_D=-4A	-	5	-	S
I_{DSS}	Drain-Source Leakage Current	V_{DS}=-30V, V_{GS}=0V	-	-	-1	uA
	Drain-Source Leakage Current (T_j=70°C)	V_{DS}=-24V, V_{GS}=0V	-	-	-25	uA
I_{GSS}	Gate-Source Leakage	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA
Q_g	Total Gate Charge[2]	I_D=-4A	-	18.3	-	nC
Q_{gs}	Gate-Source Charge	V_{DS}=-10V	-	3.6	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge	V_{GS}=-10V	-	1.5	-	nC
$t_{d(on)}$	Turn-on Delay Time[2]	V_{DS}=-10V	-	8	-	ns
t_r	Rise Time	I_D=-1A	-	9	-	ns
$t_{d(off)}$	Turn-off Delay Time	R_G=6Ω,V_{GS}=-10V	-	21	-	ns
t_f	Fall Time	R_D=10Ω	-	10	-	ns
C_{iss}	Input Capacitance	V_{GS}=0V	-	760	-	pF
C_{oss}	Output Capacitance	V_{DS}=-25V	-	345	-	pF
C_{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	90	-	pF

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
I_S	Continuous Source Current (Body Diode)	V_D=V_G=0V , V_S=-1.2V	-	-	-1.7	A
V_{SD}	Forward On Voltage[2]	T_j=25℃, I_S=-1.7A, V_{GS}=0V	-	-	-1.2	V

Notes:

1.Pulse width limited by Max. junction temperature.

2.Pulse width ≤300us , duty cycle ≤2%.

3.Surface mounted on 1 in^2 copper pad of FR4 board, t ≤10sec ; 135 ℃/W when mounted on Min. copper pad.

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

APEC DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

APEC RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN.

N-Channel

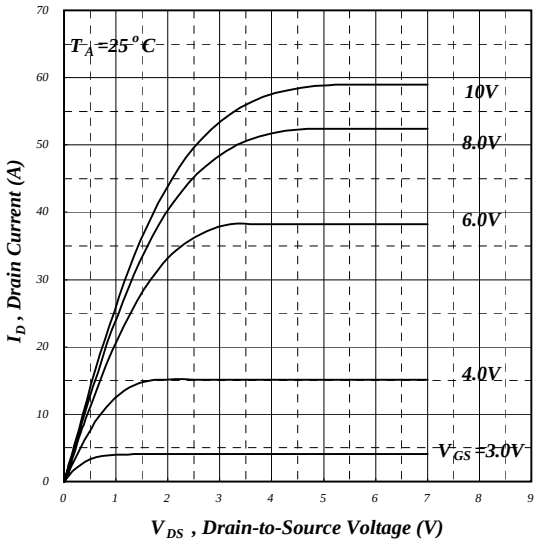


Fig 1. Typical Output Characteristics

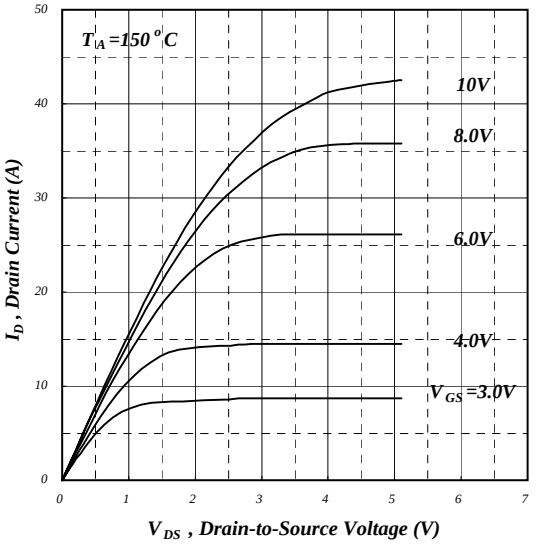


Fig 2. Typical Output Characteristics

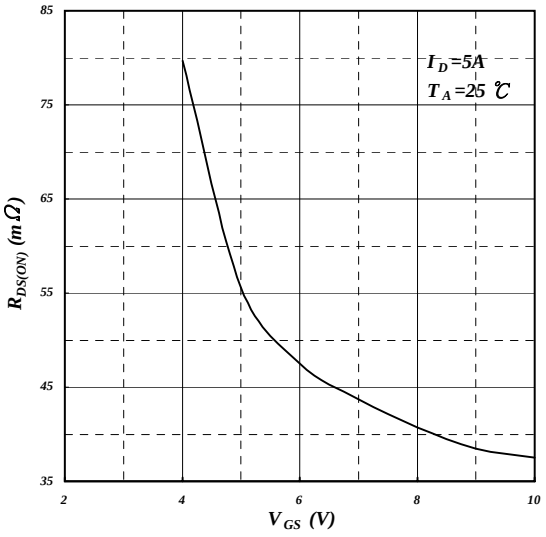


Fig 3. On-Resistance v.s. Gate Voltage

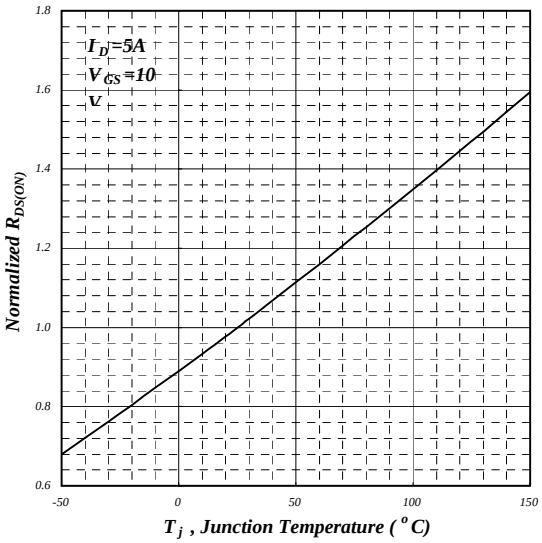


Fig 4. Normalized On-Resistance v.s. Junction Temperature

N-Channel

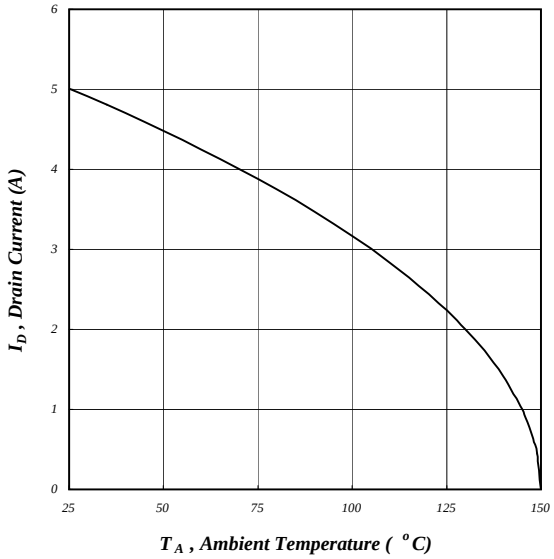


Fig 5. Maximum Drain Current v.s. Case Temperature

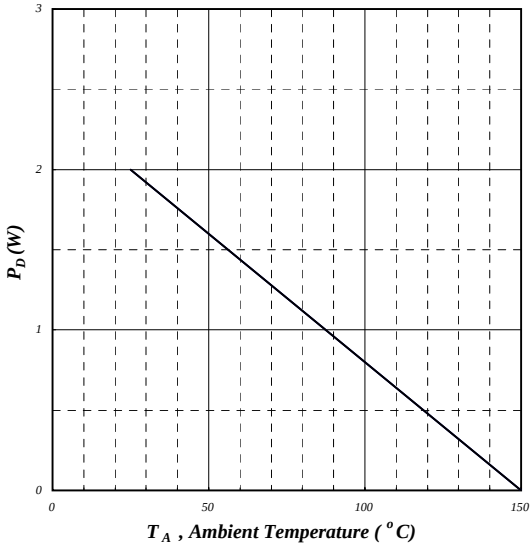


Fig 6. Typical Power Dissipation

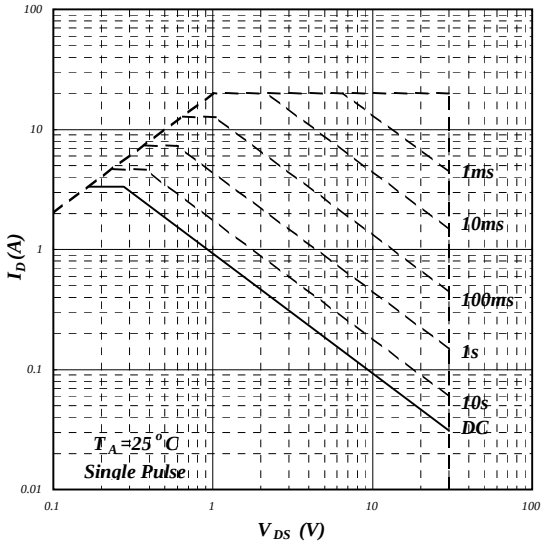


Fig 7. Maximum Safe Operating Area

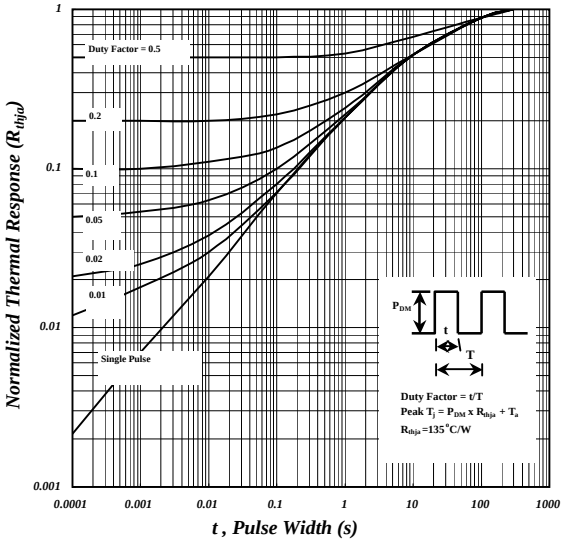


Fig 8. Effective Transient Thermal Impedance

N-Channel

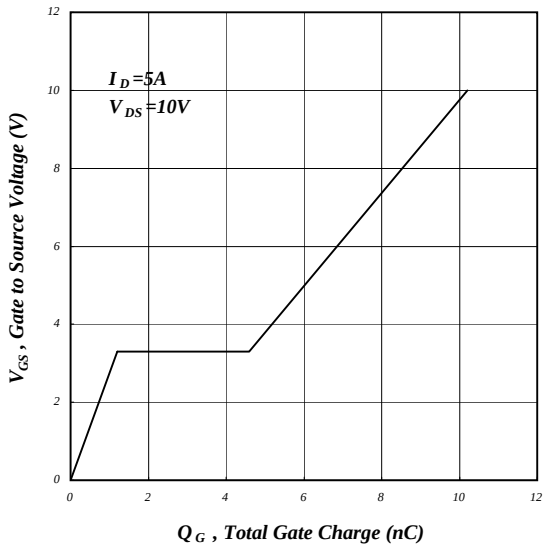


Fig 9. Gate Charge Characteristics

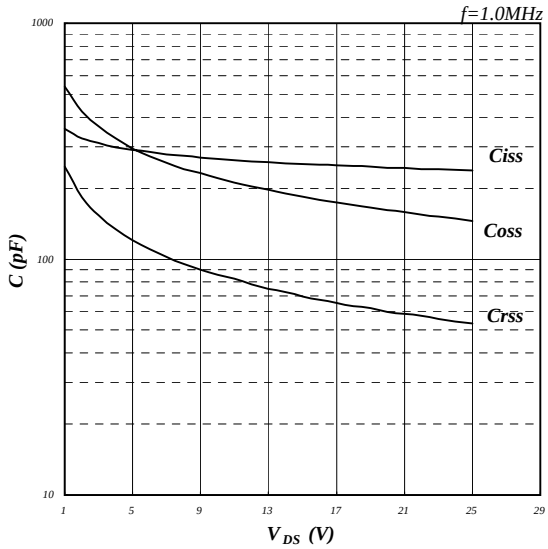


Fig 10. Typical Capacitance Characteristics

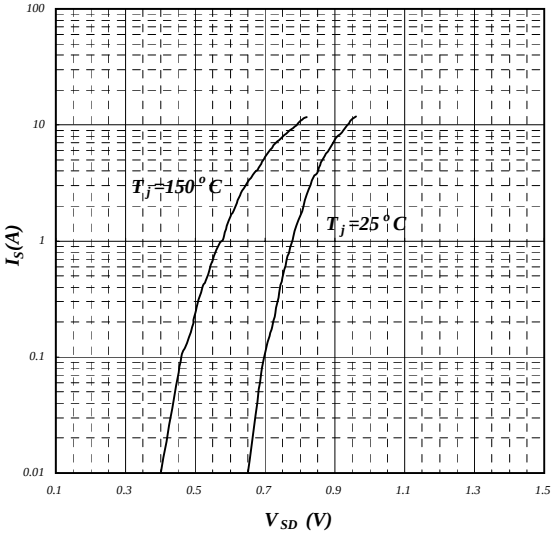


Fig 11. Forward Characteristic of Reverse Diode

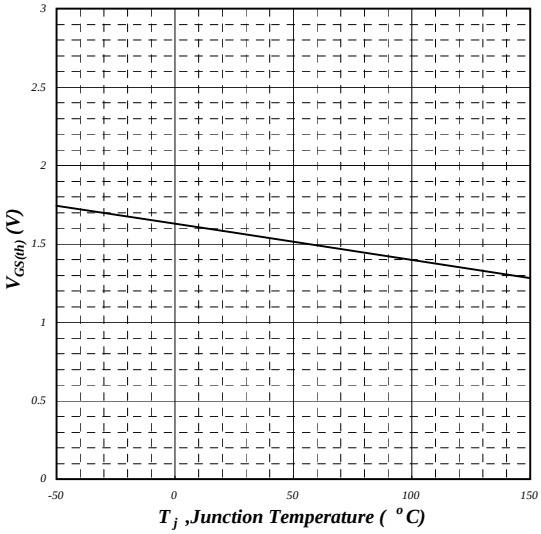


Fig 12. Gate Threshold Voltage v.s. Junction Temperature

N-Channel

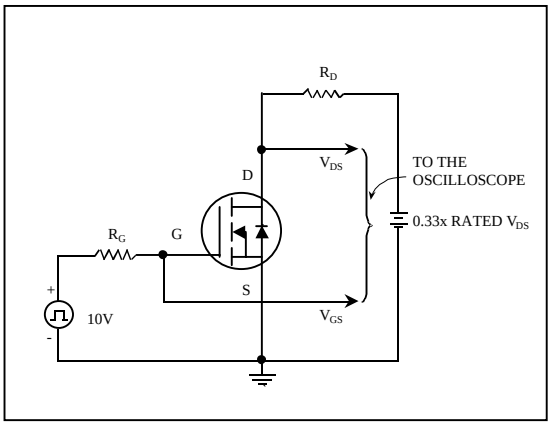


Fig 13. Switching Time Circuit

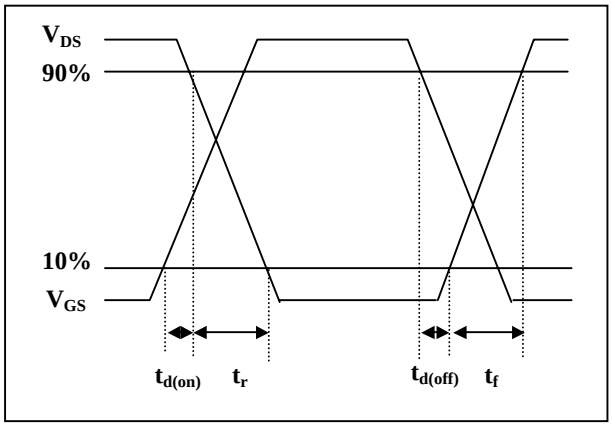


Fig 14. Switching Time Waveform

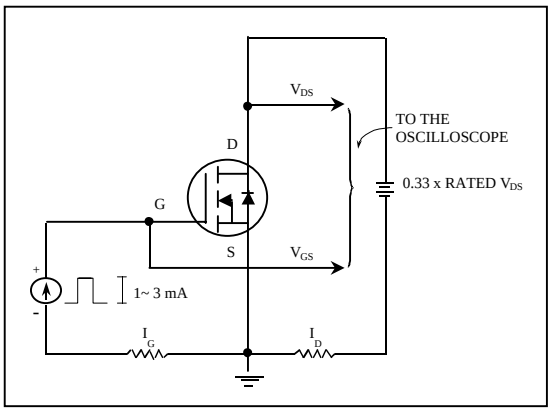


Fig 15. Gate Charge Circuit

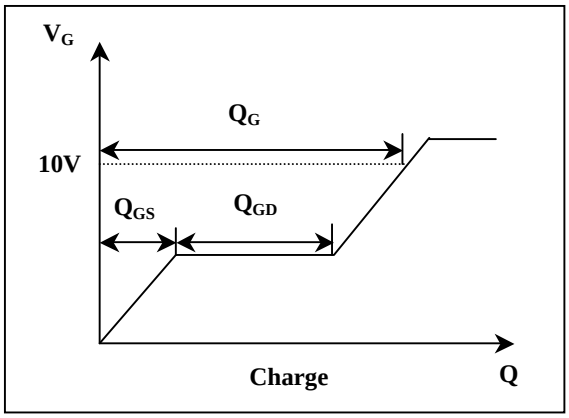


Fig 16. Gate Charge Waveform

P-Channel

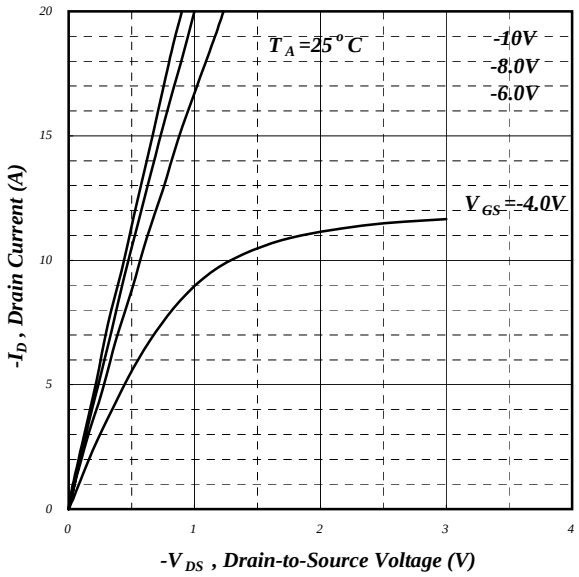


Fig 1. Typical Output Characteristics

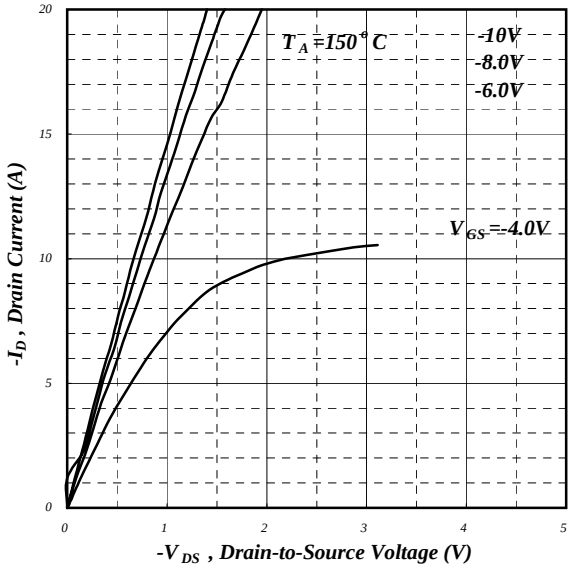


Fig 2. Typical Output Characteristics

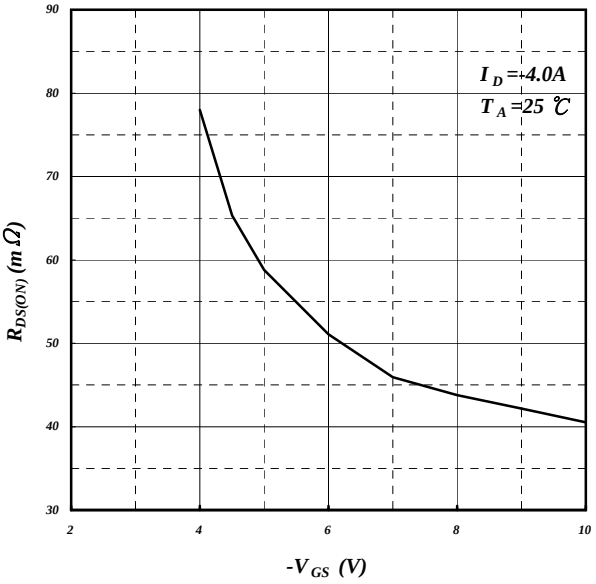


Fig 3. On-Resistance v.s. Gate Voltage

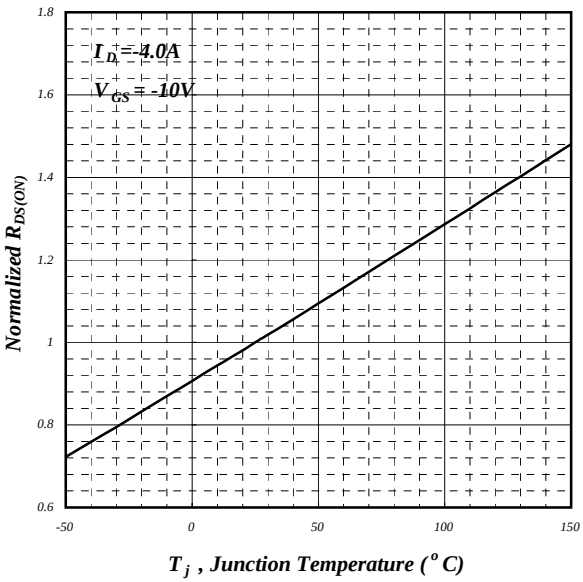


Fig 4. Normalized On-Resistance v.s. Junction Temperature

P-Channel

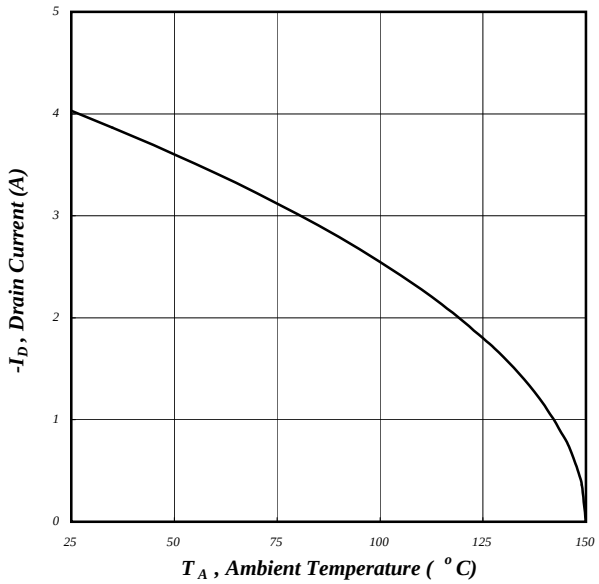


Fig 5. Maximum Drain Current v.s. Case Temperature

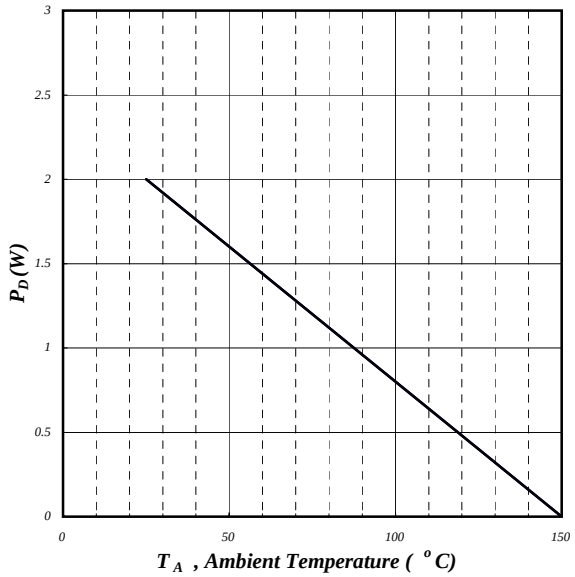


Fig 6. Typical Power Dissipation

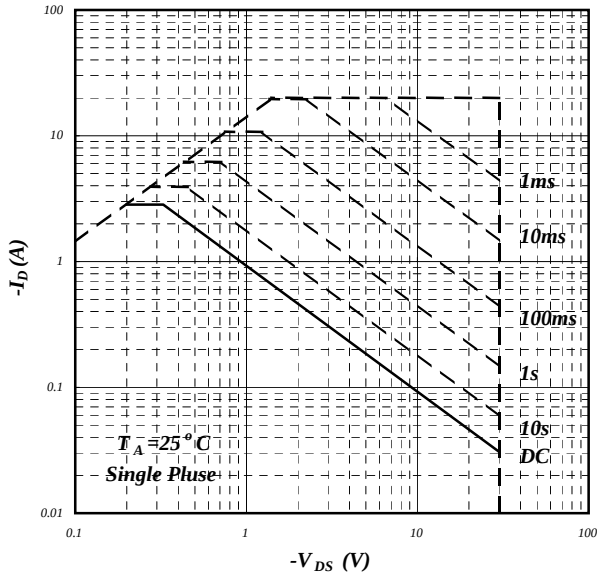


Fig 7. Maximum Safe Operating Area

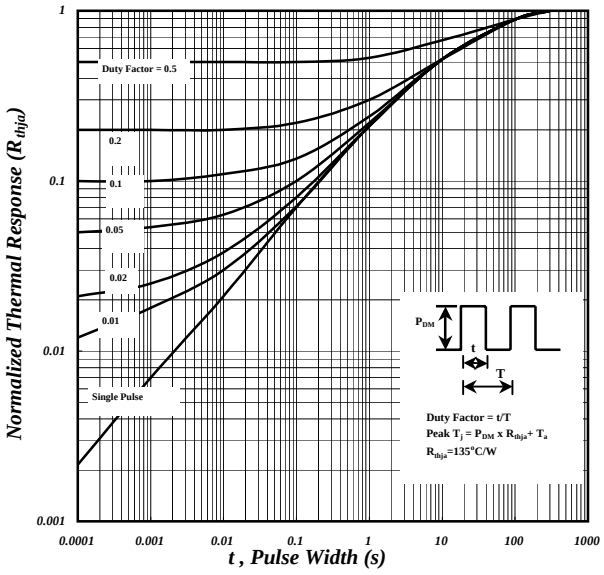


Fig 8. Effective Transient Thermal Impedance

P-Channel

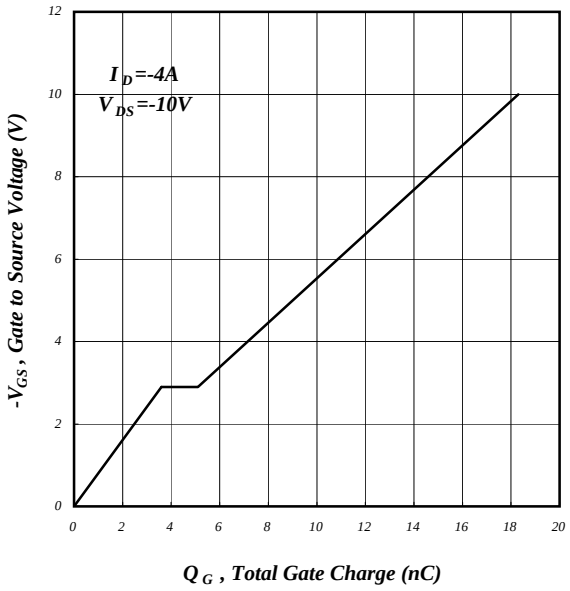


Fig 9. Gate Charge Characteristics

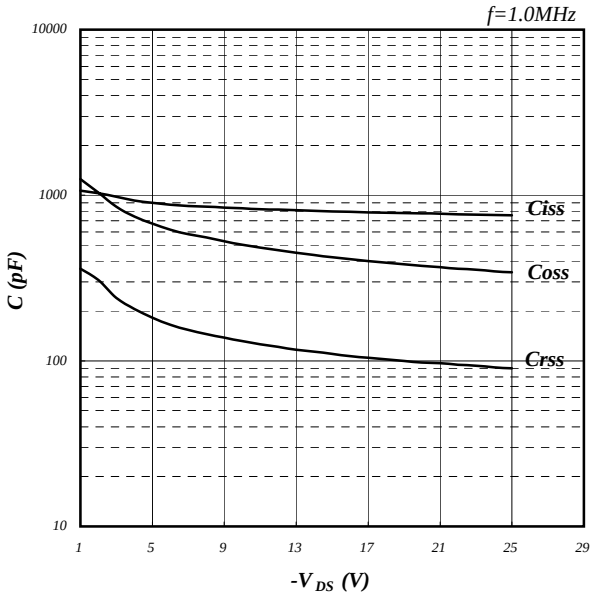


Fig 10. Typical Capacitance Characteristics

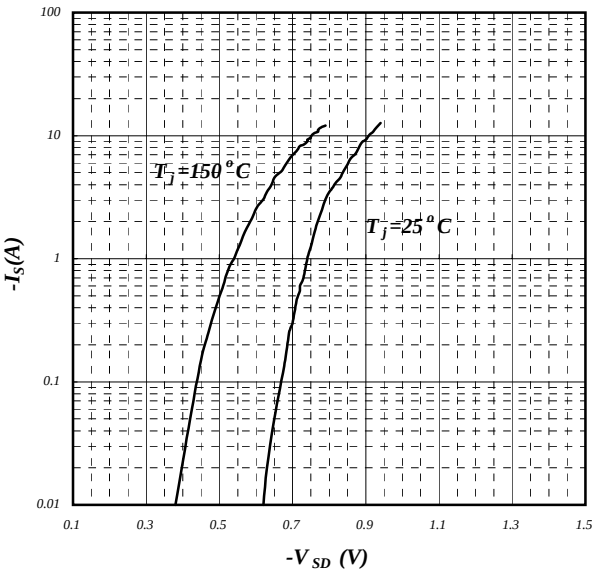


Fig 11. Forward Characteristic of Reverse Diode

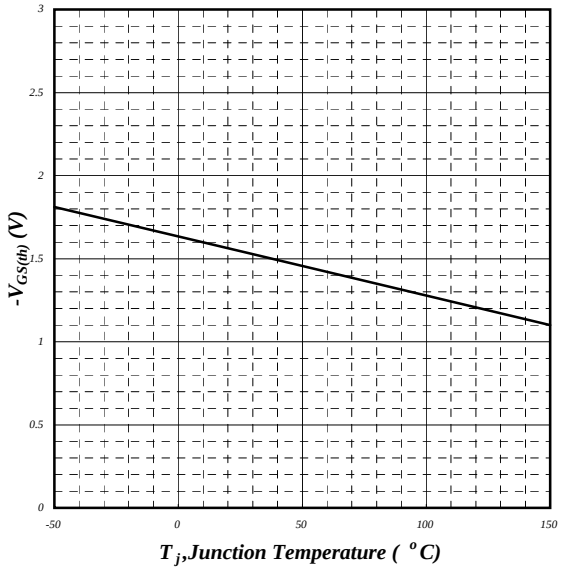


Fig 12. Gate Threshold Voltage v.s. Junction Temperature

P-Channel

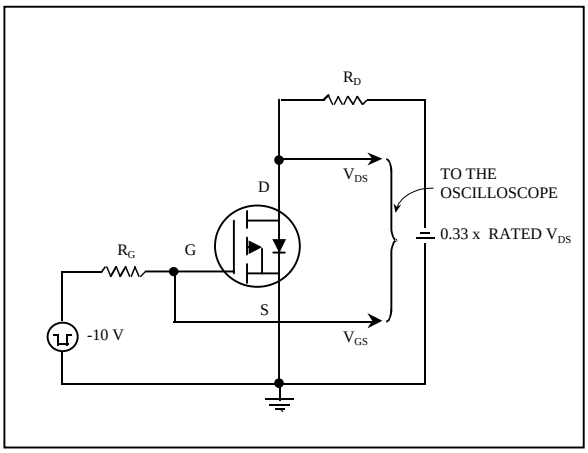


Fig 13. Switching Time Circuit

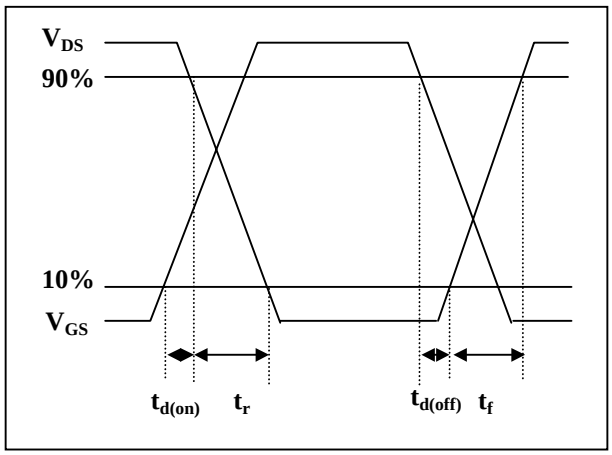


Fig 14. Switching Time Waveform

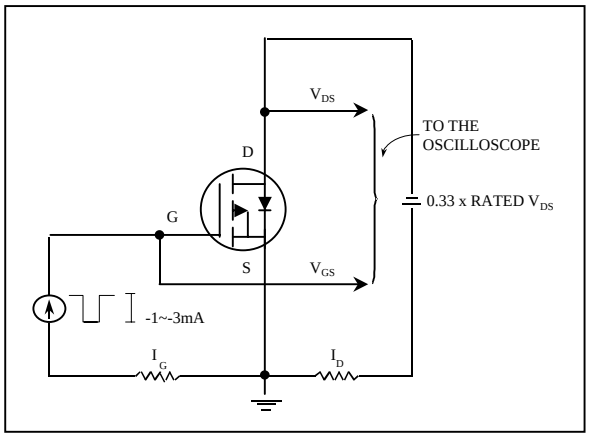


Fig 15. Gate Charge Circuit

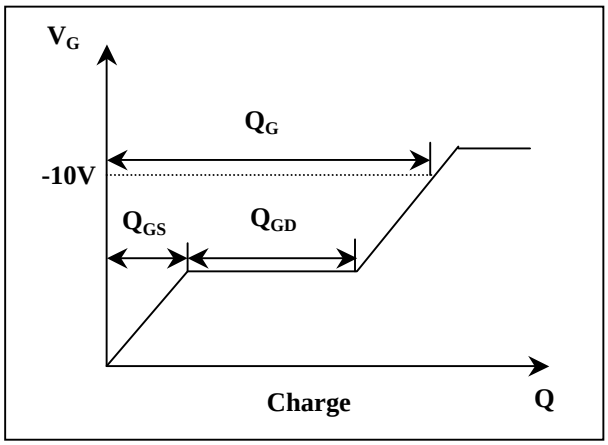


Fig 16. Gate Charge Waveform