

18Mb B-die Sync. SRAM Specification

**100TQFP with Pb & Pb-Free
(RoHS compliant)**

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Document Title

512Kx36 & 1Mx18-Bit Synchronous Burst SRAM

Revision History

<u>Rev.No.</u>	<u>History</u>	<u>Draft Date</u>	<u>Remark</u>
0.0	1. Initial draft	Mar. 23. 2004	Advance
0.1	1. Update the DC current spec(Icc, ISB)	May. 21, 2004	Preliminary
0.2	1. Change the ISB,ISB1,ISB2 - ISB ; from 120mA to 170mA - ISB1 ; from 80mA to 150mA - ISB2 ; from 80mA to 130mA	Sep. 21. 2004	Preliminary
0.3	1. Remove the 1.8V Vdd voltage level	Oct. 18, 2004	Preliminary
0.4	1. Remove the -85 speed bin	Jan. 04, 2005	Preliminary
1.0	1. Finalize the datasheet	July 18, 2005	Final

16Mb SB/SPB Synchronous SRAM Ordering Information

Org.	Part Number	Mode	VDD	Speed SB ; Access Time(ns) SPB ; Cycle Time(MHz)	PKG	Temp
1Mx18	K7B161835B-Q(P)C(I)75	SB	3.3/2.5	7.5ns	Q : 100TQFP P : Lead free 100TQFP	C ; Commercial Temp.Range
	K7A161830B-Q(P)C(I)25/16	SPB(2E1D)	3.3/2.5	250/167MHz		
	K7A161831B-Q(P)C(I)20	SPB(2E2D)	3.3/2.5	200MHz		
512Kx36	K7B163635B-Q(P)C(I)75	SB	3.3/2.5	7.5ns		I ; Industrial Temp.Range
	K7A163630B-Q(P)C(I)25/16	SPB(2E1D)	3.3/2.5	250/167MHz		
	K7A163631B-Q(P)C(I)20	SPB(2E2D)	3.3/2.5	200MHz		

512Kx36 & 1Mx18-Bit Synchronous Burst SRAM

FEATURES

- Synchronous Operation.
- On-Chip Address Counter.
- Self-Timed Write Cycle.
- On-Chip Address and Control Registers.
- $V_{DD} = 2.5$ or $3.3V \pm 5\%$ Power Supply.
- 5V Tolerant Inputs Except I/O Pins.
- Byte Writable Function.
- Global Write Enable Controls a full bus-width write.
- Power Down State via ZZ Signal.
- \overline{LBO} Pin allows a choice of either a interleaved burst or a linear burst.
- Three Chip Enables for simple depth expansion with No Data Contention only for TQFP.
- Asynchronous Output Enable Control.
- ADSP, ADSC, ADV Burst Control Pins.
- TTL-Level Three-State Output.
- 100-TQFP-1420A (Lead and Lead free package)
- Operating in commercial and industrial temperature range.

GENERAL DESCRIPTION

The K7B163635B and K7B161835B are 18,874,368-bit Synchronous Static Random Access Memory designed for high performance second level cache of Pentium and Power PC based System.

It is organized as 512K(1M) words of 36(18) bits and integrates address and control registers, a 2-bit burst address counter and added some new functions for high performance cache RAM applications; \overline{GW} , \overline{BW} , \overline{LBO} , ZZ. Write cycles are internally self-timed and synchronous.

Full bus-width write is done by \overline{GW} , and each byte write is performed by the combination of \overline{WEx} and \overline{BW} when \overline{GW} is high. And with \overline{CS}_1 high, \overline{ADSP} is blocked to control signals.

Burst cycle can be initiated with either the address status processor(\overline{ADSP}) or address status cache controller(\overline{ADSC}) inputs. Subsequent burst addresses are generated internally in the system's burst sequence and are controlled by the burst address advance(\overline{ADV}) input.

\overline{LBO} pin is DC operated and determines burst sequence(linear or interleaved).

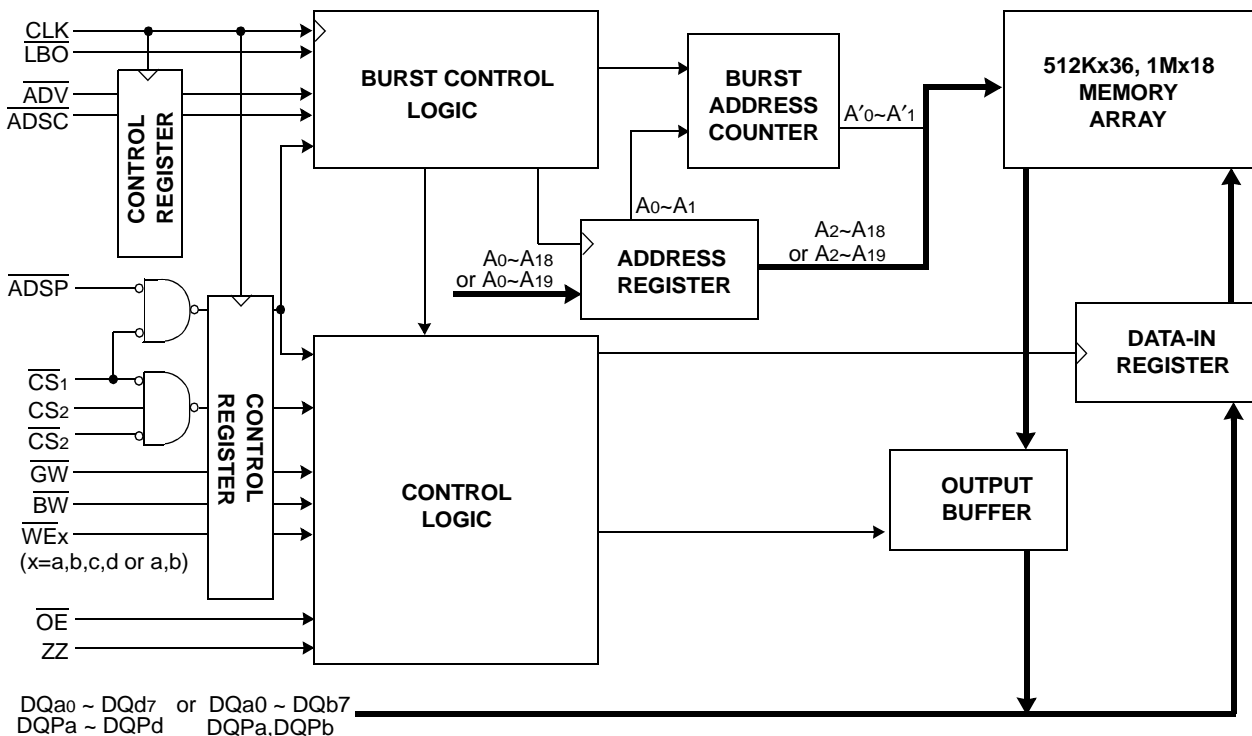
ZZ pin controls Power Down State and reduces Stand-by current regardless of CLK.

The K7B163635B and K7B161835B are fabricated using SAMSUNG's high performance CMOS technology and is available in a 100pin TQFP package. Multiple power and ground pins are utilized to minimize ground bounce.

FAST ACCESS TIMES

PARAMETER	Symbol	-75	Unit
Cycle Time	t _{CYC}	8.5	ns
Clock Access Time	t _{CD}	7.5	ns
Output Enable Access Time	t _{OE}	3.5	ns

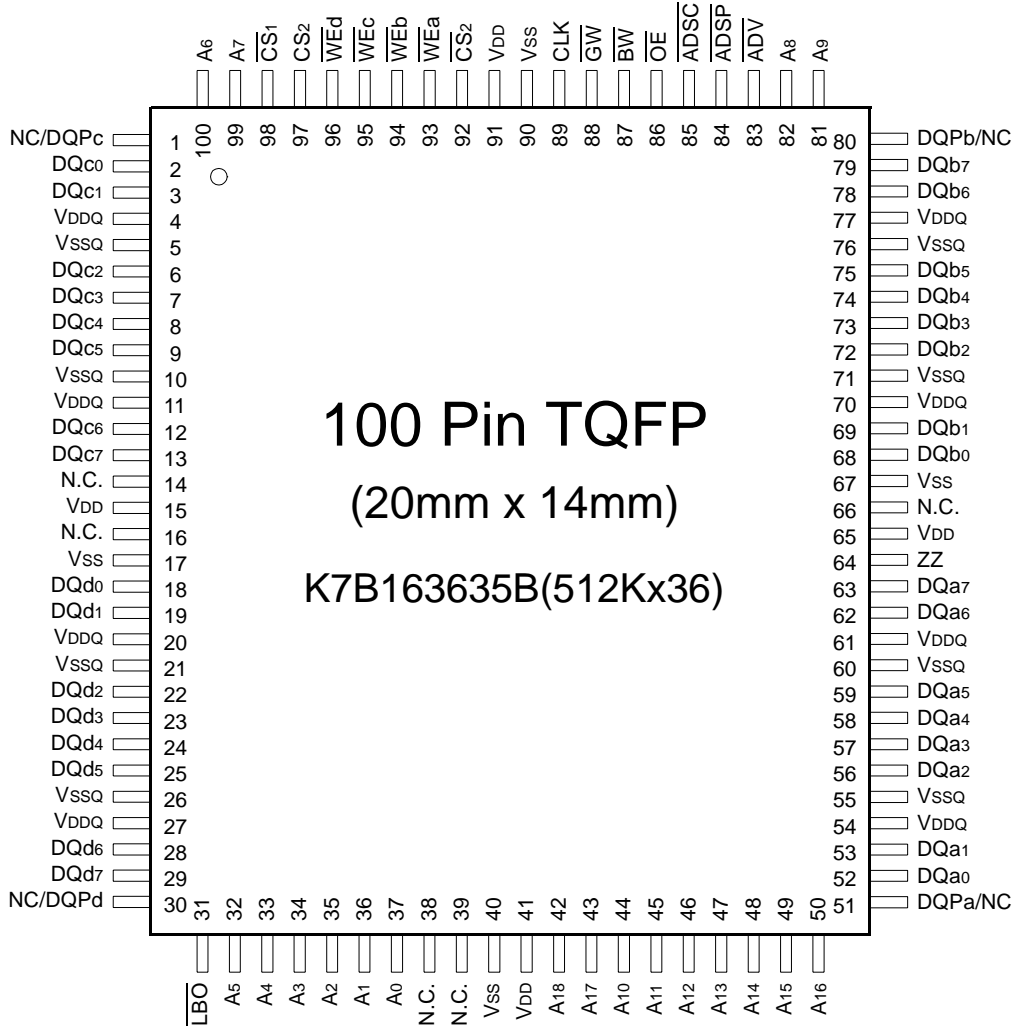
LOGIC BLOCK DIAGRAM



**K7B163635B
K7B161835B**

512Kx36 & 1Mx18 Synchronous SRAM www.DataSheet4U.com

PIN CONFIGURATION(TOP VIEW)



PIN NAME

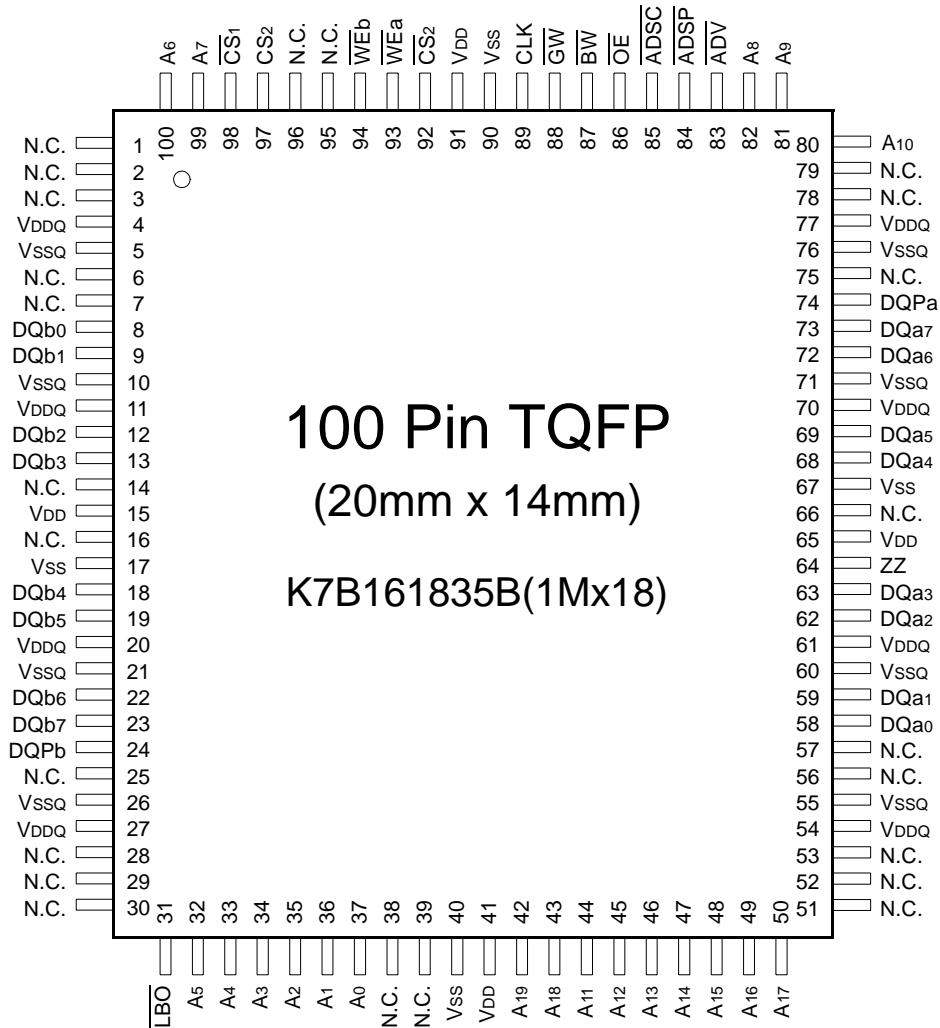
SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A0 - A18	Address Inputs	32,33,34,35,36,37,42 43,44,45,46,47,48,49 50,81,82,99,100	VDD	Power Supply(+3.3V)	15,41,65,91
			VSS	Ground	17,40,67,90
ADV	Burst Address Advance	83	N.C.	No Connect	14,16,38,39,66
ADSP	Address Status Processor	84			
ADSC	Address Status Controller	85	DQa0~a7	Data Inputs/Outputs	52,53,56,57,58,59,62,63
CLK	Clock	89	DQb0~b7		68,69,72,73,74,75,78,79
CS1	Chip Select	98	DQc0~c7		2,3,6,7,8,9,12,13
CS2	Chip Select	97	DQd0~d7		18,19,22,23,24,25,28,29
CS2	Chip Select	92	DQPa~Pd or NC		51,80,1,30
WEx(x=a,b,c,d)	Byte Write Inputs	93,94,95,96			
OE	Output Enable	86	VDDQ	Output Power Supply (2.5V or 3.3V)	4,11,20,27,54,61,70,77
GW	Global Write Enable	88	VSSQ	Output Ground	5,10,21,26,55,60,71,76
BW	Byte Write Enable	87			
ZZ	Power Down Input	64			
LBO	Burst Mode Control	31			

Notes : 1. A0 and A1 are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

**K7B163635B
K7B161835B**

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PIN CONFIGURATION(TOP VIEW)



PIN NAME

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A0 - A19	Address Inputs	32,33,34,35,36,37,42 43,44,45,46,47,48,49 50 80,81,82,99,100	VDD	Power Supply(+3.3V)	15,41,65,91
			Vss	Ground	17,40,67,90
			N.C.	No Connect	1,2,3,6,7,14,16,25,28,29, 30,38,39,51,52,53,56,57, 66,75,78,79,95,96
\overline{ADV}	Burst Address Advance	83	DQa0 ~ a7	Data Inputs/Outputs	58,59,62,63,68,69,72,73
\overline{ADSP}	Address Status Processor	84	DQb0 ~ b7		8,9,12,13,18,19,22,23
\overline{ADSC}	Address Status Controller	85	DQPa, Pb		74,24
CLK	Clock	89	VDDQ	Output Power Supply (2.5V or 3.3V)	4,11,20,27,54,61,70,77
$\overline{CS1}$	Chip Select	98	Vssq	Output Ground	5,10,21,26,55,60,71,76
$\overline{CS2}$	Chip Select	97			
$\overline{CS2}$	Chip Select	92			
$\overline{WE}x(x=a,b)$	Byte Write Inputs	93,94			
\overline{OE}	Output Enable	86			
\overline{GW}	Global Write Enable	88			
\overline{BW}	Byte Write Enable	87			
\overline{ZZ}	Power Down Input	64			
\overline{LBO}	Burst Mode Control	31			

Notes : 1. A0 and A1 are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

FUNCTION DESCRIPTION

The K7B163635B and K7B161835B are synchronous SRAM designed to support the burst address accessing sequence of the Power PC based microprocessor. All inputs (with the exception of \overline{OE} , \overline{LBO} and \overline{ZZ}) are sampled on rising clock edges. The start and duration of the burst access is controlled by \overline{ADSC} , \overline{ADSP} and \overline{ADV} and chip select pins. The accesses are enabled with the chip select signals and output enabled signals. Wait states are inserted into the access with \overline{ADV} .

When \overline{ZZ} is pulled high, the SRAM will enter a Power Down State. At this time, internal state of the SRAM is preserved. When \overline{ZZ} returns to low, the SRAM normally operates after 2cycles of wake up time. \overline{ZZ} pin is pulled down internally.

Read cycles are initiated with \overline{ADSP} (or \overline{ADSC}) using the new external address clocked into the on-chip address register when both \overline{GW} and \overline{BW} are high or when \overline{BW} is low and \overline{WEa} , \overline{WEb} , \overline{WEc} , and \overline{WEd} are high. When \overline{ADSP} is sampled low, the chip selects are sampled active, and the output buffer is enabled with \overline{OE} . the data of cell array accessed by the current address are projected to the output pins.

Write cycles are also initiated with \overline{ADSP} (or \overline{ADSC}) and are differentiated into two kinds of operations; All byte write operation and individual byte write operation.

All byte write occurs by enabling \overline{GW} (independent of \overline{BW} and \overline{WEx}), and individual byte write is performed only when \overline{GW} is high and \overline{BW} is low. In K7B163635B, a 512Kx36 organization, \overline{WEa} controls DQa0 ~ DQa7 and DQPa, \overline{WEb} controls DQb0 ~ DQb7 and DQPb, \overline{WEc} controls DQc0 ~ DQc7 and DQPc and \overline{WEd} controls DQd0 ~ DQd7 and DQPd.

$\overline{CS1}$ is used to enable the device and conditions internal use of \overline{ADSP} and is sampled only when a new external address is loaded.

\overline{ADV} is ignored at the clock edge when \overline{ADSP} is asserted, but can be sampled on the subsequent clock edges. The address increases internally for the next access of the burst when \overline{ADV} is sampled low.

Addresses are generated for the burst access as shown below, The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the \overline{LBO} pin. When this pin is Low, linear burst sequence is selected. And this pin is High, Interleaved burst sequence is selected.

BURST SEQUENCE TABLE

(Interleaved Burst)

\overline{LBO} PIN	HIGH	Case 1		Case 2		Case 3		Case 4	
		A1	A0	A1	A0	A1	A0	A1	A0
	First Address	0	0	0	1	1	0	1	1
	↓	0	1	0	0	1	1	1	0
	↓	1	0	1	1	0	0	0	1
	Fourth Address	1	1	1	0	0	1	0	0

(Linear Burst)

\overline{LBO} PIN	LOW	Case 1		Case 2		Case 3		Case 4	
		A1	A0	A1	A0	A1	A0	A1	A0
	First Address	0	0	0	1	1	0	1	1
	↓	0	1	1	0	1	1	0	0
	↓	1	0	1	1	0	0	0	1
	Fourth Address	1	1	0	0	0	1	1	0

Note : 1. \overline{LBO} pin must be tied to High or Low, and Floating State must not be allowed.

TRUTH TABLES

SYNCHRONOUS TRUTH TABLE

\overline{CS}_1	\overline{CS}_2	\overline{CS}_2	\overline{ADSP}	\overline{ADSC}	\overline{ADV}	\overline{WRITE}	CLK	ADDRESS ACCESSED	OPERATION
H	X	X	X	L	X	X	↑	N/A	Not Selected
L	L	X	L	X	X	X	↑	N/A	Not Selected
L	X	H	L	X	X	X	↑	N/A	Not Selected
L	L	X	X	L	X	X	↑	N/A	Not Selected
L	X	H	X	L	X	X	↑	N/A	Not Selected
L	H	L	L	X	X	X	↑	External Address	Begin Burst Read Cycle
L	H	L	H	L	X	L	↑	External Address	Begin Burst Write Cycle
L	H	L	H	L	X	H	↑	External Address	Begin Burst Read Cycle
X	X	X	H	H	L	H	↑	Next Address	Continue Burst Read Cycle
H	X	X	X	H	L	H	↑	Next Address	Continue Burst Read Cycle
X	X	X	H	H	L	L	↑	Next Address	Continue Burst Write Cycle
H	X	X	X	H	L	L	↑	Next Address	Continue Burst Write Cycle
X	X	X	H	H	H	H	↑	Current Address	Suspend Burst Read Cycle
H	X	X	X	H	H	H	↑	Current Address	Suspend Burst Read Cycle
X	X	X	H	H	H	L	↑	Current Address	Suspend Burst Write Cycle
H	X	X	X	H	H	L	↑	Current Address	Suspend Burst Write Cycle

- Notes :** 1. X means "Don't Care".
 2. The rising edge of clock is symbolized by ↑.
 3. $\overline{WRITE} = L$ means Write operation in WRITE TRUTH TABLE.
 $\overline{WRITE} = H$ means Read operation in WRITE TRUTH TABLE.
 4. Operation finally depends on status of asynchronous input pins(ZZ and \overline{OE}).

WRITE TRUTH TABLE (x36)

\overline{GW}	\overline{BW}	\overline{WE}_a	\overline{WE}_b	\overline{WE}_c	\overline{WE}_d	OPERATION
H	H	X	X	X	X	READ
H	L	H	H	H	H	READ
H	L	L	H	H	H	WRITE BYTE a
H	L	H	L	H	H	WRITE BYTE b
H	L	H	H	L	L	WRITE BYTE c and d
H	L	L	L	L	L	WRITE ALL BYTES
L	X	X	X	X	X	WRITE ALL BYTES

- Notes :** 1. X means "Don't Care".
 2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

WRITE TRUTH TABLE(x18)

\overline{GW}	\overline{BW}	\overline{WE}_a	\overline{WE}_b	OPERATION
H	H	X	X	READ
H	L	H	H	READ
H	L	L	H	WRITE BYTE a
H	L	H	L	WRITE BYTE b
H	L	L	L	WRITE ALL BYTES
L	X	X	X	WRITE ALL BYTES

- Notes :** 1. X means "Don't Care".
 2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

ASYNCHRONOUS TRUTH TABLE

Operation	ZZ	\overline{OE}	I/O STATUS
Sleep Mode	H	X	High-Z
Read	L	L	DQ
	L	H	High-Z
Write	L	X	Din, High-Z
Deselected	L	X	High-Z

Notes

1. X means "Don't Care".
2. ZZ pin is pulled down internally
3. For write cycles that following read cycles, the output buffers must be disabled with \overline{OE} , otherwise data bus contention will occur.
4. Sleep Mode means power down state of which stand-by current does not depend on cycle time.
5. Deselected means power down state of which stand-by current depends on cycle time.

ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT	
Voltage on VDD Supply Relative to Vss	VDD	-0.3 to 4.6	V	
Voltage on VDDQ Supply Relative to Vss	VDDQ	VDD	V	
Voltage on Input Pin Relative to Vss	VIN	-0.3 to VDD+0.3	V	
Voltage on I/O Pin Relative to Vss	VIO	-0.3 to VDDQ+0.3	V	
Power Dissipation	Pd	1.6	W	
Storage Temperature	TSTG	-65 to 150	°C	
Operating Temperature	Commercial	TOPR	0 to 70	°C
	Industrial	TOPR	-40 to 85	°C
Storage Temperature Range Under Bias	TBIAS	-10 to 85	°C	

*Note : Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING CONDITIONS (0°C ≤ TA ≤ 70°C)

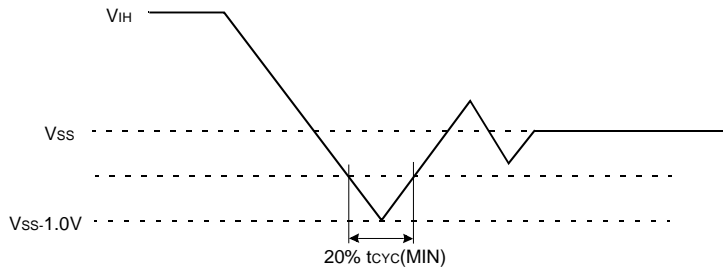
PARAMETER	SYMBOL	MIN	Typ.	MAX	UNIT
Supply Voltage	VDD1	2.375	2.5	2.625	V
	VDDQ1	2.375	2.5	2.625	V
	VDD2	3.135	3.3	3.465	V
	VDDQ2	3.135	3.3	3.465	V
Ground	VSS	0	0	0	V

- Notes: 1. The above parameters are also guaranteed at industrial temperature range.
2. It should be $VDDQ \leq VDD$

CAPACITANCE* (TA=25°C, f=1MHz)

PARAMETER	SYMBOL	TEST CONDITION	MIN	MAX	UNIT
Input Capacitance	CIN	VIN=0V	-	5	pF
Output Capacitance	COUT	VOUT=0V	-	6	pF

*Note : Sampled not 100% tested.



DC ELECTRICAL CHARACTERISTICS

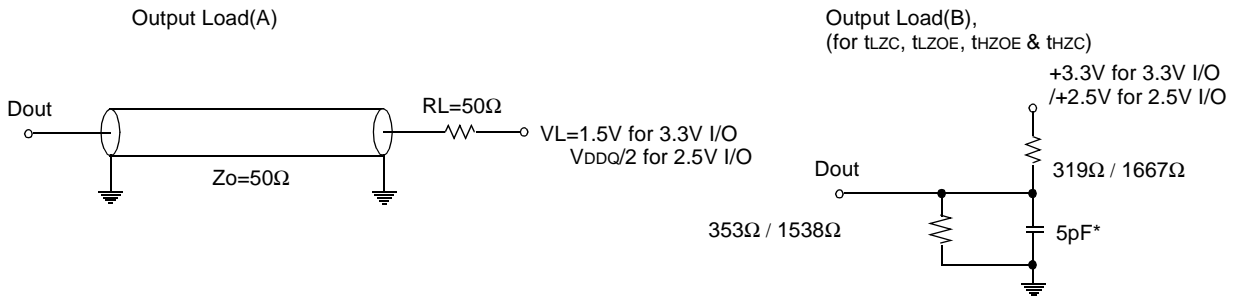
Parameter	Symbol	Test Conditions	Min	Max	Unit	Notes
Input Leakage Current(except ZZ)	IIL	VDD=Max ; VIN=VSS to VDD	-2	+2	μA	
Output Leakage Current	IOL	Output Disabled, Vout=VSS to VDDQ	-2	+2	μA	
Operating Current	ICC	Device Selected, IOUT=0mA, ZZ≤VIL, Cycle Time ≥ tcYC Min	-75	-	250	mA 1,2
Standby Current	ISB	Device deselected, IOUT=0mA, ZZ≤VIL, f=Max, All Inputs≤0.2V or ≥ VDD-0.2V	-75	-	170	mA
	ISB1	Device deselected, IOUT=0mA, ZZ≤0.2V, f=0, All Inputs=fixed (VDD-0.2V or 0.2V)	-	-	150	mA
	ISB2	Device deselected, IOUT=0mA, ZZ≥VDD-0.2V, f=Max, All Inputs≤VIL or ≥VIH	-	-	130	mA
Output Low Voltage(3.3V I/O)	VOL	IOL=8.0mA	-	0.4	V	
Output High Voltage(3.3V I/O)	VOH	IOH=-4.0mA	2.4	-	V	
Output Low Voltage(2.5V I/O)	VOL	IOL=1.0mA	-	0.4	V	
Output High Voltage(2.5V I/O)	VOH	IOH=-1.0mA	2.0	-	V	
Input Low Voltage(3.3V I/O)	VIL		-0.3*	0.8	V	
Input High Voltage(3.3V I/O)	VIH		2.0	VDD+0.3**	V	3
Input Low Voltage(2.5V I/O)	VIL		-0.3*	0.7	V	
Input High Voltage(2.5V I/O)	VIH		1.7	VDD+0.3**	V	3

- Notes :** 1. The above parameters are also guaranteed at industrial temperature range.
2. Reference AC Operating Conditions and Characteristics for input and timing.
3. Data states are all zero.
4. In Case of I/O Pins, the Max. VIH=VDDQ+0.3V

TEST CONDITIONS

PARAMETER	VALUE
Input Pulse Level(for 3.3V I/O)	0 to 3.0V
Input Pulse Level(for 2.5V I/O)	0 to 2.5V
Input Rise and Fall Time(Measured at 20% to 80% for 3.3/2.5V I/O)	1.0V/ns
Input and Output Timing Reference Levels for 3.3V I/O	1.5V
Input and Output Timing Reference Levels for 2.5V I/O	VDDQ/2
Output Load	See Fig. 1

* The above parameters are also guaranteed at industrial temperature range.



* Including Scope and Jig Capacitance

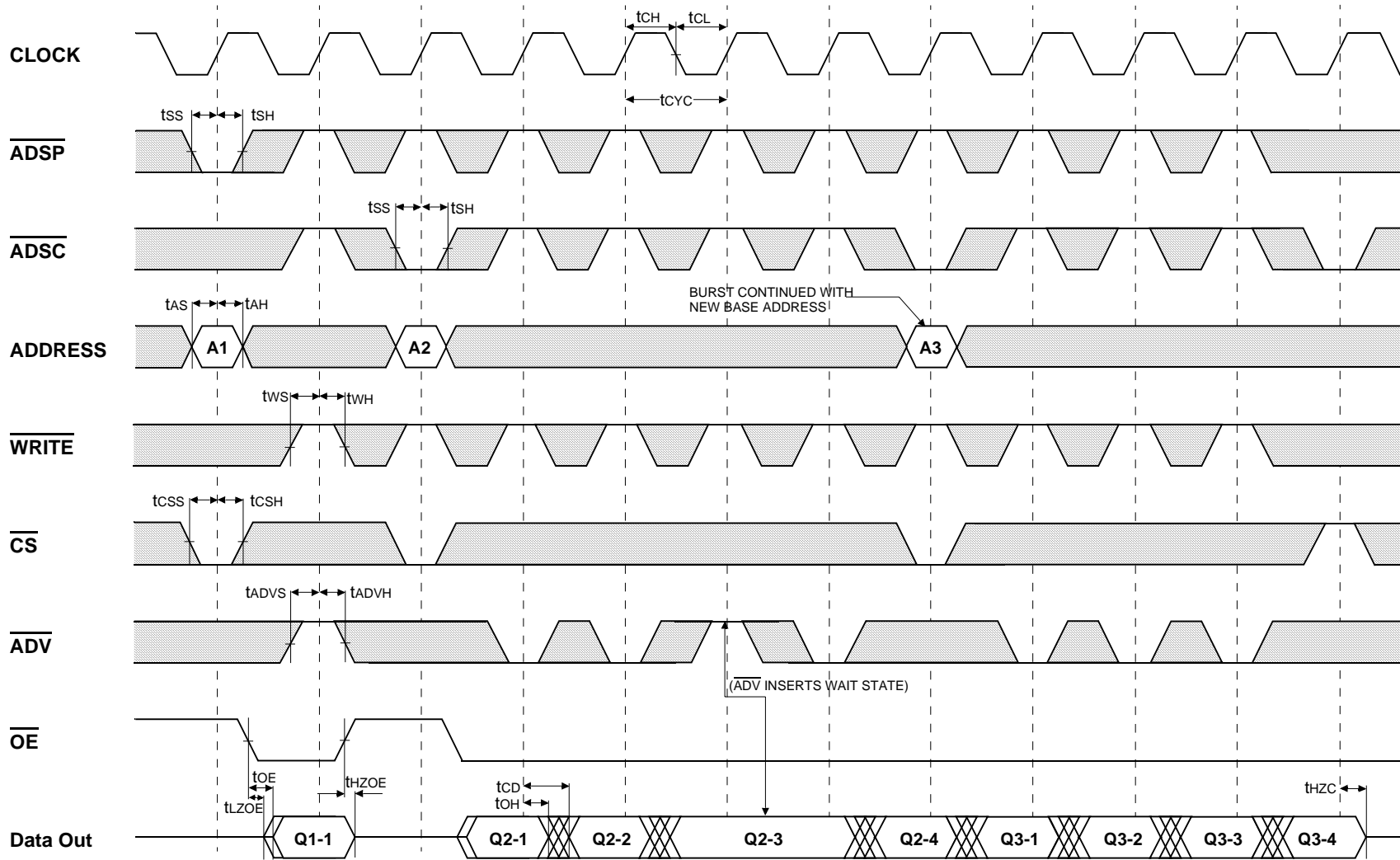
Fig. 1

AC TIMING CHARACTERISTICS

PARAMETER	SYMBOL	-75		UNIT
		MIN	MAX	
Cycle Time	tCYC	8.5	-	ns
Clock Access Time	tCD	-	7.5	ns
Output Enable to Data Valid	tOE	-	3.5	ns
Clock High to Output Low-Z	tLZC	2.5	-	ns
Output Hold from Clock High	tOH	2.5	-	ns
Output Enable Low to Output Low-Z	tLZOE	0	-	ns
Output Enable High to Output High-Z	tHZOE	-	3.5	ns
Clock High to Output High-Z	tHZC	-	4.0	ns
Clock High Pulse Width	tCH	2.5	-	ns
Clock Low Pulse Width	tCL	2.5	-	ns
Address Setup to Clock High	tAS	2.0	-	ns
Address Status Setup to Clock High	tSS	2.0	-	ns
Data Setup to Clock High	tDS	2.0	-	ns
Write Setup to Clock High (\overline{GW} , \overline{BW} , \overline{WEx})	tWS	2.0	-	ns
Address Advance Setup to Clock High	tADVS	2.0	-	ns
Chip Select Setup to Clock High	tCSS	2.0	-	ns
Address Hold from Clock High	tAH	0.5	-	ns
Address Status Hold from Clock High	tSH	0.5	-	ns
Data Hold from Clock High	tDH	0.5	-	ns
Write Hold from Clock High (\overline{GW} , \overline{BW} , \overline{WEx})	tWH	0.5	-	ns
Address Advance Hold from Clock High	tADVH	0.5	-	ns
Chip Select Hold from Clock High	tCSH	0.5	-	ns
ZZ High to Power Down	tPDS	2	-	cycle
ZZ Low to Power Up	tPUS	2	-	cycle

- Notes :**
1. The above parameters are also guaranteed at industrial temperature range.
 2. All address inputs must meet the specified setup and hold times for all rising clock edges whenever \overline{ADSC} and/or \overline{ADSP} is sampled low and \overline{CS} is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.
 3. Both chip selects must be active whenever \overline{ADSC} or \overline{ADSP} is sampled low in order for the this device to remain enabled.
 4. \overline{ADSC} or \overline{ADSP} must not be asserted for at least 2 Clock after leaving ZZ state.

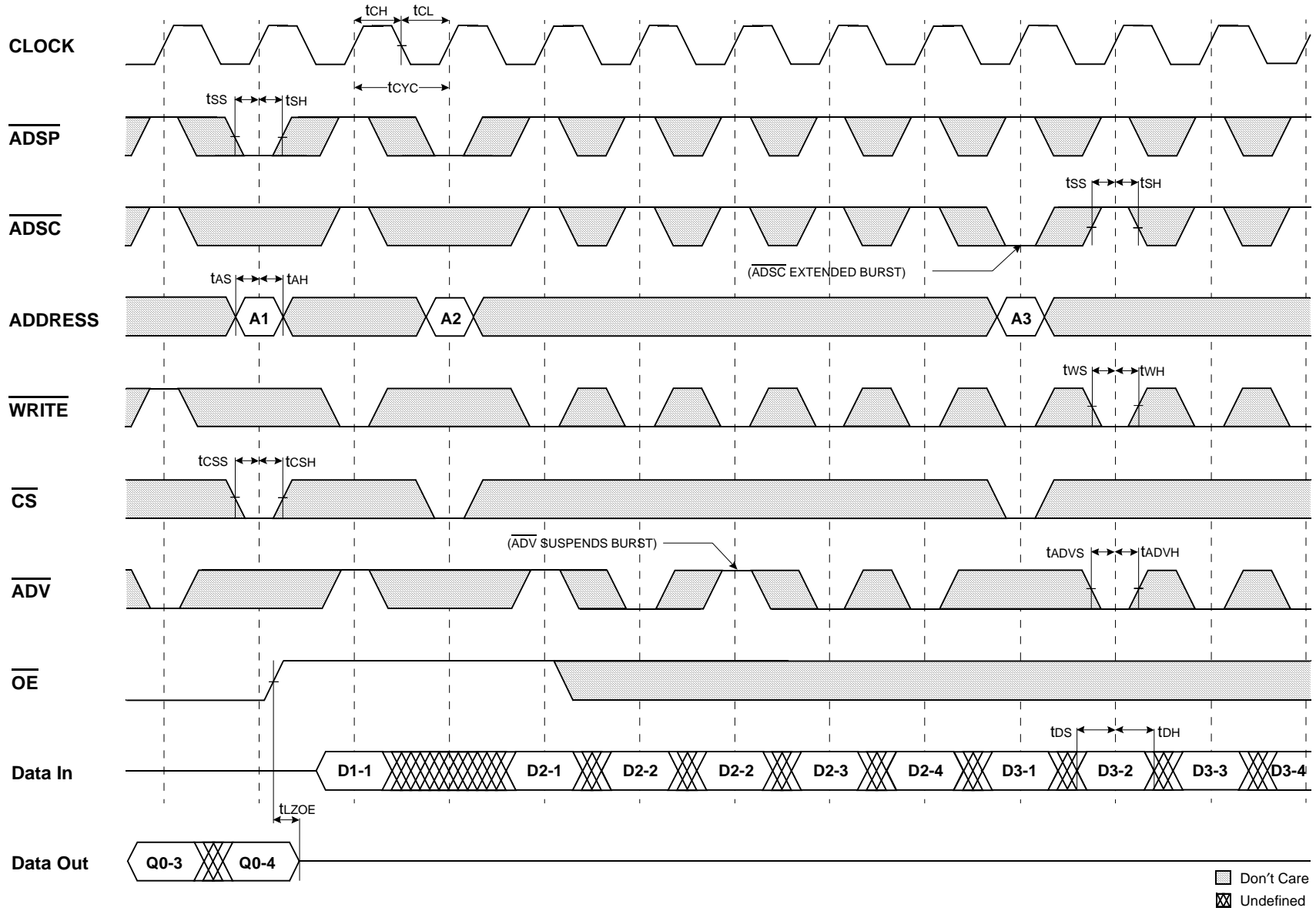
TIMING WAVEFORM OF READ CYCLE



NOTES : $\overline{\text{WRITE}} = \text{L}$ means $\overline{\text{GW}} = \text{L}$, or $\overline{\text{GW}} = \text{H}$, $\overline{\text{BW}} = \text{L}$, $\overline{\text{WEx}} = \text{L}$
 $\overline{\text{CS}} = \text{L}$ means $\overline{\text{CS}}_1 = \text{L}$, $\text{CS}_2 = \text{H}$ and $\overline{\text{CS}}_2 = \text{L}$
 $\overline{\text{CS}} = \text{H}$ means $\overline{\text{CS}}_1 = \text{H}$, or $\overline{\text{CS}}_1 = \text{L}$ and $\text{CS}_2 = \text{H}$, or $\overline{\text{CS}}_1 = \text{L}$, and $\text{CS}_2 = \text{L}$

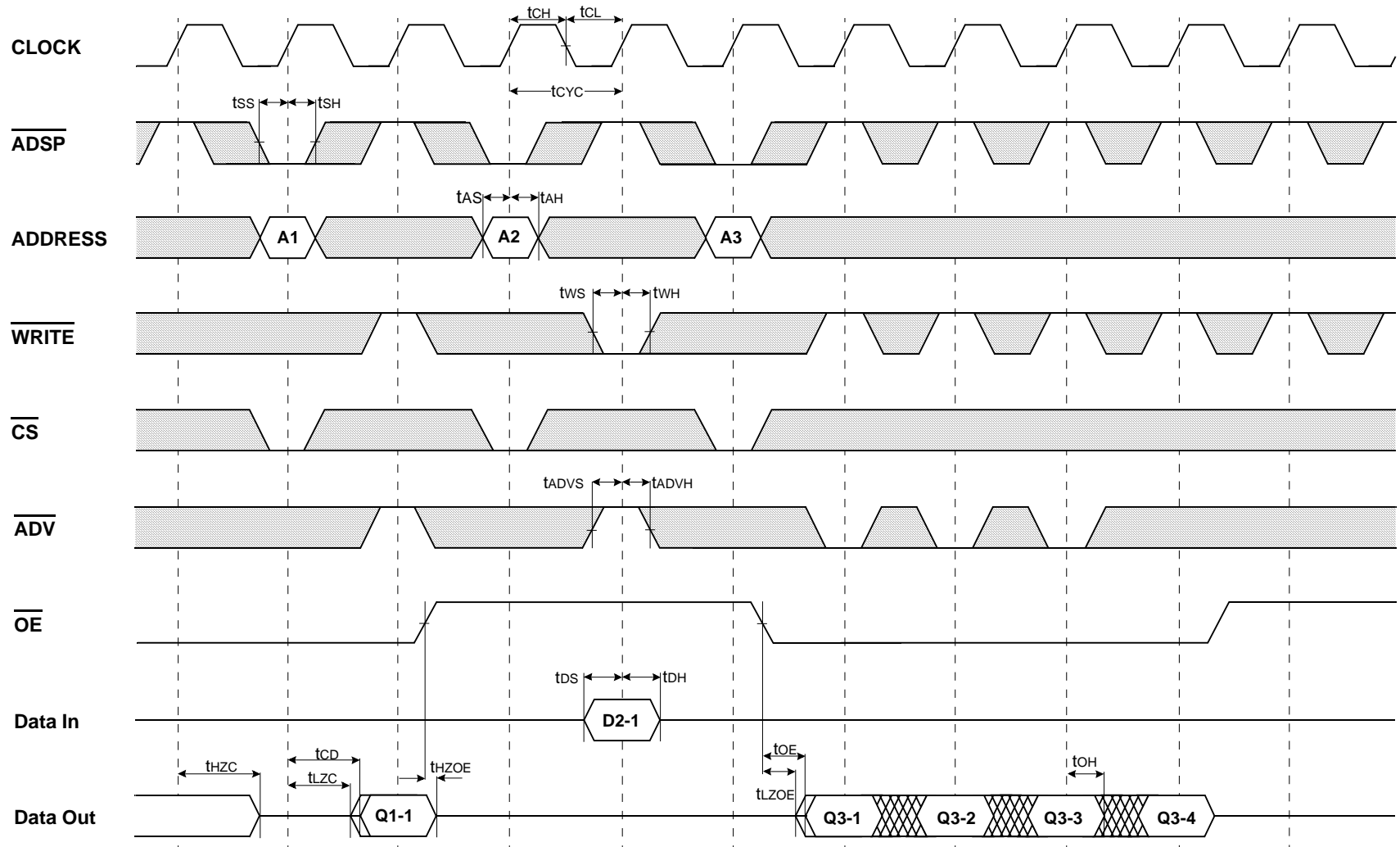
□ Don't Care
 ⊗ Undefined

TIMING WAVEFORM OF WRTE CYCLE



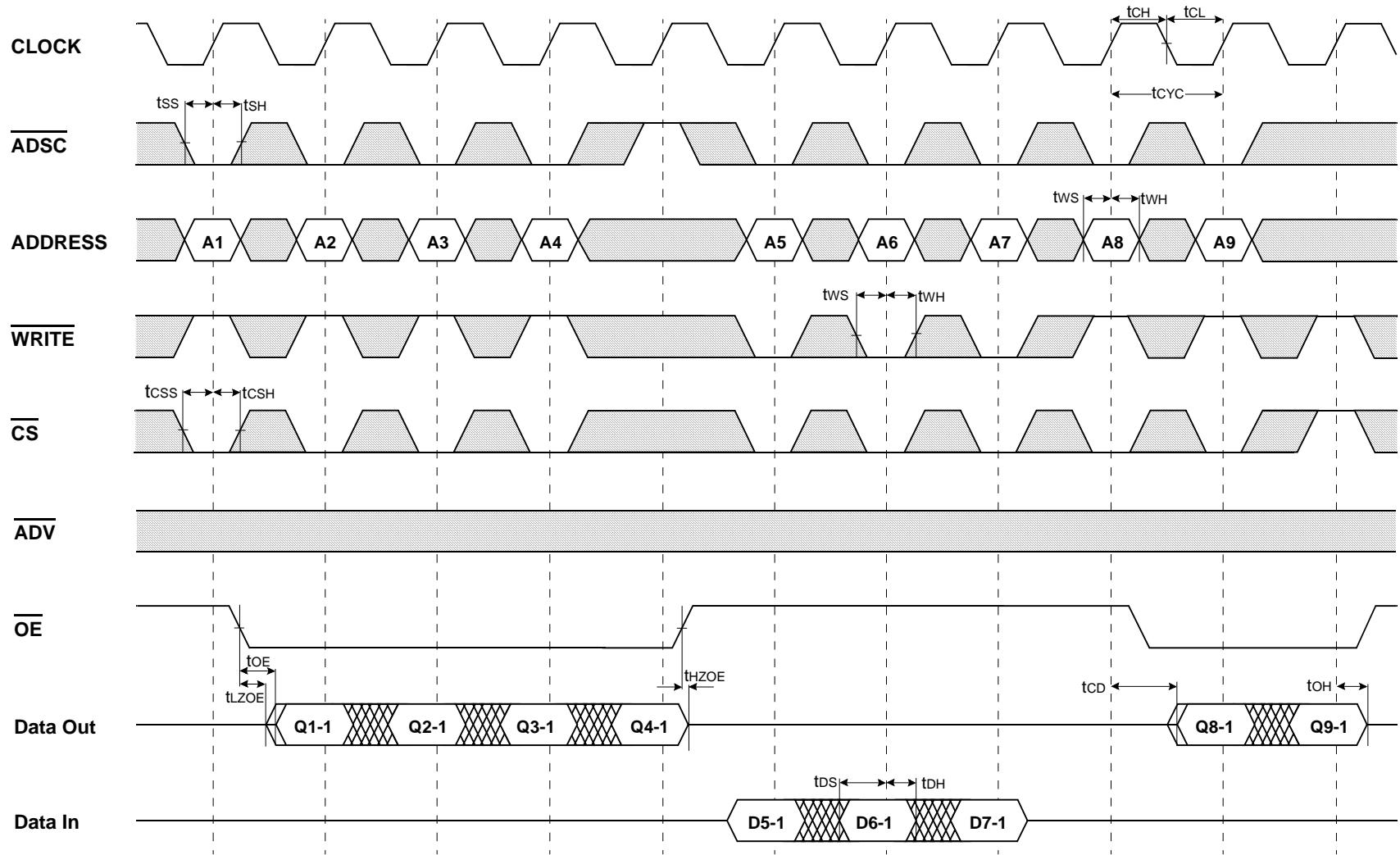
□ Don't Care
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TIMING WAVEFORM OF COMBINATION READ/WRITE CYCLE(ADSP CONTROLLED, $\overline{\text{ADSC}}=\text{HIGH}$)



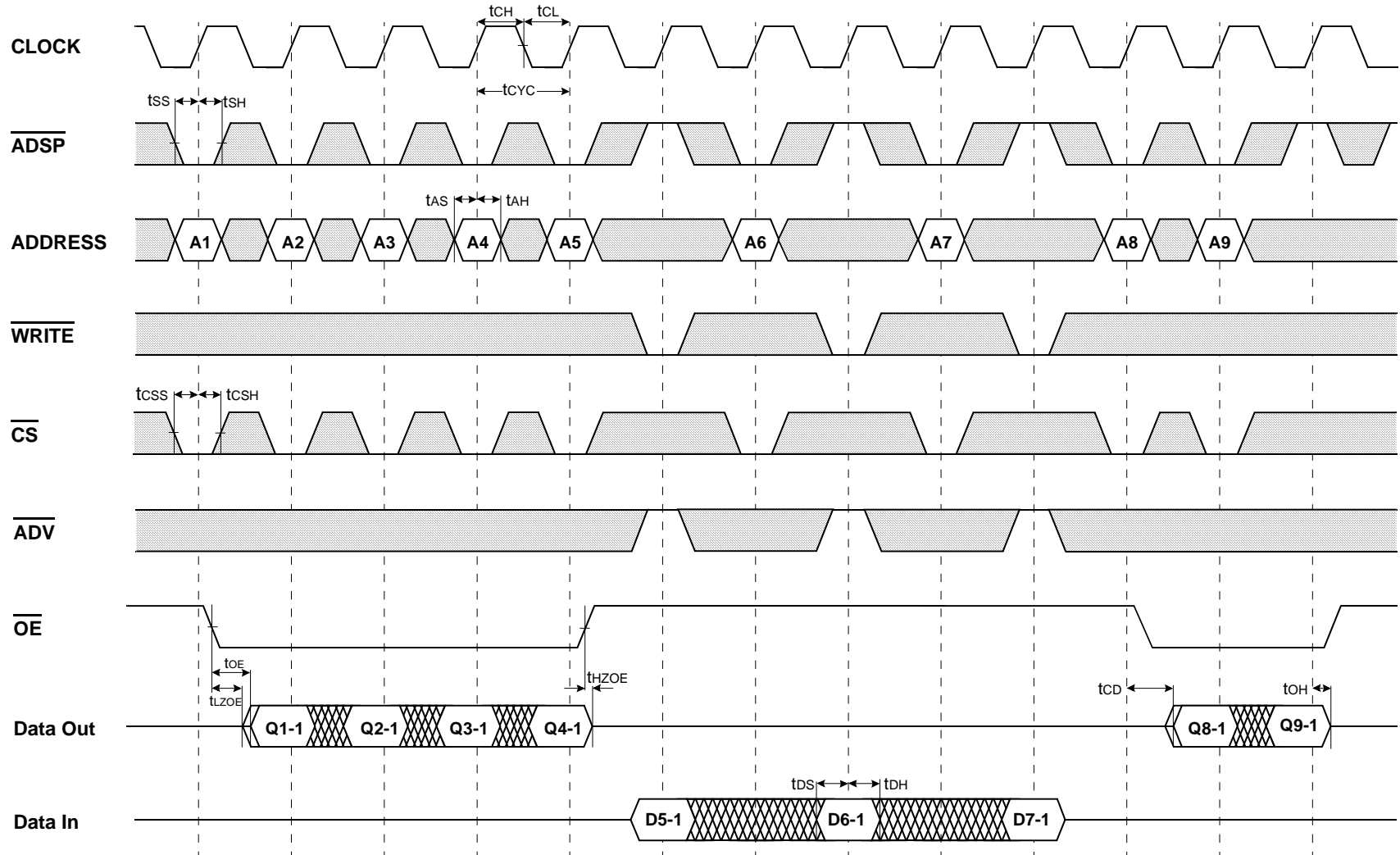
□ Don't Care
 ⊠ Undefined

TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE(ADSC CONTROLLED, $\overline{\text{ADSP}}=\text{HIGH}$)



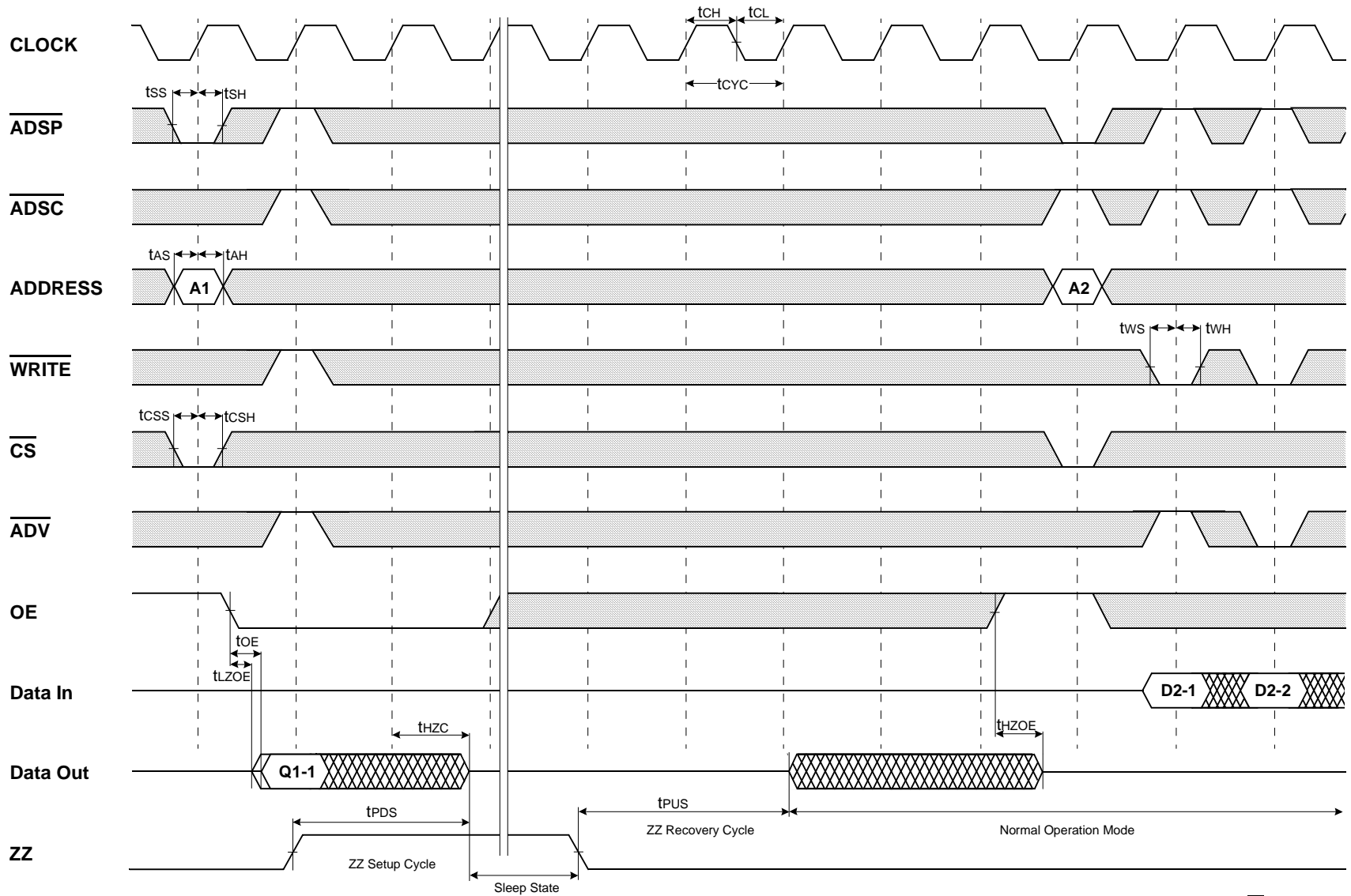
Don't Care
 Undefined

TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE(ADSP CONTROLLED, ADSC=HIGH)



□ Don't Care
 ▨ Undefined

TIMING WAVEFORM OF POWER DOWN CYCLE

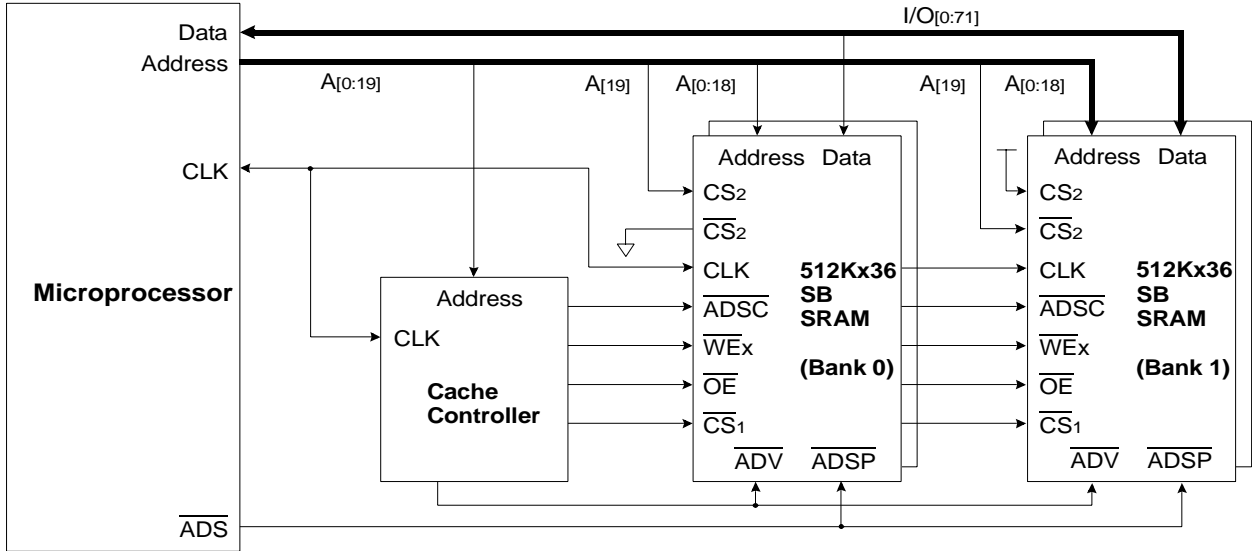


□ Don't Care
 ▨ Undefined

APPLICATION INFORMATION

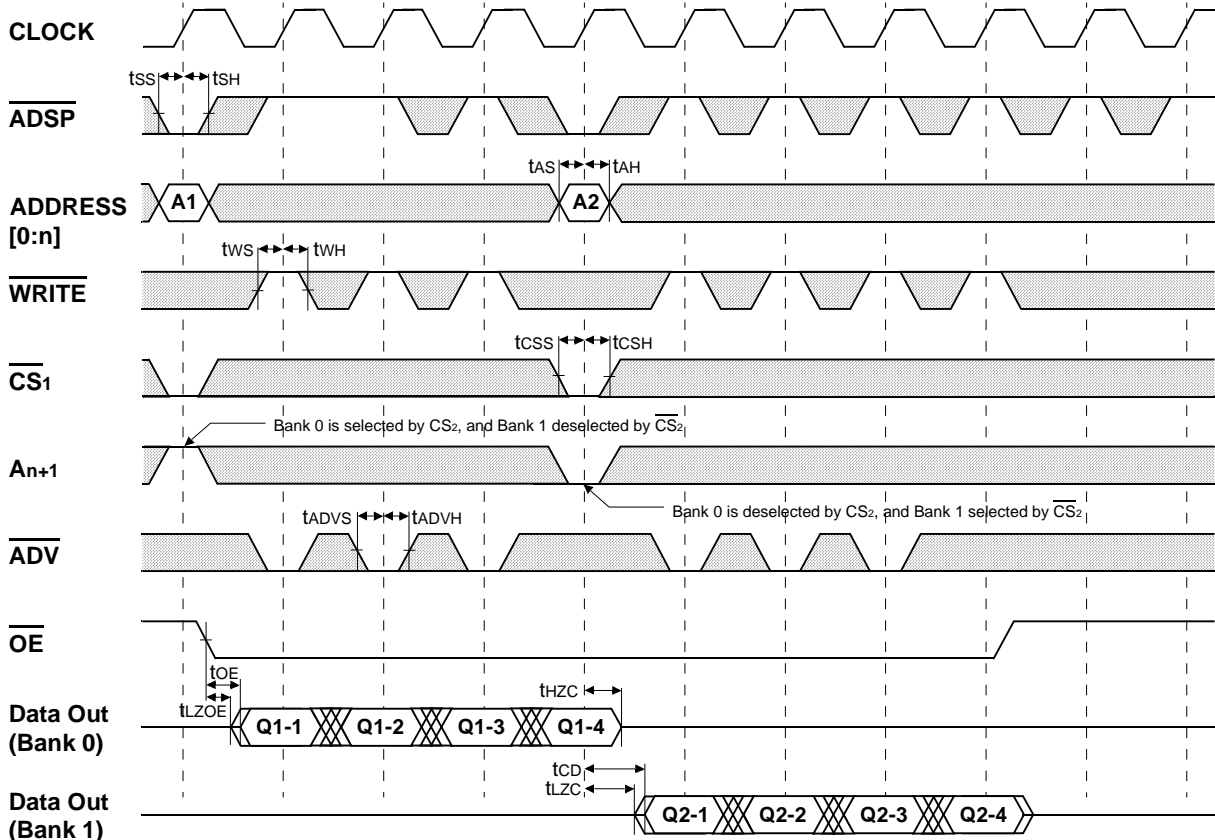
DEPTH EXPANSION

The Samsung 512Kx36 Synchronous Burst SRAM has two additional chip selects for simple depth expansion. This permits easy secondary cache upgrades from 512K depth to 1M depth without extra logic.



INTERLEAVE READ TIMING (Refer to non-interleave write timing for interleave write timing)

(ADSP CONTROLLED , ADSC=HIGH)



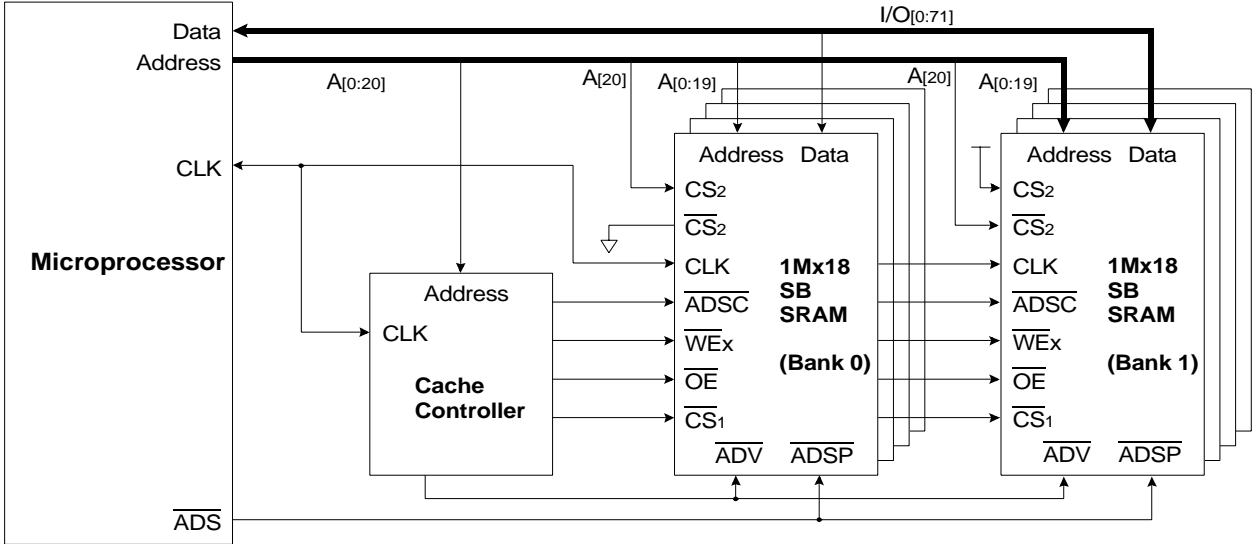
*Notes : n = 14 32K depth , 15 64K depth
16 128K depth , 17 256K depth
18 512K depth , 19 1M depth

□ Don't Care ⊗ Undefined

APPLICATION INFORMATION

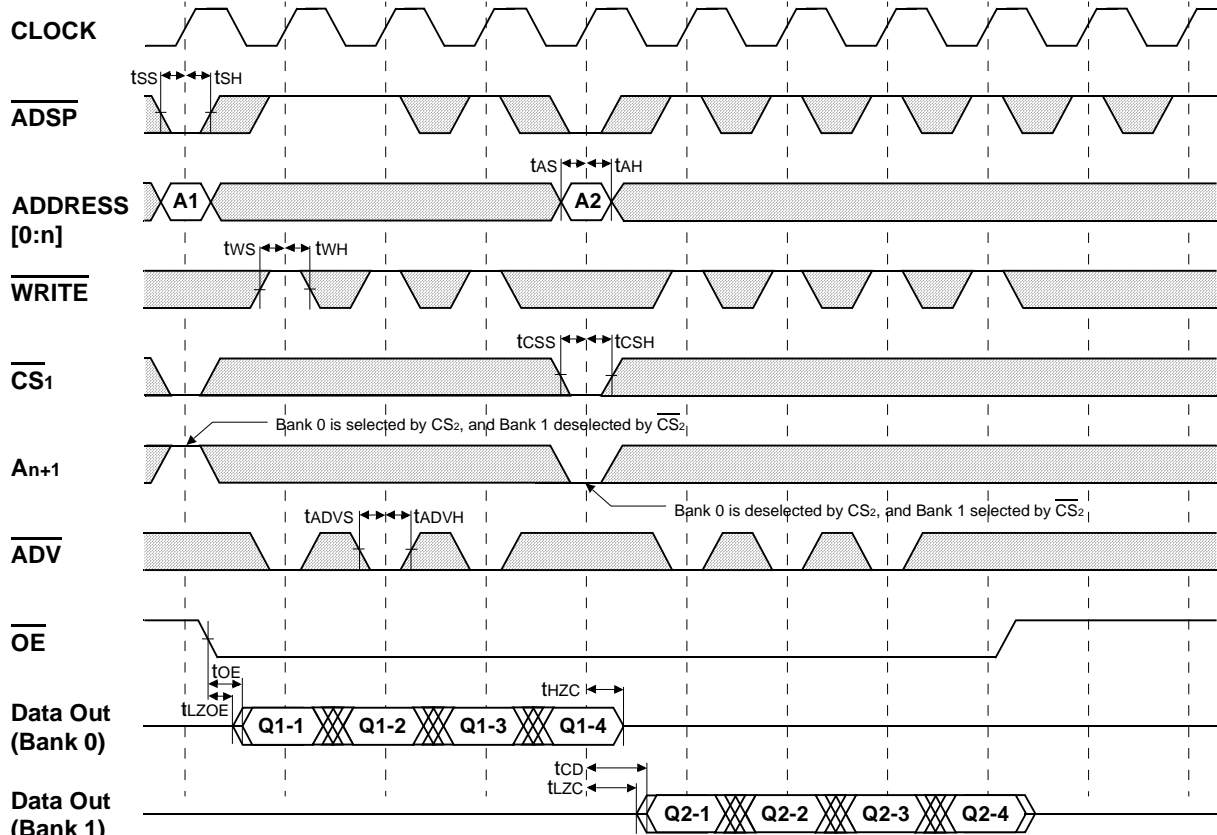
DEPTH EXPANSION

The Samsung 1Mx18 Synchronous Burst SRAM has two additional chip selects for simple depth expansion. This permits easy secondary cache upgrades from 1M depth to 2M depth without extra logic.



INTERLEAVE READ TIMING (Refer to non-interleave write timing for interleave write timing)

(ADSP CONTROLLED, ADSC=HIGH)



*Notes : n = 14 32K depth, 15 64K depth
 16 128K depth, 17 256K depth
 18 512K depth, 19 1M depth
 20 2M depth

□ Don't Care ⊗ Undefined

PACKAGE DIMENSIONS

