

Document Title**Multi-Chip Package MEMORY****64M Bit (4Mx16) U_tRAM / 64M Bit (4Mx16) U_tRAM / 8M Bit (512Kx16) SRAM**Revision History

<u>Revision No.</u>	<u>History</u>	<u>Draft Date</u>	<u>Remark</u>
0.0	Initial draft.	May 12, 2003	Preliminary
0.1	Revised - Changed ball name from Vccqs to Vccs in Pin Configuration.	July 11, 2003	Preliminary
1.0	Finalized <U _t RAM> - Changed tPC from Max 25ns to Min 25ns in the AC Characteristics.	September 22, 2003	Final

Note : For more detailed features and specifications including FAQ, please refer to Samsung's web site.
http://samsungelectronics.com/semiconductors/products/products_index.html

The attached datasheets are prepared and approved by SAMSUNG Electronics. SAMSUNG Electronics CO., LTD. reserve the right to change the specifications. SAMSUNG Electronics will evaluate and reply to your requests and questions about device. If you have any questions, please contact the SAMSUNG branch office near you.

Multi-Chip Package MEMORY**64M Bit (4Mx16) U_tRAM / 64M Bit (4Mx16) U_tRAM / 8M Bit (512Kx16) SRAM****FEATURES**

<Common>

- Operating Temperature : -25°C ~ 85°C
- Package : 111 - ball FBGA Type - 10 x 11mm, 0.8 mm pitch

<U_tRAM(each device)>

- Power Supply Voltage: 2.7~3.1V
- Organization: 4M x16 bit
- Three State Outputs
- Compatible with Low Power SRAM
- Support 4 page mode (Read only)
- Deep Power Down: Memory cell data hold invalid

<SRAM>

- Process Technology: Full CMOS
- Organization: 512K x16
- Power Supply Voltage: 2.7~3.3V
- Low Data Retention Voltage: 1.5V(Min)
- Three State Outputs

GENERAL DESCRIPTION

The KAJ000A30M is a Multi Chip Package Memory which combines two 64Mbit Unit Transistor CMOS RAM and 8Mbit SRAM. 64Mbit U_tRAM is organized as 4M x16 bit and 8Mbit SRAM is organized as 512K x16 bit.

The 64Mbit U_tRAM is fabricated by SAMSUNG's advanced CMOS technology using one transistor memory cell. The device support page mode operation. The device also supports deep power down mode for low standby current.

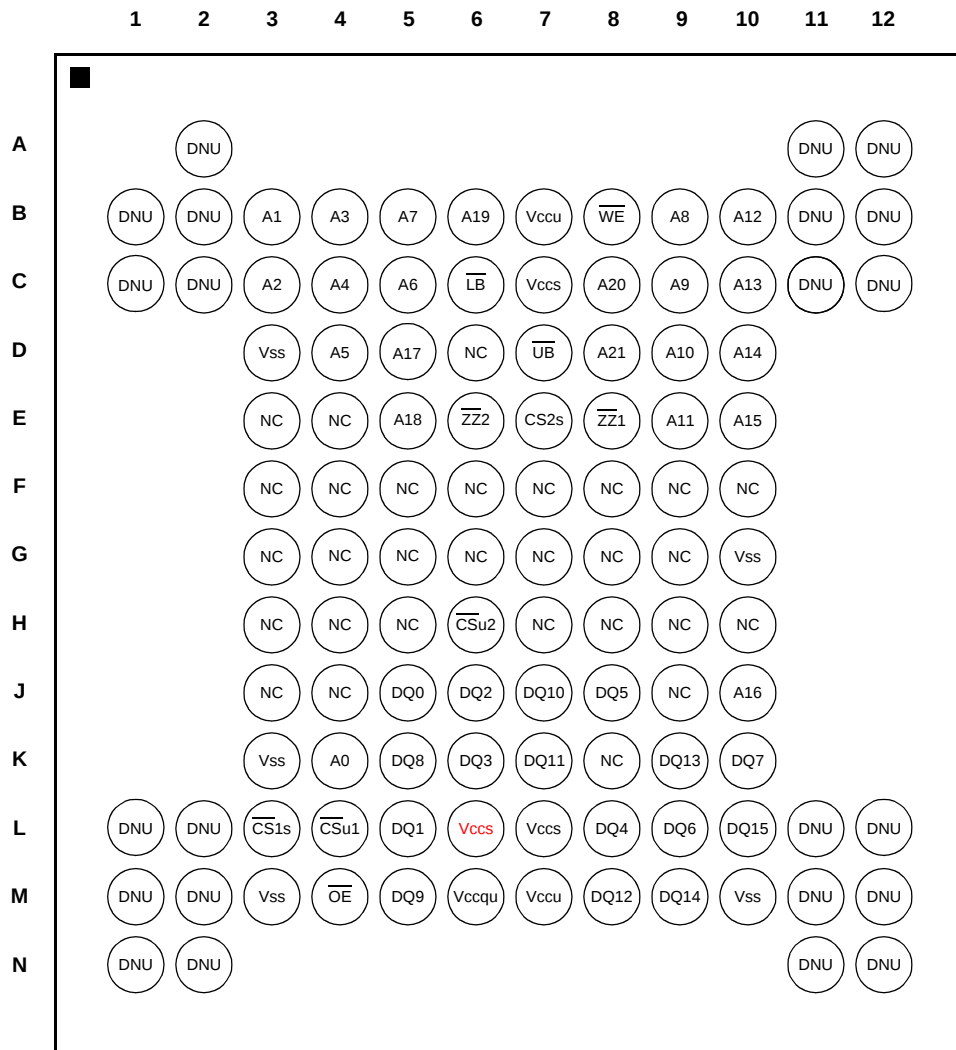
The 8Mbit SRAM is fabricated by SAMSUNG's advanced full CMOS process technology. The device supports low data retention voltage for battery back-up operation with low data retention current.

The KAJ000A30M is suitable for use in data memory of mobile communication system to reduce not only mount area but also power consumption.

This device is available in 111-ball FBGA Type.

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PIN CONFIGURATION



111-FBGA: Top View (Ball Down)

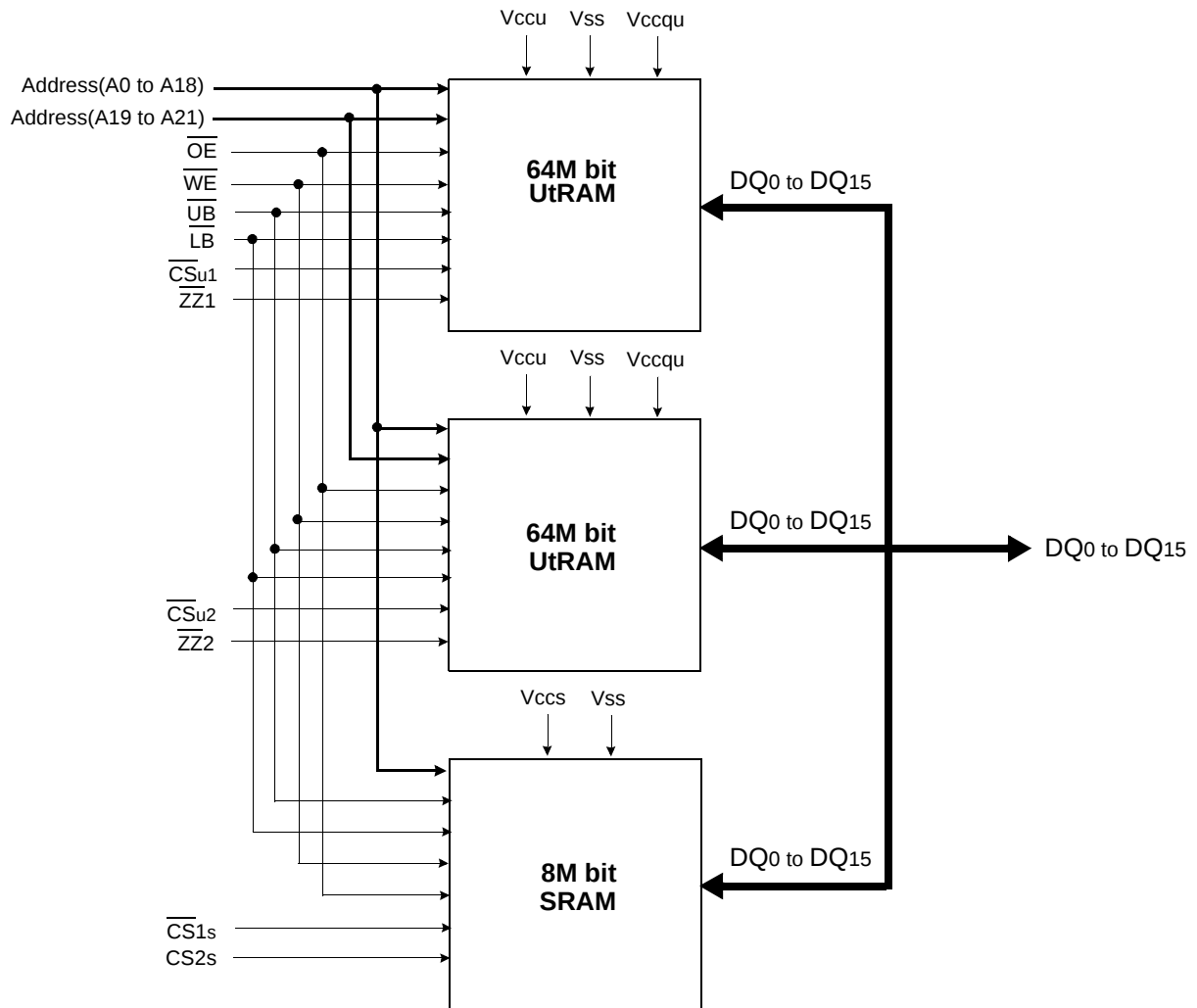
PIN DESCRIPTION

Ball Name	Description	Ball Name	Description
A ₀ to A ₁₈	Address Input Balls (UtRAM,SRAM)	$\overline{\text{ZZ2}}$	Deep Power Down (UtRAM2)
A ₁₉ to A ₂₁	Address Input Balls (UtRAM)	$\overline{\text{CSu1}}$	Chip Select (UtRAM1)
DQ ₀ to DQ ₁₅	Data Input/Output Balls (UtRAM, SRAM)	$\overline{\text{CSu2}}$	Chip Select (UtRAM2)
V _{ccu}	Power Supply (UtRAM)	$\overline{\text{CS1s}}$	Chip Select (SRAM)
V _{ccs}	Power Supply (SRAM)	CS2s	Chip Select (SRAM)
V _{ccqu}	Data Out Power (UtRAM)	$\overline{\text{WE}}$	Write Enable (UtRAM, SRAM)
V _{ss}	Ground (Common)	$\overline{\text{OE}}$	Output Enable (UtRAM, SRAM)
$\overline{\text{UB}}$	Upper Byte Enable (UtRAM, SRAM)	NC	No Connection
$\overline{\text{LB}}$	Lower Byte Enable (UtRAM, SRAM)	DNU	Do Not Use
$\overline{\text{ZZ1}}$	Deep Power Down (UtRAM1)		

ORDERING INFORMATION

K A J 00 0 A 3 0 M - F L L L													
Samsung MCP(3 Chip) Memory				Access Time L : UtRAM : 70ns L : UtRAM : 70ns L : SRAM : 70ns									
Device Type UtRAM+UtRAM+SRAM				Package F : FBGA									
NOR Flash Density , Vcc , Org. 00 : NONE				Version M : 1st Generation									
NAND Flash Density , Vcc , Org. 0 : NONE				SDRAM Density , Vcc , Org. 0 : NONE									
UtRAM Density , Vcc , Org. A : 64Mbit + 64Mbit, 3.0V, x16(Page)				SRAM Density , Vcc , Org. 3 : 8Mbit, 3.0V, x16									

Figure 1. FUNCTIONAL BLOCK DIAGRAM



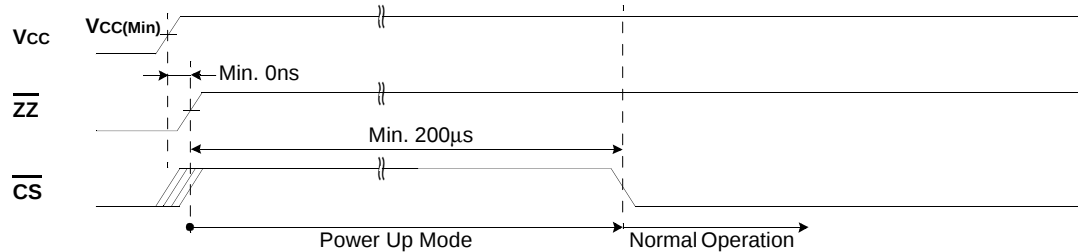
64M Bit(4Mx16) Page Mode UtRAM

For Each Device

POWER UP SEQUENCE

1. Apply power.
2. Maintain stable power($V_{CC \text{ min.}}=2.7V$) for a minimum 200 μs with $\overline{CS}$ and $\overline{ZZ}$ high.

TIMING WAVEFORM OF POWER UP



(POWER UP)

1. After V_{CC} reaches $V_{CC(Min.)}$, wait 200 μs with $\overline{CS}$ and $\overline{ZZ}$ high. Then you get into the normal operation.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{ZZ}$	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	DQ ₀₋₇	DQ ₈₋₁₅	Mode	Power
H	H	X ¹⁾	X ¹⁾	X ¹⁾	X ¹⁾	High-Z	High-Z	Deselected	Standby
X ¹⁾	L	X ¹⁾	X ¹⁾	X ¹⁾	X ¹⁾	High-Z	High-Z	Deselected	Deep Power Down
L	H	X ¹⁾	X ¹⁾	H	H	High-Z	High-Z	Deselected	Standby
L	H	H	H	L	X ¹⁾	High-Z	High-Z	Output Disabled	Active
L	H	H	H	X ¹⁾	L	High-Z	High-Z	Output Disabled	Active
L	H	L	H	L	H	Dout	High-Z	Lower Byte Read	Active
L	H	L	H	H	L	High-Z	Dout	Upper Byte Read	Active
L	H	L	H	L	L	Dout	Dout	Word Read	Active
L	H	X ¹⁾	L	L	H	Din	High-Z	Lower Byte Write	Active
L	H	X ¹⁾	L	H	L	High-Z	Din	Upper Byte Write	Active
L	H	X ¹⁾	L	L	L	Din	Din	Word Write	Active

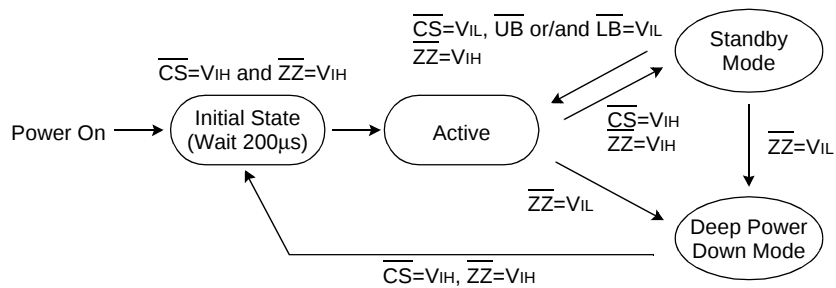
1. X means don't care.(Must be low or high state)

ABSOLUTE MAXIMUM RATINGS¹⁾

Item	Symbol	Ratings	Unit
Voltage on any pin relative to V _{SS}	V _{IN} , V _{OUT}	-0.2 to V _{CC} +0.3V	V
Voltage on V _{CC} supply relative to V _{SS}	V _{CC}	-0.2 to 3.6V	V
Power Dissipation	P _D	1.0	W
Storage temperature	T _{STG}	-65 to 150	°C
Operating Temperature	T _A	-25 to 85	°C

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to be used under recommended operating condition. Exposure to absolute maximum rating conditions longer than 1 second may affect reliability.

STANDBY MODE STATE MACHINES



STANDBY MODE CHARACTERISTIC

Power Mode	Memory Cell Data	Standby Current(µA)	Wait Time(µs)
Standby	Valid	120	0
Deep Power Down	Invalid	20	200

RECOMMENDED DC OPERATING CONDITIONS¹⁾

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V _{CC}	2.7	2.9	3.1	V
Ground	V _{SS}	0	0	0	V
Input high voltage	V _{IH}	2.2	-	V _{CC} +0.2 ²⁾	V
Input low voltage	V _{IL}	-0.2 ³⁾	-	0.6	V

1. T_A=-25 to 85°C, otherwise specified.

2. Overshoot: V_{CC}+1.0V in case of pulse width ≤20ns.

3. Undershoot: -1.0V in case of pulse width ≤20ns.

4. Overshoot and undershoot are sampled, not 100% tested.

CAPACITANCE¹⁾(f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C _{IN}	V _{IN} =0V	-	8	pF
Input/Output capacitance	C _{IO}	V _{IO} =0V	-	10	pF

1. Capacitance is sampled, not 100% tested.

DC AND OPERATING CHARACTERISTICS

Item	Symbol	Test Conditions	Min	Typ ¹⁾	Max	Unit
Input leakage current	I _{LI}	V _{IN} =V _{SS} to V _{CC}	-1	-	1	μA
Output leakage current	I _{LO}	$\overline{CS}=V_{IH}$, $\overline{ZZ}=V_{IH}$, $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$, V _{IO} =V _{SS} to V _{CC}	-1	-	1	μA
Average operating current	I _{CC1}	Cycle time=1μs, 100% duty, I _{IO} =0mA, $\overline{CS} \leq 0.2V$, $\overline{ZZ} \geq V_{CC}-0.2V$, V _{IN} ≤0.2V or V _{IN} ≥V _{CC} -0.2V	-	-	15	mA
	I _{CC2}	Cycle time=t _{RC} +3t _{PC} , I _{IO} =0mA, 100% duty, $\overline{CS}=V_{IL}$, $\overline{ZZ}=V_{IH}$, V _{IN} =V _{IL} or V _{IH}	-	-	45	mA
Output low voltage	V _{OL}	I _{OL} =2.1mA	-	-	0.4	V
Output high voltage	V _{OH}	I _{OH} =-1.0mA	2.4	-	-	V
Standby Current(CMOS)	I _{SB1}	$\overline{CS} \geq V_{CC}-0.2V$, $\overline{ZZ} \geq V_{CC}-0.2V$, Other inputs=V _{SS} to V _{CC}	-	-	120	μA
Deep Power Down	I _{SD}	$\overline{ZZ} \leq 0.2V$, Other inputs=V _{SS} to V _{CC}	-	-	20	μA

1. Typical values are tested at V_{CC}=2.9V, T_A=25°C and not guaranteed.

AC OPERATING CONDITIONS**TEST CONDITIONS**(Test Load and Test Input/Output Reference)

Input pulse level: 0.4 to 2.2V

Input rising and falling time: 5ns

Input and output reference voltage: 1.5V

Output load: $C_L=50\text{pF}$ **AC CHARACTERISTICS**($V_{CC}=2.7\sim 3.1\text{V}$, $T_A=-25$ to 85°C)

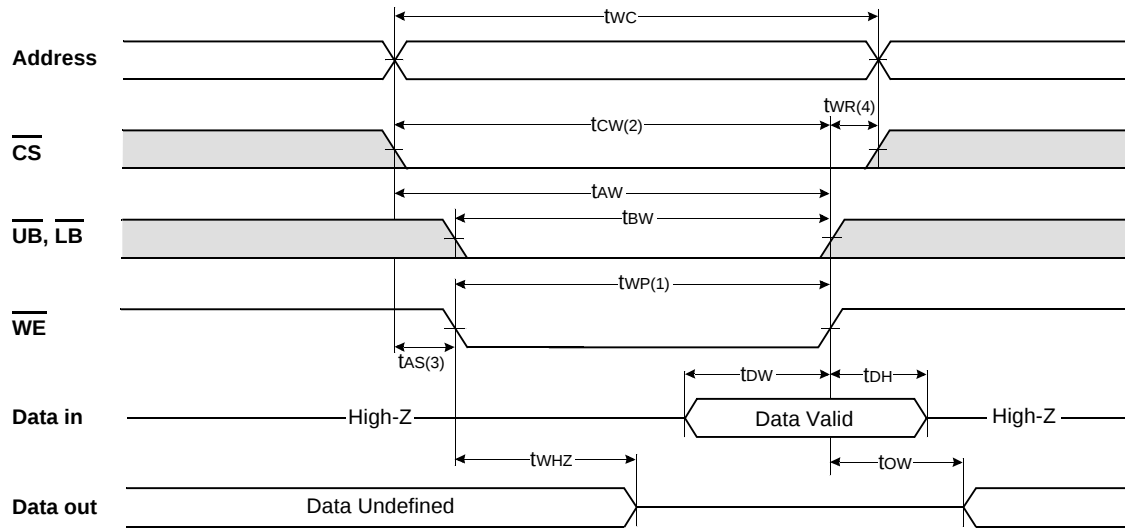
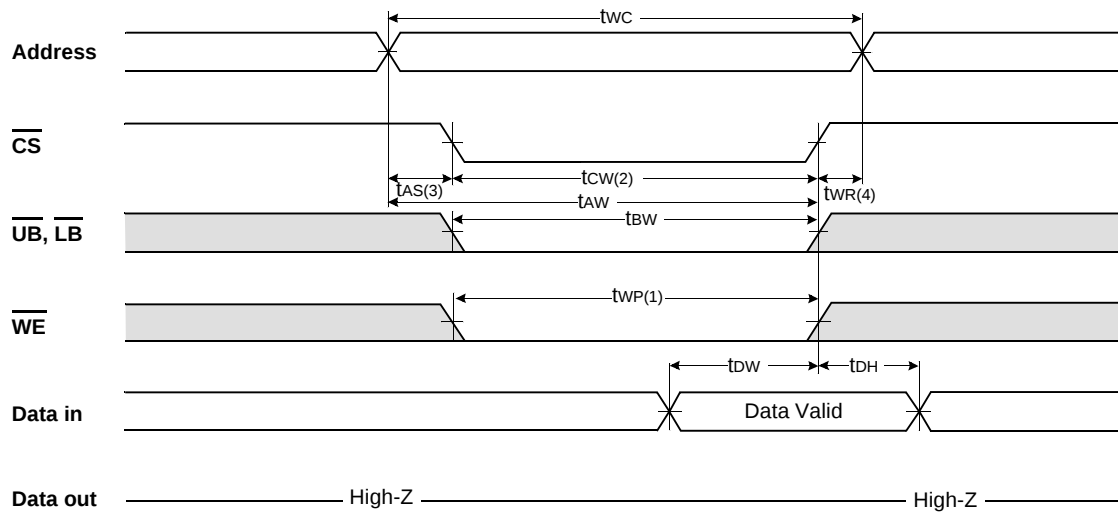
Parameter List		Symbol	Speed Bins		Units
			70ns		
			Min	Max	
Read	Read Cycle Time	t _{RC}	70	-	ns
	Address Access Time	t _{AA}	-	70	ns
	Chip Select to Output	t _{CO}	-	70	ns
	Output Enable to Valid Output	t _{OE}	-	35	ns
	$\overline{\text{UB}}$, $\overline{\text{LB}}$ Access Time	t _{BA}	-	70	ns
	Chip Select to Low-Z Output	t _{LZ}	10	-	ns
	$\overline{\text{UB}}$, $\overline{\text{LB}}$ Enable to Low-Z Output	t _{BLZ}	10	-	ns
	Output Enable to Low-Z Output	t _{OLZ}	5	-	ns
	Chip Disable to High-Z Output	t _{HZ}	0	25	ns
	$\overline{\text{UB}}$, $\overline{\text{LB}}$ Disable to High-Z Output	t _{BHZ}	0	25	ns
	Output Disable to High-Z Output	t _{OHZ}	0	25	ns
	Output Hold from Address Change	t _{OH}	5	-	ns
	Page Cycle	t _{PC}	25	-	ns
	Page Access Time	t _{PA}	-	20	ns
Write	Write Cycle Time	t _{WC}	70	-	ns
	Chip Select to End of Write	t _{CW}	60	-	ns
	Address Set-up Time	t _{AS}	0	-	ns
	Address Valid to End of Write	t _{AW}	60	-	ns
	$\overline{\text{UB}}$, $\overline{\text{LB}}$ Valid to End of Write	t _{BW}	60	-	ns
	Write Pulse Width	t _{WP}	55 ¹⁾	-	ns
	Write Recovery Time	t _{WR}	0	-	ns
	Write to Output High-Z	t _{WHZ}	0	25	ns
	Data to Write Time Overlap	t _{DW}	30	-	ns
	Data Hold from Write Time	t _{DH}	0	-	ns
	End Write to Output Low-Z	t _{OW}	5	-	ns

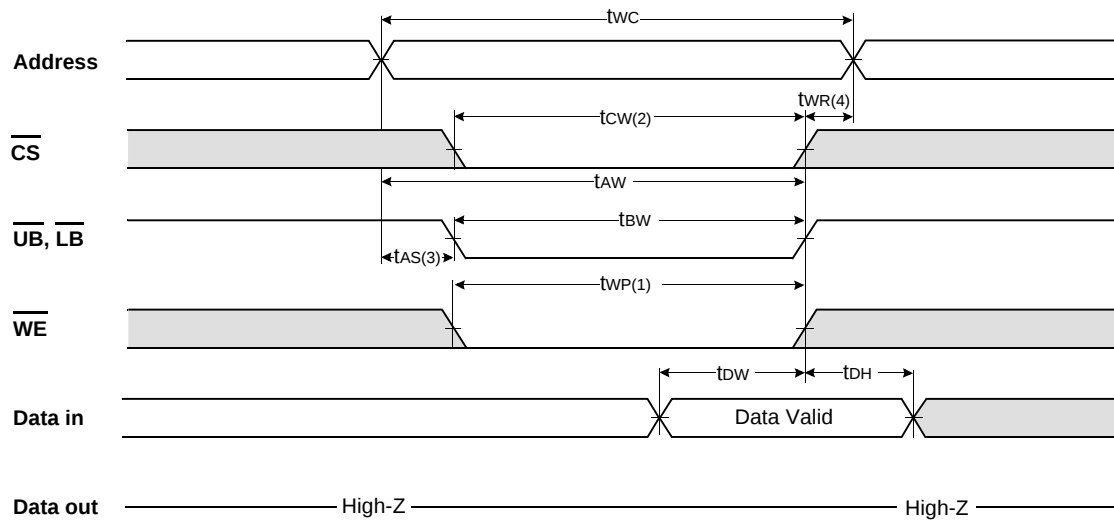
1. t_{WP}(min)=70ns for continuous write operation over 50 times.

TIMING WAVEFORM OF READ CYCLE(1)(Address Controlled, $\overline{\text{CS}}=\overline{\text{OE}}=V_{\text{IL}}$, $\overline{\text{ZZ}}=\overline{\text{WE}}=V_{\text{IH}}$, $\overline{\text{UB}}$ or/and $\overline{\text{LB}}=V_{\text{IL}}$)



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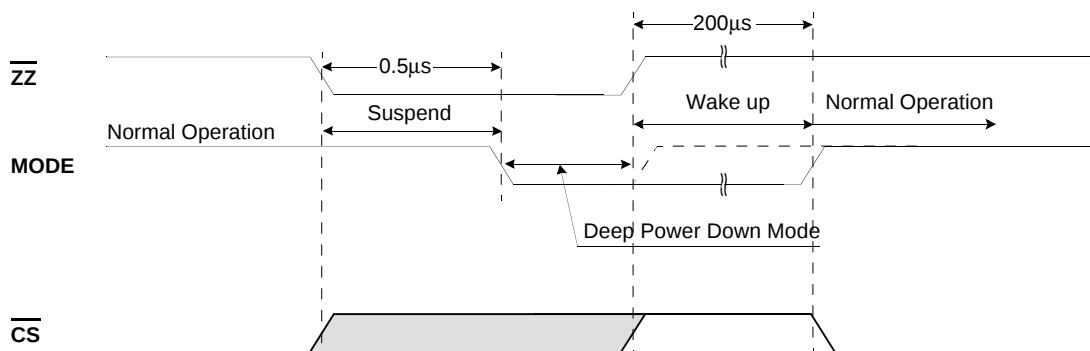
TIMING WAVEFORM OF WRITE CYCLE(1)($\overline{WE}$ Controlled, $\overline{ZZ}=V_{IH}$)TIMING WAVEFORM OF WRITE CYCLE(2)($\overline{CS}$ Controlled, $\overline{ZZ}=V_{IH}$)

TIMING WAVEFORM OF WRITE CYCLE(3)($\overline{UB}$, $\overline{LB}$ Controlled, $\overline{ZZ}=V_{IH}$)

(WRITE CYCLE)

1. A write occurs during the overlap(t_{WP}) of low $\overline{CS}$ and low $\overline{WE}$. A write begins when $\overline{CS}$ goes low and $\overline{WE}$ goes low with asserting $\overline{UB}$ or $\overline{LB}$ for single byte operation or simultaneously asserting $\overline{UB}$ and $\overline{LB}$ for double byte operation. A write ends at the earliest transition when $\overline{CS}$ goes high and $\overline{WE}$ goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the $\overline{CS}$ going low to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} is applied in case a write ends with $\overline{CS}$ or $\overline{WE}$ going high.

TIMING WAVEFORM OF DEEP POWER DOWN MODE ENTRY AND EXIT



(DEEP POWER DOWN MODE)

1. When you toggle $\overline{ZZ}$ pin low, the device gets into the Deep Power Down mode after 0.5μs suspend period.
2. To return to normal operation, the device needs Wake Up period.
3. Wake Up sequence is just the same as Power Up sequence.

8M Bit(512Kx16) SRAM

FUNCTIONAL DESCRIPTION

$\overline{CS}_1$	CS_2	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	DQ ₀₋₇	DQ ₈₋₁₅	Mode	Power
H	X ¹⁾	X ¹⁾	X ¹⁾	X ¹⁾	X ¹⁾	High-Z	High-Z	Deselected	Standby
X ¹⁾	L	X ¹⁾	X ¹⁾	X ¹⁾	X ¹⁾	High-Z	High-Z	Deselected	Standby
X ¹⁾	X ¹⁾	X ¹⁾	X ¹⁾	H	H	High-Z	High-Z	Deselected	Standby
L	H	H	H	L	X ¹⁾	High-Z	High-Z	Output Disabled	Active
L	H	H	H	X ¹⁾	L	High-Z	High-Z	Output Disabled	Active
L	H	L	H	L	H	Dout	High-Z	Lower Byte Read	Active
L	H	L	H	H	L	High-Z	Dout	Upper Byte Read	Active
L	H	L	H	L	L	Dout	Dout	Word Read	Active
L	H	X ¹⁾	L	L	H	Din	High-Z	Lower Byte Write	Active
L	H	X ¹⁾	L	H	L	High-Z	Din	Upper Byte Write	Active
L	H	X ¹⁾	L	L	L	Din	Din	Word Write	Active

1. X means don't care. (Must be low or high state)

ABSOLUTE MAXIMUM RATINGS¹⁾

Item	Symbol	Ratings	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-0.2 to V _{CC} +0.3V(Max. 3.6V)	V
Voltage on Vcc supply relative to Vss	V _{CC}	-0.2 to 3.6	V
Power Dissipation	P _d	1.0	W
Storage temperature	T _{STG}	-65 to 150	°C
Operating Temperature	T _A	-25 to 85	°C

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to be used under recommended operating condition. Exposure to absolute maximum rating conditions over 1 second may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS¹⁾

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V _{CC}	2.7	3.0	3.3	V
Ground	V _{SS}	0	0	0	V
Input high voltage	V _{IH}	2.2	-	V _{CC} +0.2 ²⁾	V
Input low voltage	V _{IL}	-0.2 ³⁾	-	0.6	V

Note:

1. T_A=-25 to 85°C, otherwise specified.2. Overshoot: V_{CC}+2.0V in case of pulse width ≤20ns.

3. Undershoot: -2.0V in case of pulse width ≤20ns.

4. Overshoot and undershoot are sampled, not 100% tested.

CAPACITANCE¹⁾ (f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C _{IN}	V _{IN} =0V	-	8	pF
Input/Output capacitance	C _{IO}	V _{IO} =0V	-	10	pF

1. Capacitance is sampled, not 100% tested.

DC AND OPERATING CHARACTERISTIC

Item	Symbol	Test Conditions	Min	Typ ¹⁾	Max	Unit
Input leakage current	I _{LI}	V _{IN} =V _{SS} to V _{CC}	-1	-	1	μA
Output leakage current	I _{LO}	$\overline{CS1}=V_{IH}$ or CS2=V _{IL} or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$ or LB=UB=V _{IH} , V _{IO} =V _{SS} to V _{CC}	-1	-	1	μA
Average operating current	I _{CC1}	Cycle time=1μs, 100%duty, I _{IO} =0mA, $\overline{CS1} \leq 0.2V$, LB≤0.2V or/and UB≤0.2V, CS2≥V _{CC} -0.2V, V _{IN} ≤0.2V or V _{IN} ≥V _{CC} -0.2V	-	-	5	mA
	I _{CC2}	Cycle time=Min, I _{IO} =0mA, 100% duty, $\overline{CS1}=V_{IL}$, CS2=V _{IH} , LB=V _{IL} or/and UB=V _{IL} , V _{IN} =V _{IL} or V _{IH}	70ns	-	30	mA
Output low voltage	V _{OL}	I _{OL} = 2.1mA	-	-	0.4	V
Output high voltage	V _{OH}	I _{OH} = -1.0mA	2.4	-	-	V
Standby Current(CMOS)	I _{SB1}	Other input =0~V _{CC} 1) $\overline{CS1} \geq V_{CC}-0.2V$, CS2≥V _{CC} -0.2V($\overline{CS1}$ controlled) or 2) 0V≤CS2≤0.2V(CS2 controlled)	-	-	25	μA

1. Typical values are measured at V_{CC}=3.0V, T_A=25°C and not 100% tested.

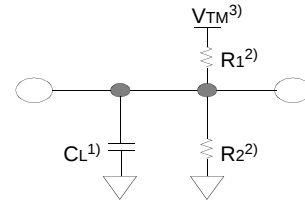
AC OPERATING CONDITIONS

TEST CONDITIONS (Test Load and Input/Output Reference)

Input pulse level: 0.4 to 2.2V

Input rising and falling time: 5ns

Input and output reference voltage: 1.5V

Output load (see right): $C_L=100\text{pF}+1\text{TTL}$ 

1. Including scope and jig capacitance
2. $R_1=3070\Omega$, $R_2=3150\Omega$
3. $V_{TM}=2.8\text{V}$

AC CHARACTERISTICS ($V_{CC}=2.7\sim 3.3\text{V}$, Industrial product: $T_A=-25$ to 85°C)

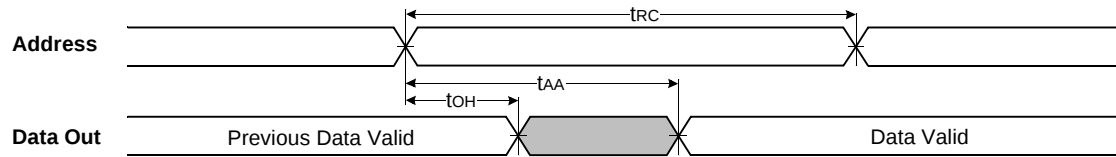
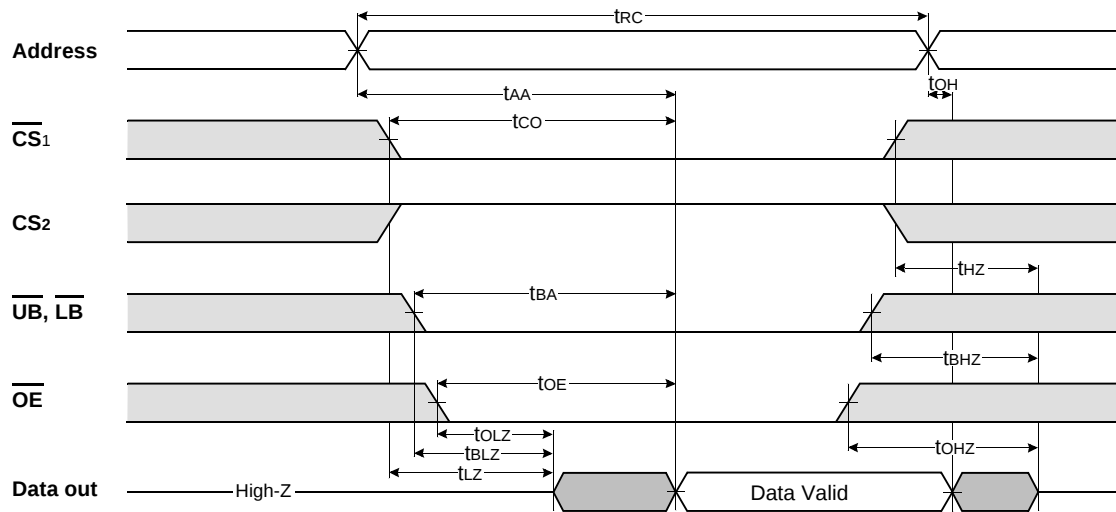
Parameter List		Symbol	Speed Bins		Units
			70ns		
			Min	Max	
Read	Read Cycle Time	t _{RC}	70	-	ns
	Address Access Time	t _{AA}	-	70	ns
	Chip Select to Output	t _{CO}	-	70	ns
	Output Enable to Valid Output	t _{OE}	-	35	ns
	$\overline{\text{UB}}$, $\overline{\text{LB}}$ Access Time	t _{BA}	-	70	ns
	Chip Select to Low-Z Output	t _{LZ}	10	-	ns
	$\overline{\text{UB}}$, $\overline{\text{LB}}$ Enable to Low-Z Output	t _{BLZ}	10	-	ns
	Output Enable to Low-Z Output	t _{OLZ}	5	-	ns
	Chip Disable to High-Z Output	t _{HZ}	0	25	ns
	$\overline{\text{UB}}$, $\overline{\text{LB}}$ Disable to High-Z Output	t _{BHZ}	0	25	ns
	Output Disable to High-Z Output	t _{OHZ}	0	25	ns
	Output Hold from Address Change	t _{OH}	10	-	ns
Write	Write Cycle Time	t _{WC}	70	-	ns
	Chip Select to End of Write	t _{CW}	60	-	ns
	Address Set-up Time	t _{AS}	0	-	ns
	Address Valid to End of Write	t _{AW}	60	-	ns
	$\overline{\text{UB}}$, $\overline{\text{LB}}$ Valid to End of Write	t _{BW}	60	-	ns
	Write Pulse Width	t _{WP}	50	-	ns
	Write Recovery Time	t _{WR}	0	-	ns
	Write to Output High-Z	t _{WHZ}	0	20	ns
	Data to Write Time Overlap	t _{DW}	30	-	ns
	Data Hold from Write Time	t _{DH}	0	-	ns
	End Write to Output Low-Z	t _{OW}	5	-	ns

DATA RETENTION CHARACTERISTICS

Item	Symbol	Test Condition	Min	Typ ²⁾	Max	Unit
V _{CC} for data retention	V _{DR}	$\overline{\text{CS}}_1 \geq V_{CC}-0.2\text{V}^{1)}$	1.5	-	3.3	V
Data retention current	I _{DR}	$V_{CC}=1.5\text{V}$, $\overline{\text{CS}}_1 \geq V_{CC}-0.2\text{V}^{1)}$	-	-	15	μA
Data retention set-up time	t _{SDR}	See data retention waveform	0	-	-	ns
Recovery time	t _{RDR}		t _{RC}	-	-	

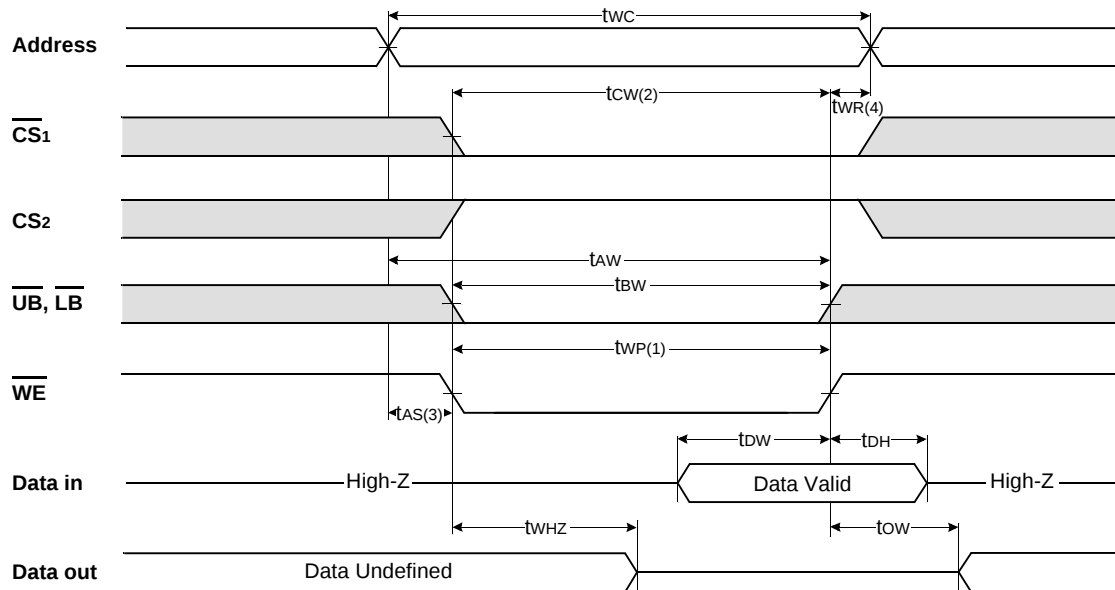
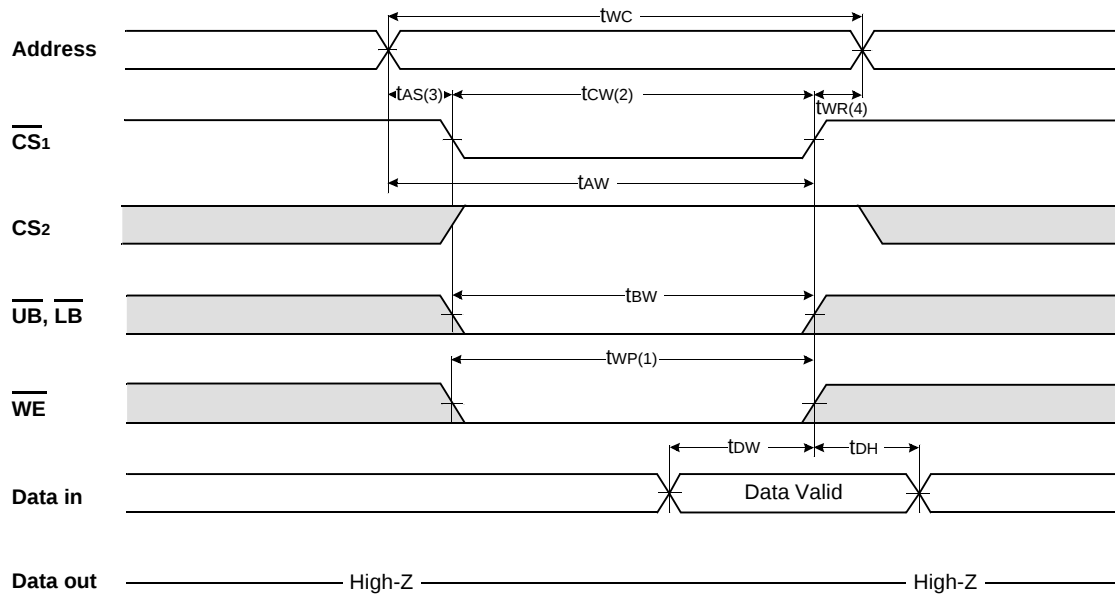
1. 1) $\overline{\text{CS}}_1 \geq V_{CC}-0.2\text{V}$, $\text{CS}_2 \geq V_{CC}-0.2\text{V}$ ($\overline{\text{CS}}_1$ controlled) or2) $0 \leq \text{CS}_2 \leq 0.2\text{V}$ (CS_2 controlled)2. Typical values are measured at $T_A=25^\circ\text{C}$ and not 100% tested.

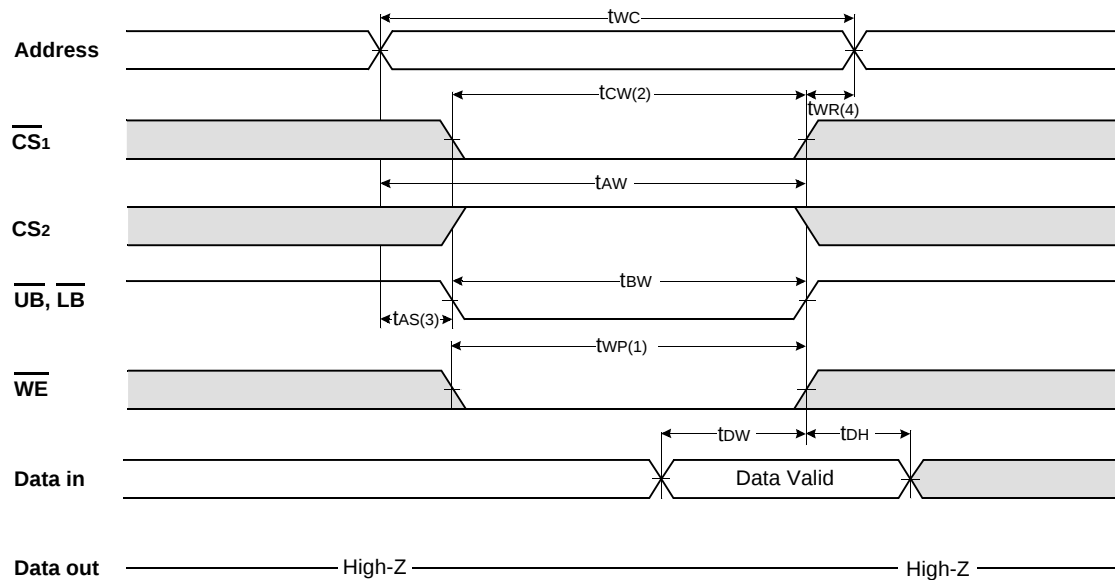
TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS1}=\overline{OE}=V_{IL}$, $CS2=\overline{WE}=V_{IH}$, $\overline{UB}$ or/and $\overline{LB}=V_{IL}$)TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}=V_{IH}$)

NOTES (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, $t_{HZ}(\text{Max.})$ is less than $t_{LZ}(\text{Min.})$ both for a given device and from device to device interconnection.

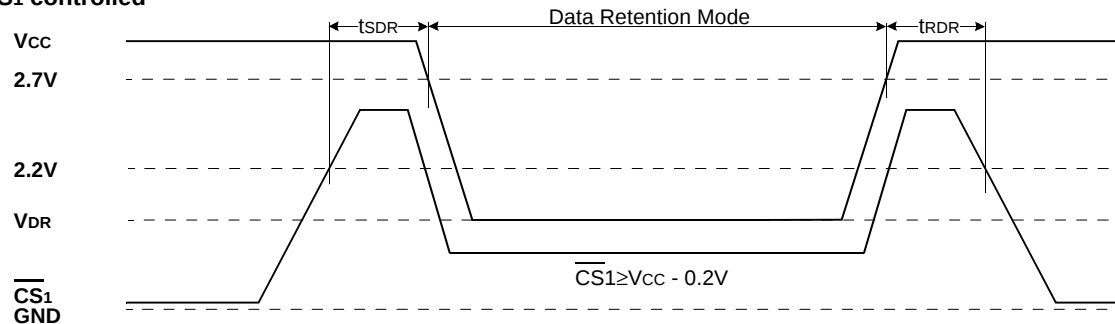
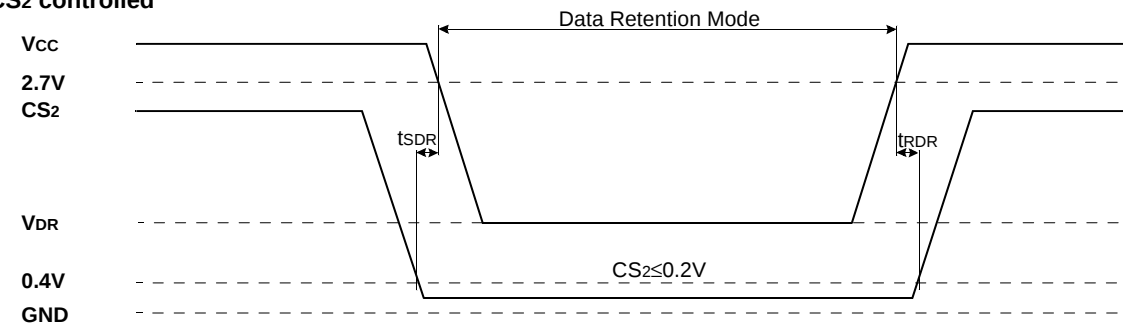
TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{\text{WE}}$ Controlled)TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{\text{CS1}}$ Controlled)

TIMING WAVEFORM OF WRITE CYCLE(3) ($\overline{\text{UB}}$, $\overline{\text{LB}}$ Controlled)

NOTES (WRITE CYCLE)

1. A write occurs during the overlap(t_{WP}) of low $\overline{\text{CS1}}$ and low $\overline{\text{WE}}$. A write begins when $\overline{\text{CS1}}$ goes low and $\overline{\text{WE}}$ goes low with asserting $\overline{\text{UB}}$ or $\overline{\text{LB}}$ for single byte operation or simultaneously asserting $\overline{\text{UB}}$ and $\overline{\text{LB}}$ for double byte operation. A write ends at the earliest transition when $\overline{\text{CS1}}$ goes high and $\overline{\text{WE}}$ goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the $\overline{\text{CS1}}$ going low to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} is applied in case a write ends with $\overline{\text{CS1}}$ or $\overline{\text{WE}}$ going high.

DATA RETENTION WAVE FORM

 $\overline{\text{CS1}}$ controlled $\overline{\text{CS2}}$ controlled

PACKAGE DIMENSION

111-Ball FINE PITCH BGA Package (measured in millimeters)

