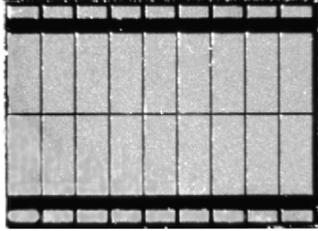


Thin Film Filter Networks



Product may not
be to scale

FEATURES

- Wire bondable
- Standard resistance range: 25 Ω and 50 Ω
- Standard capacitance range:
50 pF, 100 pF, 200 pF, 400 pF
- Resistance tolerance to 1 %
Capacitance tolerance to 5 %
- Capacitor MOS/MNOS
- Resistor material: Tantalum nitride, self-passivating
- Oxidized silicon substrate

The RCN series combines resistor and capacitor technology on a single chip to provide filtering capability together with excellent stability. Specifications below are standard but may be changed and customized for the application and are available in widebody SOIC or DIP packages.

These chips are manufactured using Vishay (EFI) sophisticated Thin Film equipment and manufacturing technology. The RCNs are 100 % electrically tested and visually inspected to MIL-STD-883.

APPLICATIONS

The RCN filter chips are used for low pass filters, RFI & EMI, CMOS digital filters, ECL terminators and power supply filters. Contact our Sales Department for any special configurations or requirements that are needed.

TEMPERATURE COEFFICIENT OF RESISTANCE, VALUES AND COMBOS (Standard)

Absolute TCR = ± 100 ppm/ $^{\circ}$ C

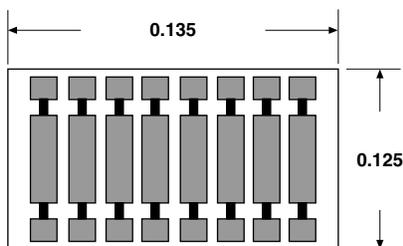
Absolute TCC = $+ 45 \pm 75$ ppm/ $^{\circ}$ C

R	C	R	C
25 Ω	50 pF	50 Ω	50 pF
25 Ω	100 pF	50 Ω	100 pF
25 Ω	200 pF	50 Ω	200 pF
25 Ω	400 pF	50 Ω	400 pF

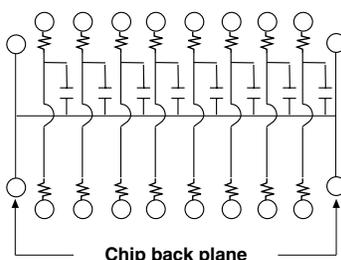
STANDARD ELECTRICAL SPECIFICATIONS

PARAMETER	
Noise, MIL-STD-202, Method 308 100 Ω - 250 k Ω < 100 Ω or > 251 k Ω	- 35 dB typ. - 20 dB typ.
Moisture Resistance, MIL-STD-202, Method 106	± 0.5 % max. $\Delta R/R$
Stability, 100 h, + 125 $^{\circ}$C, 50 mW/Res, at WVDC	± 0.5 % max. $\Delta R/R$ ± 2.0 % max. $\Delta R/R$
Operating Temperature Range	- 55 $^{\circ}$ C to + 125 $^{\circ}$ C
Thermal Shock, MIL-STD-202, Method 107, Test Condition F	± 0.1 % max. $\Delta R/R$
High Temperature Exposure, + 150 $^{\circ}$C, 1000 h	± 0.2 % max. $\Delta R/R$
Insulation Resistance	10^9 min.
Operating Voltage	25 V max.
DC Pwr Rating at - 55 $^{\circ}$C to + 125 $^{\circ}$C (100 V Maximum)	50 mW
5 x Rated Power Short-Time Overload, + 25 $^{\circ}$C, 5 s (100 V Maximum)	± 0.5 % max. $\Delta R/R$

DIMENSIONS in inches



SCHEMATIC



RESISTOR
CAPACITOR
ARRAYS

MECHANICAL SPECIFICATIONS in inches	
PARAMETER	
Chip Size	0.135 x 0.125 ± 0.005 (3.429 x 3.175 ± 0.127 mm)
Chip Thickness	0.010 ± 0.002 (0.254 ± 0.05 mm)
Chip Substrate Material	Oxidized silicon, 10 kÅ minimum SiO ₂
Resistor Material	Tantalum nitride, self-passivating
Bonding Pad Size	0.005 x 0.007 (0.127 x 0.178 mm)
Number of Pads	16 (8 x RC)
Pad Material	10 kÅ minimum aluminum
Backing	3 kÅ minimum gold

Options: Gold bonding pads 15 kÅ minimum thickness
Consult Applications Engineer

ORDERING INFORMATION							
Example: 100 % visualled, 25 Ω ± 20 %, 200 pF ± 20 %, ± 100 ppm/°C, aluminum pads, class H visual inspection							
P/N:	W	RCN	200	250	A	201	M
	INSPECTION	PRODUCT	SERIES	RESISTANCE	RESISTOR	CAPACITOR	CAPACITANCE
	/PACKAGING	FAMILY		VALUE	TOLERANCE	VALUE	TOLERANCE
	W = 100 % visually inspected parts in matrix trays per MIL-STD-883			Use the first 3 significant digits of the resistance and multiplier	B = 0.01 A = 0.1 0 = 1 1 = 10 2 = 100	Use the first 3 significant digits of the capacitance and multiplier	J = 5.0 % K = 10 % M = 20 % N = 25 %
	X = Sample, commercial visually inspected parts loaded in matrix trays (4 % AQL)						



Disclaimer

All product specifications and data are subject to change without notice.

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