

General Description

The DS1110 delay line is an improved replacement for the DS1010. It has ten equally spaced taps providing delays from 5ns to 500ns. The devices are offered in a standard 14-pin DIP, 16-pin SO, or 14-pin TSSOP. The DS1110 series delay lines provide a nominal accuracy of ±5% or ±2ns, whichever is greater, at 5V and +25°C. The DS1110 reproduces the input logic state at the tap 10 output after a fixed delay as specified by the dash number extension of the part number. The DS1110 is designed to produce both leading- and trailing-edge delays with equal precision. Each tap is capable of driving up to ten 74LS type loads. Dallas Semiconductor can customize standard products to meet special needs.

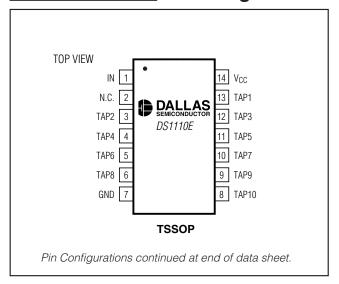
Applications

Communications Equipment Medical Devices Automated Test Equipment PC Peripheral Devices

Features

- ◆ All-Silicon, 5V, 10-Tap Delay Line
- ◆ Improved, Drop-In Replacement for the DS1010
- ◆ 10 Taps Equally Spaced
- Delays are Stable and Precise
- ◆ Leading- and Trailing-Edge Accuracy
- ◆ Delay Tolerance ±5% or ±2ns, whichever is Greater, at 5V and +25°C
- Economical
- Auto-Insertable, Low Profile
- ♦ Low-Power CMOS
- ◆ TTL/CMOS Compatible
- ◆ Vapor Phase, IR, and Wave Solderable
- ♦ Fast-Turn Prototypes
- Delays Specified Over Commercial and Industrial **Temperature Ranges**
- Custom Delays Available
- ◆ Standard 14-Pin DIP, 16-Pin SO or, 14-Pin TSSOP

Pin Configurations



Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
DS1110-XXX	-40°C to +85°C	14 DIP
DS1110E-XXX	-40°C to +85°C	14 TSSOP
DS1110S-XXX	-40°C to +85°C	16 SO

Selector Guide appears at end of data sheet.

ABSOLUTE MAXIMUM RATINGS

Voltage on Any Pin Relative to Ground0.5V to +6.0V	Storage Temperature Range55°C to +125°C
Operating Temperature Range40°C to +85°C	Soldering TemperatureSee IPC/JEDEC J-STD-020A

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

 $(VCC = 5.0V \pm 5\%, T_A = -40^{\circ}C \text{ to } +85^{\circ}C.)$

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	Vcc	(Note 1)	4.75	5.0	5.25	V
High-Level Input Voltage	V _{IH}	(Note 1)	2.4		V _C C + 0.3	V
Low-Level Input Voltage	VIL	(Note 1)	-0.3		+0.8	V
Input Leakage Current	II	$0V \le V_1 \le V_{CC}$	-1.0		+1.0	μΑ
Active Current	Icc	V _{CC} = max, period = min (Note 2)		40	150	mA
High-Level Output Current	Іон	V _{CC} = min, V _{OH} = 2.3V			-1.0	mA
Low-Level Output Current	loL	$V_{CC} = min, V_{OL} = 0.5V$	12			mA

AC ELECTRICAL CHARACTERISTICS

 $(VCC = 5.0V \pm 5\%, T_A = -40^{\circ}C \text{ to } +85^{\circ}C.)$

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Pulse Width	twı	(Note 6)	10% of tap 10			ns
		+25°C, 5.0V (Notes 3, 5, 6, 7)	-2	Table 1	+2	ns
Input-to-Tap Delay (Delays ≤ 40ns)	tPLH tPHL	0°C to +70°C (Notes 4-7)	-3	Table 1	+3	
(Delays \(\simeg\) 40115)	YPHL	-40°C to +85°C (Notes 4-7)	-4	Table 1	+4	
		+25°C, 5.0V (Notes 3, 5, 6, 7)	-5	Table 1	+5	%
Input-to-Tap Delay (Delays > 40ns)	tPLH tPHL	0°C to +70°C (Notes 4-7)	-8	Table 1	+8	
(Delays > 40113)	YPHL	-40°C to +85°C (Notes 4-7)	-13	Table 1	+13	
Power-Up Time	tpu				200	ms
Input Period	Period	(Note 8)	2 (t _{Wl}) or whiche is great	ver		ns

CAPACITANCE

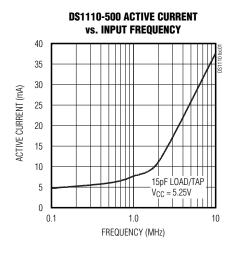
 $(T_A = +25^{\circ}C.)$

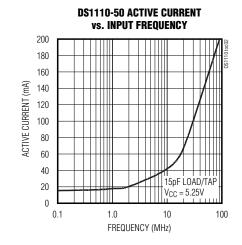
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Capacitance	CIN		•	5	10	рF

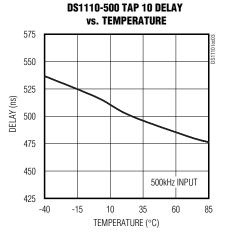
- Note 1: All voltages are referenced to ground.
- Note 2: Measured with outputs open.
- Note 3: Initial tolerances are ± with respect to the nominal value at +25°C and V_{CC} = 5.0V for both leading and trailing edges.
- **Note 4:** Temperature and voltage tolerances are with respect to the actual delay measured over stated temperature range and a 4.75V to 5.25V range.
- Note 5: Intermediate delay values are available on a custom basis.
- Note 6: See Test Conditions section.
- **Note 7:** All tap delays tend to vary unidirectionally with temperature or voltage changes. For example, if tap 1 slows down, all other taps also slow down; tap 3 can never be faster than tap 2.
- Note 8: Pulse width and period specifications may be exceeded; however, accuracy is application sensitive (decoupling, layout, etc.).

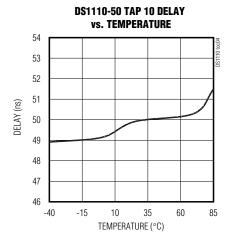
_Typical Operating Characteristics

($V_{CC} = 5.0V$, $T_A = +25$ °C, unless otherwise noted.)



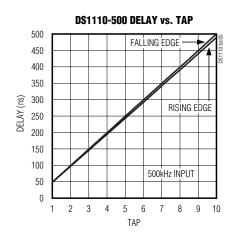


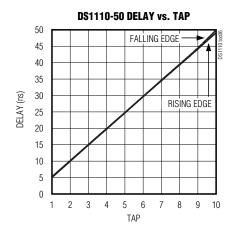


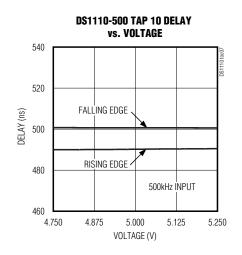


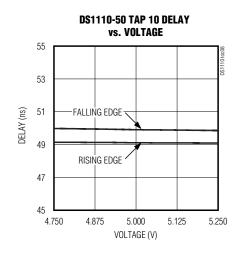
Typical Operating Characteristics (continued)

($V_{CC} = 5.0V$, $T_A = +25$ °C, unless otherwise noted.)









Pin Description

Р	IN	NAME	FUNCTION
DIP/TSSOP	P SO NAME		FUNCTION
1	1	IN	Input
2	2, 3, 15	N.C.	No Connection
7	8	GND	Ground
13, 3, 12, 4, 11, 5, 10, 6, 9, 8	14, 4, 13, 5, 12, 6, 11, 7, 10, 9	Tap 1-Tap 10	Tap Output Number
14	16	Vcc	5.0V

Detailed Description

The DS1110 delay line is an improved replacement for the DS1010. It has ten equally spaced taps providing delays from 5ns to 500ns. The devices are offered in a standard 14-pin DIP, 16-pin SO, or 14-pin TSSOP. The DS1110 series delay lines provide a nominal accuracy of ±5% or ±2ns, whichever is greater, at 5V and +25°C. The DS1110 reproduces the input logic state at the tap 10 output after a fixed delay as specified by the dash number extension of the part number. The DS1110 is designed to produce both leading- and trailing-edge delays with equal precision. Each tap is capable of driving up to ten 74LS type loads. Dallas Semiconductor can customize standard products to meet special needs. For special requests call 972-371-4348.

Table 1. Part Number by Delay (tphl, tplh)

PART	TOTAL DELAY* (ns)	DELAY/TAP (ns)
DS1110-50	50	5
DS1110-60	60	6
DS1110-75	75	7.5
DS1110-80	80	8
DS1110-100	100	10
DS1110-125	125	12.5
DS1110-150	150	15
DS1110-175	175	17.5
DS1110-200	200	20
DS1110-250	250	25
DS1110-300	300	30
DS1110-350	350	35
DS1110-400	400	40
DS1110-450	450	45
DS1110-500	500	50

^{*}Custom delays are available.

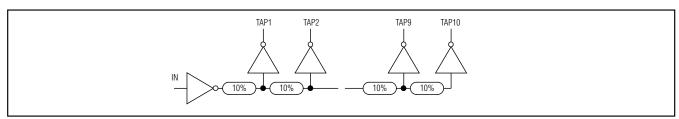


Figure 1. Logic Diagram

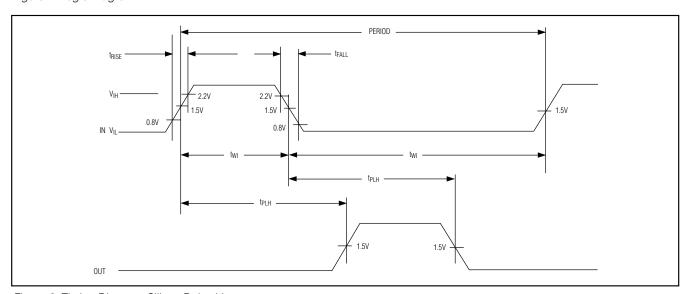


Figure 2. Timing Diagram: Silicon Delay Line

Terminology

Period: The time elapsed between the leading edge of the first pulse and the leading edge of the following pulse.

twi (Pulse Width): The elapsed time on the pulse between the 1.5V point on the leading edge and the 1.5V point on the trailing edge, or the 1.5V point on the trailing edge and the 1.5V point on the leading edge.

TRISE (Input Rise Time): The elapsed time between the 20% and the 80% point on the leading edge of the input pulse.

tFALL (Input Fall Time): The elapsed time between the 80% and the 20% point on the trailing edge of the input pulse.

tpLH (Time Delay, Rising): The elapsed time between the 1.5V point on the leading edge of the input pulse and the 1.5V point on the leading edge of any tap output pulse.

tpHL (Time Delay, Falling): The elapsed time between the 1.5V point on the trailing edge of the input pulse and the 1.5V point on the trailing edge of any tap output pulse.

Test Setup Description

Figure 3 illustrates the hardware configuration used for measuring the timing parameters on the DS1110. A precision pulse generator under software control produces the input waveform. Time delays are measured by a time interval counter (20ps resolution) connected

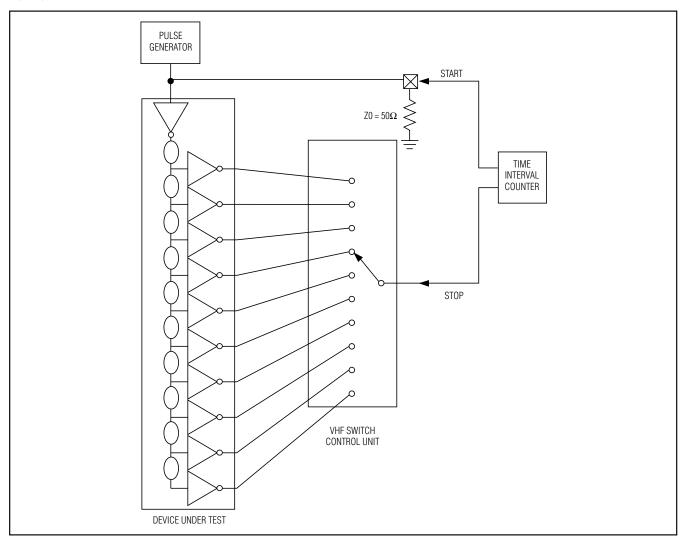


Figure 3. Test Circuit



between the input and each tap. Each tap is selected and connected to the counter by a VHF switch-control unit. All measurements are fully automated, with each instrument controlled by a central computer over an IEEE-488 bus.

Output

Each output is loaded with the equivalent of one 74FO4 input gate. Delay is measured at the 1.5V level on the rising and falling edge.

Chip Information

TRANSISTOR COUNT: 6813

Table 2. Test Conditions

INPUT	CONDITION	
Ambient Temperature	+25°C ±3°C	
Supply Voltage (V _{CC})	5.0V ±0.1V	
Input Dulco	High = $3.0V \pm 0.1V$	
Input Pulse	$Low = 0.0V \pm 0.1V$	
Source Impedance	50Ω max	
Rise and Fall Time	3ns max	
Pulse Width	500ns (1µs for -500ns)	
Period	1μs (2μs for -500ns)	

Note: The above conditions are for test only and do not restrict the operation of the device under other data sheet conditions.

Selector Guide

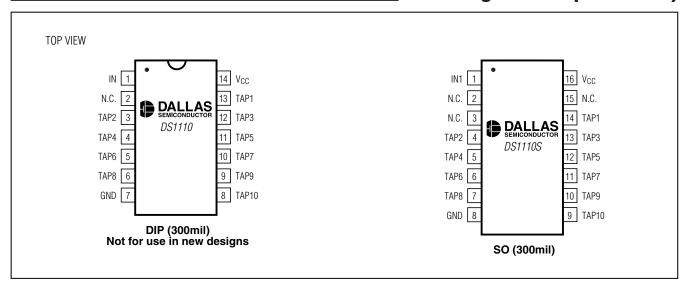
PART	TEMP RANGE	PIN- PACKAGE	TOTAL DELAY (ns)*
DS1110-50	-40°C to +85°C	14 DIP	50
DS1110-60	-40°C to +85°C	14 DIP	60
DS1110-75	-40°C to +85°C	14 DIP	75
DS1110-80	-40°C to +85°C	14 DIP	80
DS1110-100	-40°C to +85°C	14 DIP	100
DS1110-125	-40°C to +85°C	14 DIP	125
DS1110-150	-40°C to +85°C	14 DIP	150
DS1110-175	-40°C to +85°C	14 DIP	175
DS1110-200	-40°C to +85°C	14 DIP	200
DS1110-250	-40°C to +85°C	14 DIP	250
DS1110-300	-40°C to +85°C	14 DIP	300
DS1110-350	-40°C to +85°C	14 DIP	350
DS1110-400	-40°C to +85°C	14 DIP	400
DS1110-450	-40°C to +85°C	14 DIP	450
DS1110-500	-40°C to +85°C	14 DIP	500
DS1110E-50	-40°C to +85°C	14 TSSOP	50
DS1110E-60	-40°C to +85°C	14 TSSOP	60
DS1110E-75	-40°C to +85°C	14 TSSOP	75
DS1110E-80	-40°C to +85°C	14 TSSOP	80
DS1110E-100	-40°C to +85°C	14 TSSOP	100
DS1110E-125	-40°C to +85°C	14 TSSOP	125
DS1110E-150	-40°C to +85°C	14 TSSOP	150
DS1110E-175	-40°C to +85°C	14 TSSOP	175
DS1110E-200	-40°C to +85°C	14 TSSOP	200

PART	TEMP RANGE	PIN- PACKAGE	TOTAL DELAY (ns)*
DS1110E-250	-40°C to +85°C	14 TSSOP	250
DS1110E-300	-40°C to +85°C	14 TSSOP	300
DS1110E-350	-40°C to +85°C	14 TSSOP	350
DS1110E-400	-40°C to +85°C	14 TSSOP	400
DS1110E-450	-40°C to +85°C	14 TSSOP	450
DS1110E-500	-40°C to +85°C	14 TSSOP	500
DS1110S-50	-40°C to +85°C	16 SO	50
DS1110S-60	-40°C to +85°C	16 SO	60
DS1110S-75	-40°C to +85°C	16 SO	75
DS1110S-80	-40°C to +85°C	16 SO	80
DS1110S-100	-40°C to +85°C	16 SO	100
DS1110S-125	-40°C to +85°C	16 SO	125
DS1110S-150	-40°C to +85°C	16 SO	150
DS1110S-175	-40°C to +85°C	16 SO	175
DS1110S-200	-40°C to +85°C	16 SO	200
DS1110S-250	-40°C to +85°C	16 SO	250
DS1110S-300	-40°C to +85°C	16 SO	300
DS1110S-350	-40°C to +85°C	16 SO	350
DS1110S-400	-40°C to +85°C	16 SO	400
DS1110S-450	-40°C to +85°C	16 SO	450
DS1110S-500	-40°C to +85°C	16 SO	500

^{*}Custom delays are available.



Pin Configurations (continued)



Package Information

For the latest package outline information, go to **www.maxim-ic. com/packages**.

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