

HM62256A Series

32,768-word × 8-bit High Speed CMOS Static RAM

The Hitachi HM62256A is a CMOS static RAM organized 32-kword × 8-bit. It realizes higher performance and low power consumption by employing 0.8 μm Hi-CMOS process technology. The device, packaged in a 8 × 14 mm TSOP with thickness of 1.2 mm, 450-mil SOP (foot print pitch width), 600-mil plastic DIP, or 300-mil plastic DIP, is available for high density mounting. TSOP package is suitable for cards, and reverse type TSOP is also provided. It offers low power standby power dissipation; therefore, it is suitable for battery back up system.

Features

- High speed: Fast Access time 85/100/120/150 ns (max)
- Low Power
Standby: 5 μW (typ) (L/L-SL version)
Operation: 40 mW (typ) (f = 1 MHz)
- Single 5 V supply
- Completely static memory
No clock or timing strobe required
- Equal access and cycle times
- Common data input and output: Three state output
- Directly TTL compatible: All inputs and outputs
- Capability of battery back up operation

Ordering Information

Type No.	Access time	Package
HM62256AP-8	85 ns	600-mil 28-pin plastic DIP (DP-28)
HM62256AP-10	100 ns	
HM62256AP-12	120 ns	
HM62256AP-15	150 ns	
HM62256ALP-8	85 ns	
HM62256ALP-10	100 ns	
HM62256ALP-12	120 ns	
HM62256ALP-15	150 ns	
HM62256ALP-8SL	85 ns	
HM62256ALP-10SL	100 ns	
HM62256ALP-12SL	120 ns	
HM62256ALP-15SL	150 ns	
HM62256ASP-8	85 ns	300-mil 28-pin plastic DIP (DP-28NA)
HM62256ASP-10	100 ns	
HM62256ASP-12	120 ns	
HM62256ASP-15	150 ns	
HM62256ALSP-8	85 ns	
HM62256ALSP-10	100 ns	
HM62256ALSP-12	120 ns	
HM62256ALSP-15	150 ns	
HM62256ALSP-8SL	85 ns	
HM62256ALSP-10SL	100 ns	
HM62256ALSP-12SL	120 ns	
HM62256ALSP-15SL	150 ns	
HM62256AFP-8T	85 ns	450-mil 28-pin plastic SOP (FP-28DA)
HM62256AFP-10T	100 ns	
HM62256AFP-12T	120 ns	
HM62256AFP-15T	150 ns	
HM62256ALFP-8T	85 ns	
HM62256ALFP-10T	100 ns	
HM62256ALFP-12T	120 ns	
HM62256ALFP-15T	150 ns	
HM62256ALFP-8SLT	85 ns	
HM62256ALFP-10SLT	100 ns	
HM62256ALFP-12SLT	120 ns	
HM62256ALFP-15SLT	150 ns	

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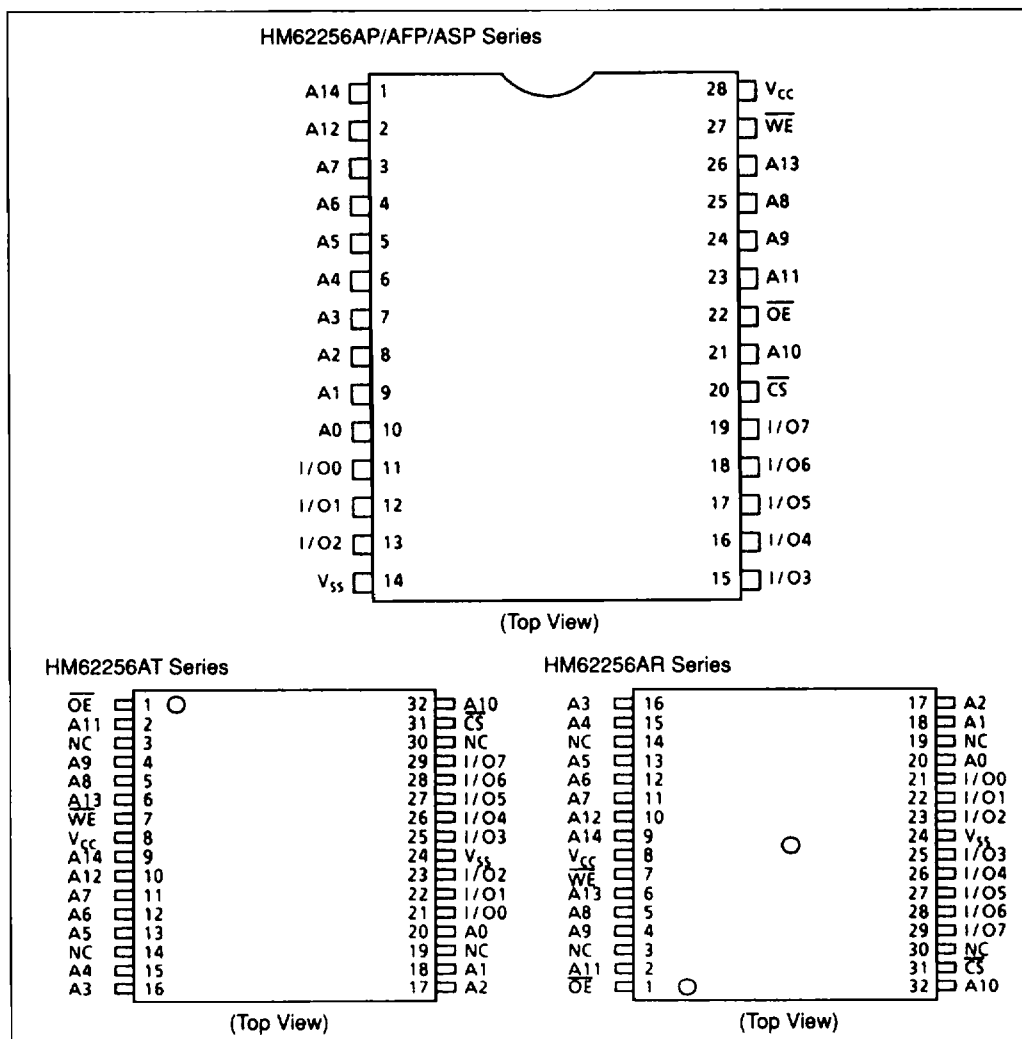
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TSOP Series

Type No.	Access time	Package	Type No.	Access time	Package
HM62256ALT-8	85 ns	8 mm × 14 mm	HM62256ALR-8	85 ns	8 mm × 14 mm
HM62256ALT-10	100 ns	32-pin TSOP	HM62256ALR-10	100 ns	32-pin TSOP
HM62256ALT-12	120 ns	(normal type)	HM62256ALR-12	120 ns	(reverse type)
HM62256ALT-15	150 ns	(TFP-32DA)	HM62256ALR-15	150 ns	(TFP-32DAR)
HM62256ALT-8SL	85 ns		HM62256ALR-8SL	85 ns	
HM62256ALT-10SL	100 ns		HM62256ALR-10SL	100 ns	
HM62256ALT-12SL	120 ns		HM62256ALR-12SL	120 ns	
HM62256ALT-15SL	150 ns		HM62256ALR-15SL	150 ns	

Pin Arrangement



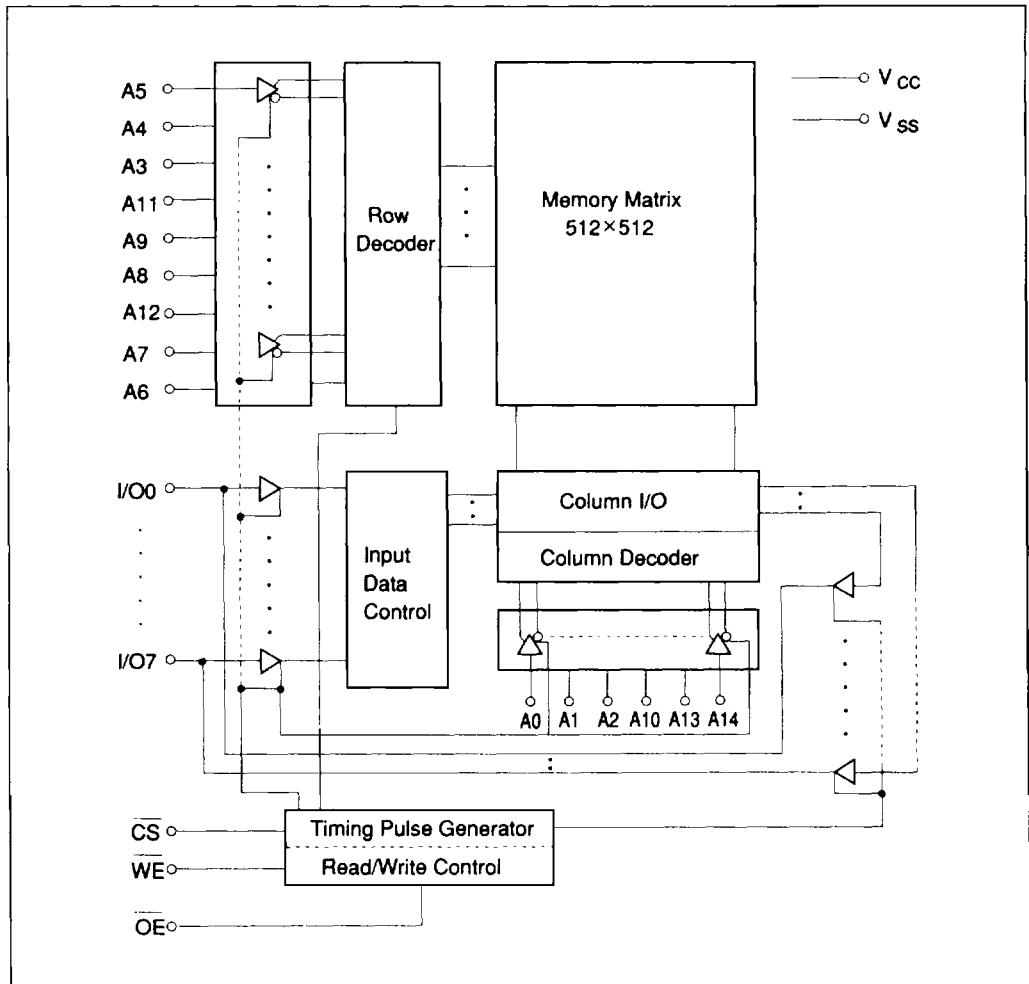
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Pin Description

Symbol	Function
A0 – A14	Address
I/O0 – I/O7	Input/output
$\overline{CS}$	Chip select
WE	Write enable

Symbol	Function
OE	Output enable
NC	No connection
V _{CC}	Power supply
V _{SS}	Ground

Block Diagram



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Function Table

WE	CS	OE	Mode	V _{CC} current	I/O pin	Ref. cycle
X	H	X	Not selected	I _{SB} , I _{SB1}	High-Z	—
H	L	H	Output disable	I _{CC}	High-Z	—
H	L	L	Read	I _{CC}	Dout	Read cycle (1)–(3)
L	L	H	Write	I _{CC}	Din	Write cycle (1)
L	L	L	Write	I _{CC}	Din	Write cycle (2)

Note: X: H or L

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V _{SS}	V _T	−0.5*1 to +7.0	V
Power dissipation	P _T	1.0	W
Operating temperature	T _{opr}	0 to +70	°C
Storage temperature	T _{stg}	−55 to +125	°C
Storage temperature under bias	T _{bias}	−10 to +85	°C

Note: 1. V_T min = −3.0 V for pulse half-width ≤ 50 ns

Recommended DC Operating Conditions (T_a = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
	V _{SS}	0	0	0	V
Input high (logic 1) voltage	V _{IH}	2.2	—	6.0	V
Input low (logic 0) voltage	V _{IL}	−0.5*1	—	0.8	V

Note: 1. V_{IL} min = −3.0 V for pulse half-width ≤ 50 ns

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DC Characteristics ($T_a = 0$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Min	Typ* ¹	Max	Unit	Test conditions
Input leakage current	$ I_{LI} $	—	—	1	μA	$V_{in} = V_{SS}$ to V_{CC}
Output leakage current	$ I_{LO} $	—	—	1	μA	$\overline{CS} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$, $V_{I/O} = V_{SS}$ to V_{CC}
Operating V_{CC} current	I_{CC}	—	6	15	mA	$\overline{CS} = V_{IL}$, others = V_{IH}/V_{IL} $I_{out} = 0\text{ mA}$
HM62256A-8	I_{CC1}	—	33	50	mA	min cycle, duty = 100%, $I_{I/O} = 0\text{ mA}$ $\overline{CS} = V_{IL}$, others = V_{IH}/V_{IL}
HM62256A-10		—	30	50		
HM62256A-12		—	27	45		
HM62256A-15		—	24	40		
	I_{CC2}	—	5	15	mA	Cycle time = $1\mu\text{s}$, $I_{I/O} = 0\text{ mA}$ $\overline{CS} = V_{IL}$, $V_{IH} = V_{CC}$, $V_{IL} = 0$
Standby V_{CC} current	I_{SB}	—	0.3	2	mA	$\overline{CS} = V_{IH}$
	I_{SB1}	—	0.01	1	mA	$V_{in} \geq 0\text{ V}$ $\overline{CS} \geq V_{CC} - 0.2\text{ V}$
		—	0.3^{*2}	100^{*2}	μA	
		—	0.3^{*3}	50^{*3}	μA	
Output low voltage	V_{OL}	—	—	0.4	V	$I_{OL} = 2.1\text{ mA}$
Output high voltage	V_{OH}	2.4	—	—	V	$I_{OH} = -1.0\text{ mA}$

- Notes: 1. Typical values are at $V_{CC} = 5.0\text{ V}$, $T_a = +25^\circ\text{C}$ and not guaranteed.
2. This characteristics is guaranteed only for L-version.
3. This characteristics is guaranteed only for L-SL version.

Capacitance ($T_a = 25^\circ\text{C}$, $f = 1\text{ MHz}$)*¹

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance	C_{in}	—	—	6	pF	$V_{in} = 0\text{ V}$
Input/output capacitance	$C_{I/O}$	—	—	8	pF	$V_{I/O} = 0\text{ V}$

- Note: 1. This parameter is sampled and not 100% tested.

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AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, unless otherwise noted.)

Test Conditions

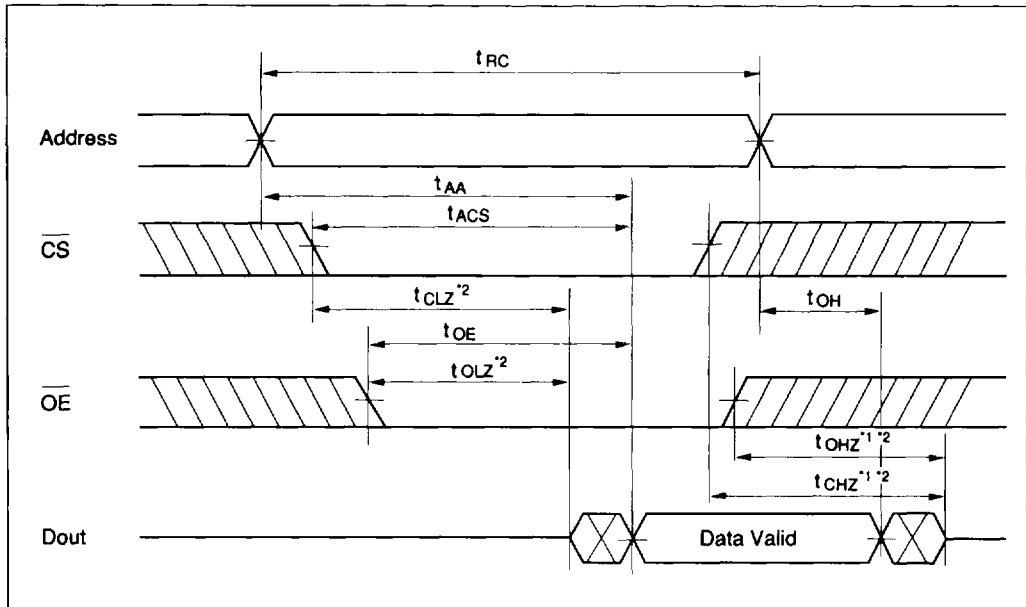
- Input pulse levels: 0.8 V to 2.4 V
- Input and output timing reference levels: 1.5 V
- Input rise and fall times: 5 ns
- Output load: 1 TTL Gate + C_L (100 pF)
(Including scope & jig)

Read Cycle

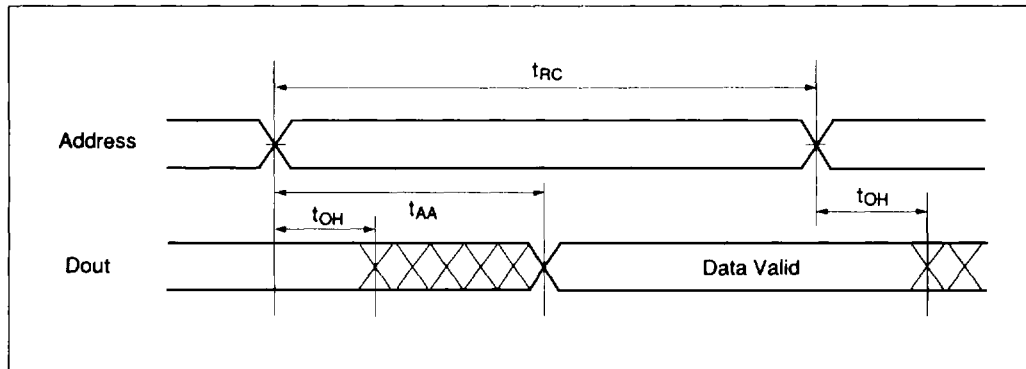
Parameter	Symbol	HM62256A-8		HM62256A-10		HM62256A-12		HM62256A-15		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Read cycle time	t _{RC}	85	—	100	—	120	—	150	—	ns	
Address access time	t _{AA}	—	85	—	100	—	120	—	150	ns	
Chip select access time	t _{ACS}	—	85	—	100	—	120	—	150	ns	
Output enable to output valid	t _{OE}	—	45	—	50	—	60	—	70	ns	
Chip selection to output in low-Z	t _{CLZ}	10	—	10	—	10	—	10	—	ns	2
Output enable to output in low-Z	t _{OLZ}	5	—	5	—	5	—	5	—	ns	2
Chip deselection to output in high-Z	t _{CHZ}	0	30	0	35	0	40	0	50	ns	1, 2
Output disable to output in high-Z	t _{OHZ}	0	30	0	35	0	40	0	50	ns	1, 2
Output hold from address change	t _{OH}	5	—	10	—	10	—	10	—	ns	

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Read Timing Waveform (1) *3

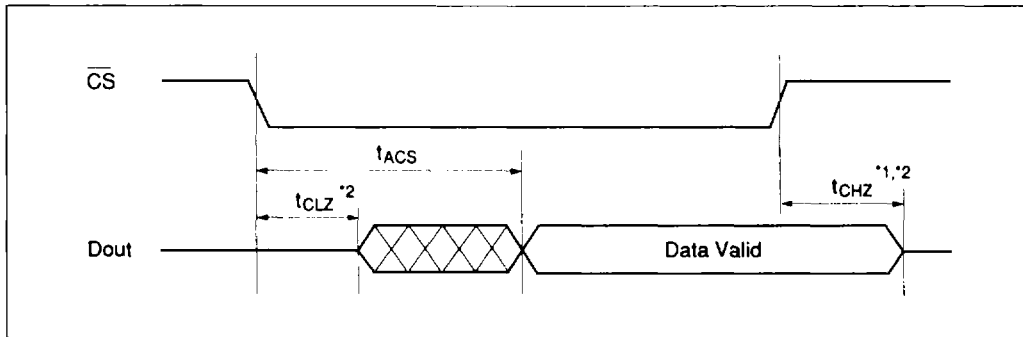


Read Timing Waveform (2) *3 *4 *6



HM62256A Series

Read Timing Waveform (3) *3 *5 *6



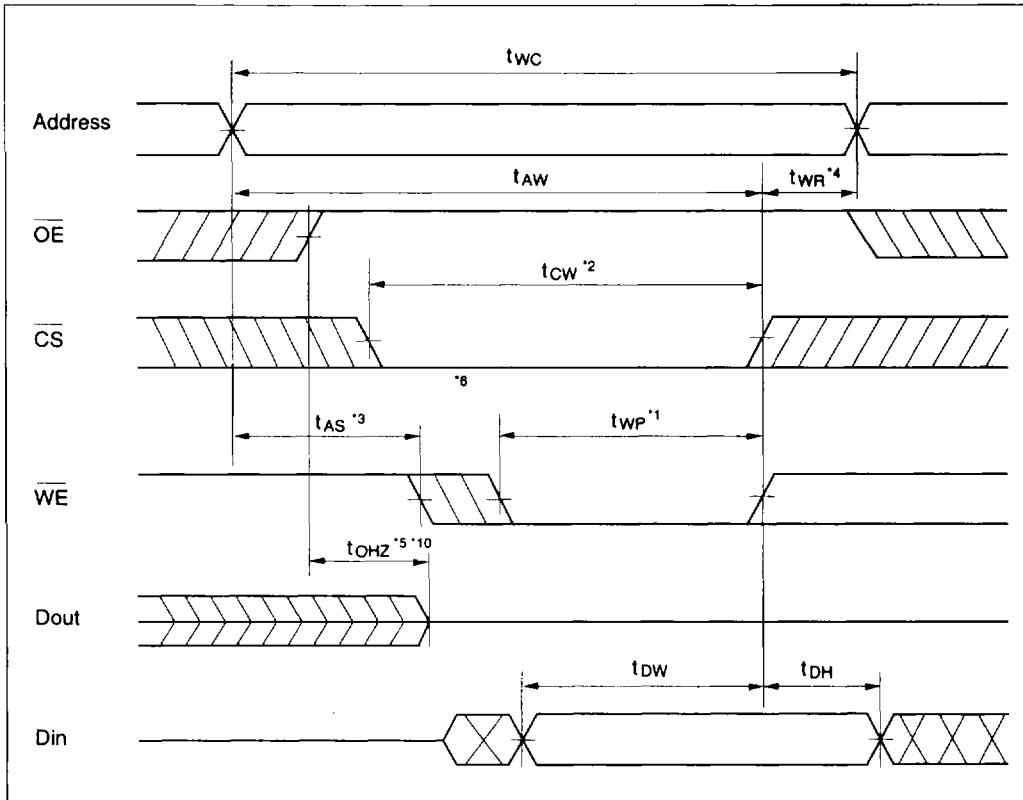
- Notes:
1. t_{CHZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
 2. This parameter is sampled and not 100% tested.
 3. WE is high for read cycle.
 4. Device is continuously selected, $\overline{CS} = V_{IL}$.
 5. Address Valid prior to or coincident with $\overline{CS}$ transition Low.
 6. $OE = V_{IL}$.

Write Cycle

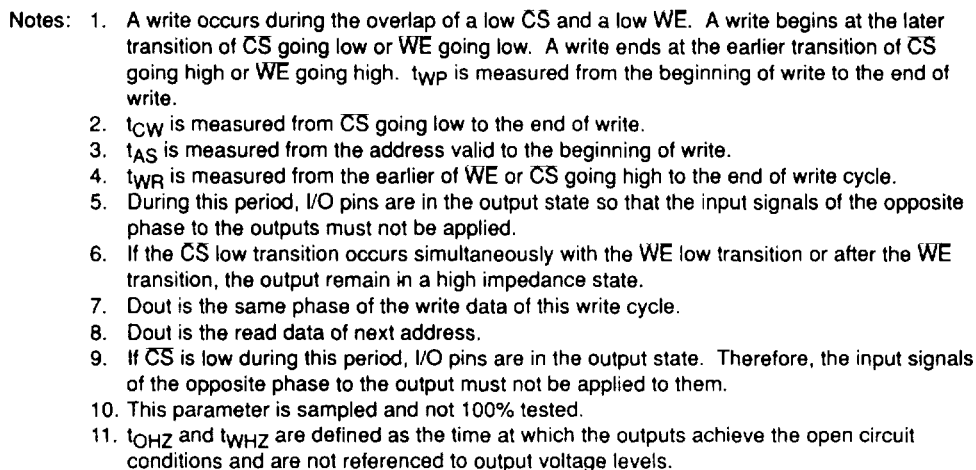
Parameter	Symbol	HM62256A-8		HM62256A-10		HM62256A-12		HM62256A-15		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Write cycle time	t_{WC}	85	—	100	—	120	—	150	—	ns	
Chip selection to end of write	t_{CW}	75	—	80	—	85	—	100	—	ns	2
Address setup time	t_{AS}	0	—	0	—	0	—	0	—	ns	3
Address valid to end of write	t_{AW}	75	—	80	—	85	—	100	—	ns	
Write pulse width	t_{WP}	55	—	60	—	70	—	90	—	ns	1
Write recovery time	t_{WR}	0	—	0	—	0	—	0	—	ns	4
WE to output in high-Z	t_{WHZ}	0	30	0	35	0	40	0	50	ns	10
Data to write time overlap	t_{DW}	40	—	40	—	50	—	60	—	ns	
Data hold from write time	t_{DH}	0	—	0	—	0	—	0	—	ns	
Output active from end of write	t_{OW}	5	—	5	—	5	—	5	—	ns	10
Output disable to output in high-Z	t_{OHZ}	0	30	0	35	0	40	0	50	ns	10, 11

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Write Timing Waveform (1) ($\overline{\text{OE}}$ Clock)



Write Timing Waveform (2) ($\overline{\text{OE}}$ Low Fixed)

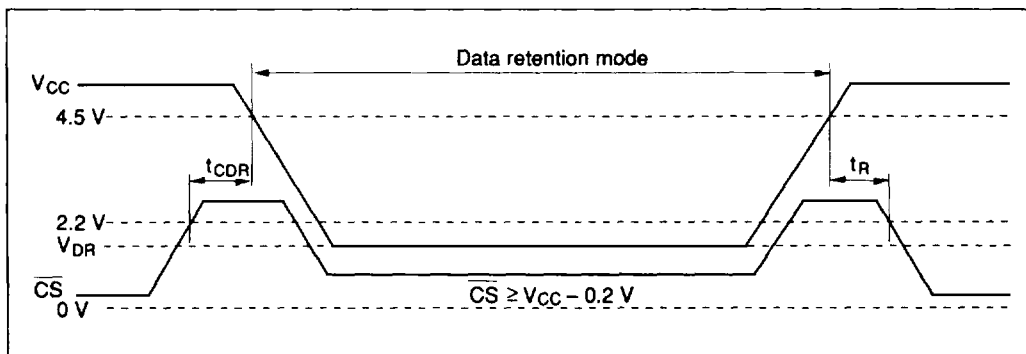


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Low V_{CC} Data Retention Characteristics ($T_a = 0$ to $+70^\circ\text{C}$)

This characteristics is guaranteed only for L/L-SL version.

Parameter	Symbol	Min	Typ ^{*1}	Max	Unit	Test conditions
V_{CC} for data retention	V_{DR}	2	—	—	V	$\overline{CS} \geq V_{CC} - 0.2 \text{ V}$, $V_{in} \geq 0 \text{ V}$
Data retention current	I_{CCDR}	—	0.2	30^{*2}	μA	$V_{CC} = 3.0 \text{ V}$, $V_{in} \geq 0 \text{ V}$
		—	0.2	10^{*3}	μA	$\overline{CS} \geq V_{CC} - 0.2 \text{ V}$
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	See retention waveform
Operation recovery time	t_R	t_{RC}^{*4}	—	—	ns	

Low V_{CC} Data Retention Timing Waveform


- Notes:
1. Typical values are at $V_{CC} = 3.0 \text{ V}$, $T_a = +25^\circ\text{C}$ and not guaranteed.
 2. $20 \mu\text{A}$ max at $T_a = 0$ to $+40^\circ\text{C}$. (only for L-version)
 3. $3 \mu\text{A}$ max at $T_a = 0$ to $+40^\circ\text{C}$. (only for L-SL version)
 4. t_{RC} = read cycle time.
 5. $\overline{CS}$ controls address buffer, WE buffer, OE buffer, and Din buffer. If $\overline{CS}$ controls data retention mode, V_{in} levels (address, WE, OE, I/O) can be in the high impedance state.