# CS-8165

# 8V/5V Low Dropout Dual Regulator with ENABLE

## Description

The CS-8165 is a low dropout, 8V/5V dual linear regulator. The second 5V/20mA output for powering systems with standby memory. Quiescent current drain is less than 2mA when supplying 10mA loads from the standby regulator.

In automotive applications, the CS-8165 and all regulated circuits are protected from reverse battery installations, and over voltage transients. During line transients, such as a 60V load dump, the 750mA output will automatically shut down to protect both internal circuits and the load, while the second output will continue to power any standby load.

The CS-8165 is packaged in a 5-lead TO-220, with copper tab for connection to a heat sink, if necessary.

## Features

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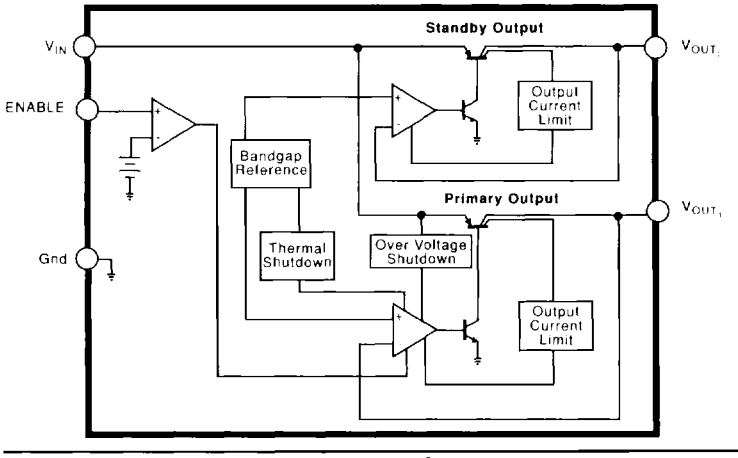
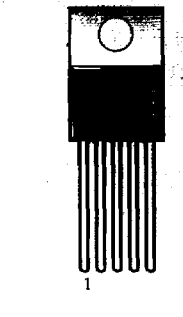
### Absolute Maximum Ratings

Input Voltage
- Operating Range ..... –0.5V to 26V
- Overvoltage Protection ..... 60V

Internal Power Dissipation ..... Internally Limited
Operating Temperature Range ..... –40°C to +125°C
Junction Temperature Range ..... –40°C +150°C
Storage Temperature Range ..... –65°C to +150°C
Soldering Lead Temperature: TO-220 ( 10sec) ..... 260°C

### Block Diagram




1 $V_{IN}$
2 $V_{OUT_1}$
3 Gnd
4 ENABLE
5 $V_{OUT_2}$

CSC™ CHERRY SEMICONDUCTOR

Cherry Semiconductor Corporation
2000 South County Trail
East Greenwich, Rhode Island 02818-1530
Tel: (401)885-3600 Fax (401)885-5786
email: info@cherry-semi.com

**Electrical Characteristics for $V_O$: $V_{IN}$ = 14V, $I_O$ = 500mA, -40°C ≤ $T_J$ ≤ +150°C unless otherwise specified**

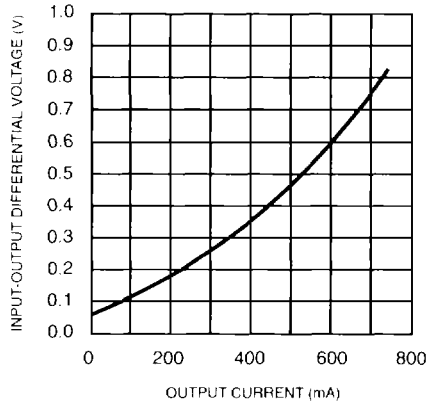
| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **■ Output Stage ($V_{OUT_1}$)** | | | | | |
| Output Voltage, $V_{OUT_1}$ | 13V≤$V_{IN}$≤26V, $I_{OUT_1}$≤500mA, | 7.6 | 8.0 | 8.4 | V |
| **Dropout Voltage** | **$I_{OUT_1}$=500mA** | | | **0.60** | **V** |
| Line Regulation | 13V≤$V_{IN}$≤16V, $I_{OUT_1}$=5mA | | 15 | 80 | mV |
| **Load Regulation** | **5mA≤ $I_{OUT_1}$≤500mA** | | **15** | **80** | **mV** |
| Quiescent Current | $I_{OUT_1}$<10mA, No Load on $V_{OUT_2}$ | | 3 | 7 | mA |
| | $I_{OUT_1}$=500mA, No Load on $V_{OUT_2}$ | | 40 | 100 | mA |
| | $I_{OUT_1}$=750mA, No Load on $V_{OUT_2}$ | | 90 | | mA |
| **Ripple Rejection** | **f=120Hz** | | **53** | | **dB** |
| Current Limit | | 0.75 | 1.40 | 2.50 | A |
| **Maximum Line Transient** | **$V_{OUT_1}$≤13V** | **60** | | | **V** |
| Reverse Polarity Input Voltage, DC | $V_{OUT_1}$≥-0.6V, 10Ω Load | -18 | -30 | | V |
| **Reverse Polarity Input Voltage, Transient** | **1% Duty Cycle, t=100ms, $V_{OUT}$≥-6V, 10Ω Load** | **-50** | **-80** | | **V** |
| Output Noise Voltage | 10Hz-100kHz | | 100 | | μVrms |
| **Long Term Stability** | | | **50** | | **mV/khr** |
| Output Impedance | 500mA DC and 10mA rms, 100Hz-10kHz | | 200 | | mΩ |
| **■ Standby Output ($V_{OUT_2}$)** | | | | | |
| Output Voltage, ($V_{OUT_2}$) | 6V≤$V_{IN}$≤26V | 4.75 | 5.00 | 5.25 | V |
| **Dropout Voltage** | **$I_{OUT_2}$≤10mA** | | **0.55** | **0.70** | **V** |
| Line Regulation | 6V≤$V_{IN}$≤26V | | 4 | 50 | mV |
| **Load Regulation** | **1mA≤$I_{OUT_2}$≤10mA** | | **10** | **50** | **mV** |
| Quiescent Current | $I_{OUT_2}$<10mA, -40°C≤$T_J$≤+125°C $V_{OUT_1}$ OFF | | 2 | 3 | mA |
| **Ripple Rejection** | **f=120Hz** | | **66** | | **dB** |
| Current Limit | | 25 | 70 | | mA |
| **Output Noise Voltage** | **10Hz-100kHz** | | **300** | | **μV** |
| Long Term Stability | | | 20 | | mV/kh |
| **Output Impedance** | **10mA DC and 1mA rms, 100Hz-10kHz** | | 1 | | **Ω** |
| **■ ENABLE Function (ENABLE)** | | | | | |
| Input ENABLE Threshold | $V_{OUT_1}$ Off | | 1.25 | 0.80 | V |
| | $V_{OUT_1}$ On | 2.00 | 1.25 | | V |
| **Input ENABLE Current** | **Input Voltage Range 0 to 26V** | **-10** | | **10** | **μA** |

**Package Pin Description**

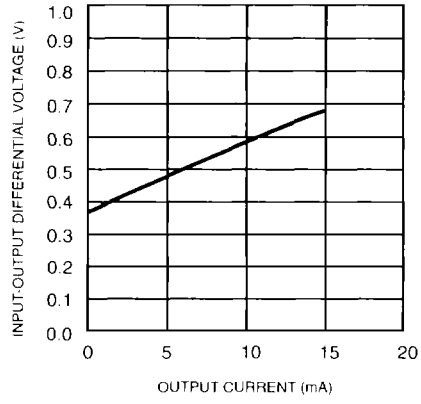
| PACKAGE PIN # | PIN SYMBOL | FUNCTION |
|---|---|---|
| **TO-220** | | |
| 1 | $V_{IN}$ | Supply voltage, usually direct from battery. |
| **2** | **$V_{OUT_1}$** | **Regulated output 8V, 750mA (typ)** |
| 3 | Gnd | Ground connection. |
| **4** | **ENABLE** | **CMOS compatible input pin; switches $V_{OUT_1}$ on and off. When ENABLE is high $V_{OUT_1}$ is active.** |
| 5 | $V_{OUT_2}$ | Standby output 5V, 20mA (typ); always on. |

## Typical Performance Characteristics

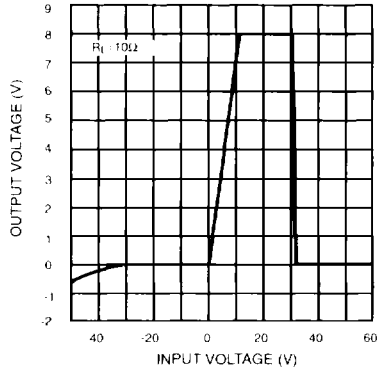
### Dropout Voltage vs. Output Current



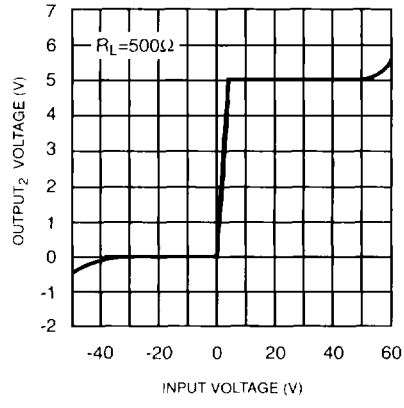

### Standby Dropout Voltage vs. Output Current



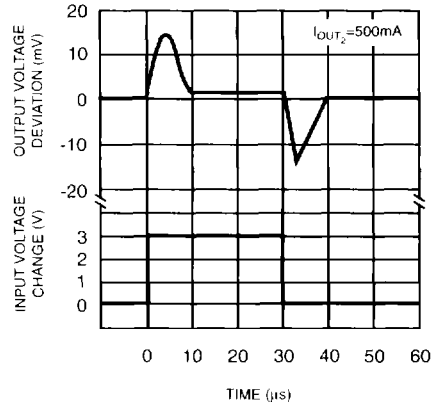

### Output Voltage vs. Input Voltage



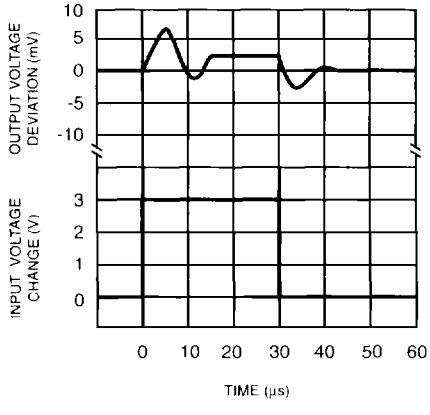

### Standby Output Voltage vs. Input Voltage




### Line Transient Response ($V_{OUT_1}$)

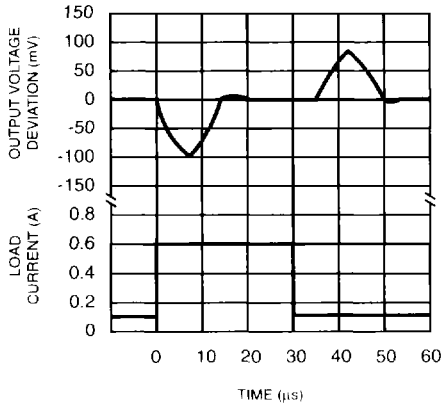



### Line Transient Response ($V_{OUT_2}$)

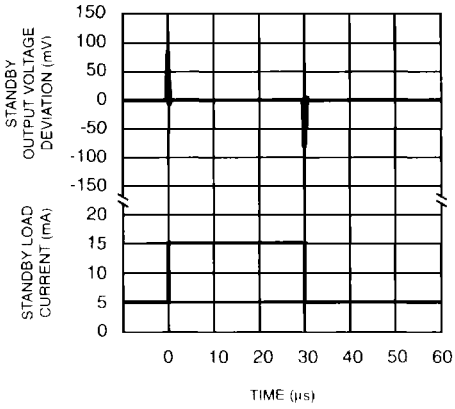


## Typical Performance Characteristics

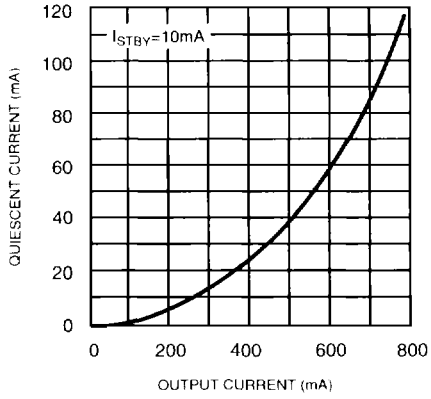
### Load Transient Response ($V_{OUT_1}$)



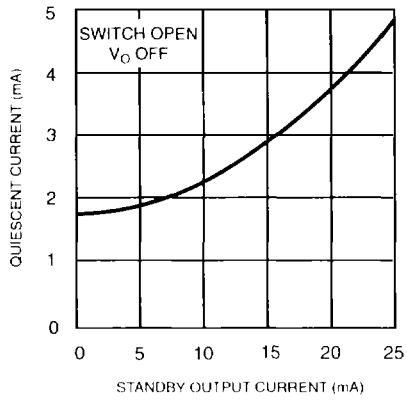

### Load Transient Response ($V_{OUT_2}$)



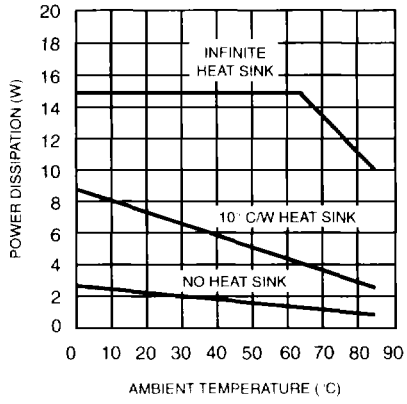

### Quiescent Current vs. Output Current




### Quiescent Current vs. Standby Output Current




### Maximum Power Dissipation (TO-220)



## Definition of Terms

**Dropout Voltage:** The input-output voltage differential at which the circuit ceases to regulate against further reduction in input voltage. Measured when the output voltage has dropped 100mV from the nominal value obtained at 14V input, dropout voltage is dependent upon load current and junction temperature.

**Input Voltage:** The DC voltage applied to the input terminals with respect to ground.

**Input Output Differential:** The voltage difference between the unregulated input voltage and the regulated output voltage for which the regulator will operate.

**Line Regulation:** The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

**Load Regulation:** The change in output voltage for a change in load current at constant chip temperature.

**Long Term Stability:** Output voltage stability under accelerated life-test conditions after 1000 hours with maximum rated voltage and junction temperature.

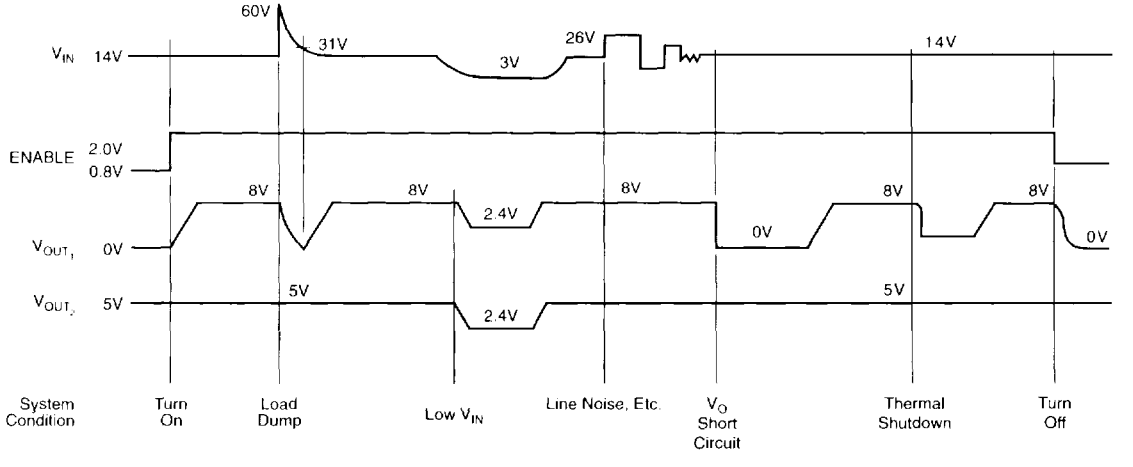
**Output Noise Voltage:** The rms AC voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

**Quiescent Current:** The part of the positive input current that does not contribute to the positive load current. i.e., the regulator ground lead current.

**Ripple Rejection:** The ratio of the peak-to-peak input ripple voltage to the peak-to-peak output ripple voltage.

**Temperature Stability of $V_{OUT}$:** The percentage change in output voltage for a thermal variation from room temperature to either temperature extreme.

## Typical Circuit Waveform



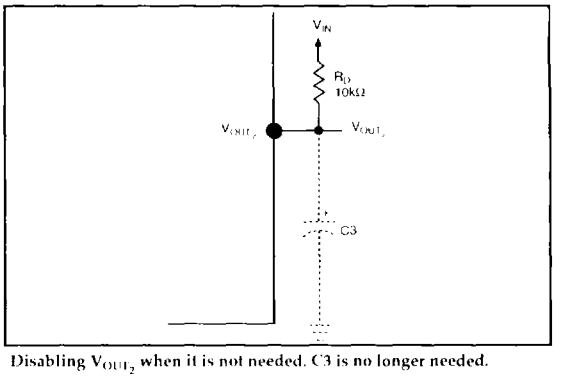

## Circuit Description

### Standby Output ($V_{OUT_2}$)

The CS-8165 is equipped with two outputs. The second output is intended for use in systems requiring standby memory circuits. While the high current regulator output ($V_{OUT_1}$) can be controlled with the ENABLE pin described below, the standby output remains on under all conditions as long as sufficient input voltage is applied to the IC. Thus, memory and other circuits powered by this output remain unaffected by positive line transients, thermal shutdown, etc.

The standby regulator circuit ($V_{OUT_2}$) is designed so that the quiescent current to the IC is very low (<2mA) when primary regulator output ($V_{OUT_1}$) is off.

In applications where the standby output is not needed, it may be disabled by connecting a resistor from the standby




**Disabling $V_{OUT_2}$ when it is not needed, C3 is no longer needed.**

## Cricuit Description: continued

output to the supply voltage. This eliminates the need for a capacitor on the output to prevent unwanted oscillations. The value of the resistor depends upon the minimum input voltage expected for a given system. Since the standby output is shunted with an internal 6.0V Zener, the current through the external resistor should be sufficient to bias $V_{OUT_2}$ up to this point. Approximately 60µA of current is required. For most applications a 10kΩ external resistor is sufficient.

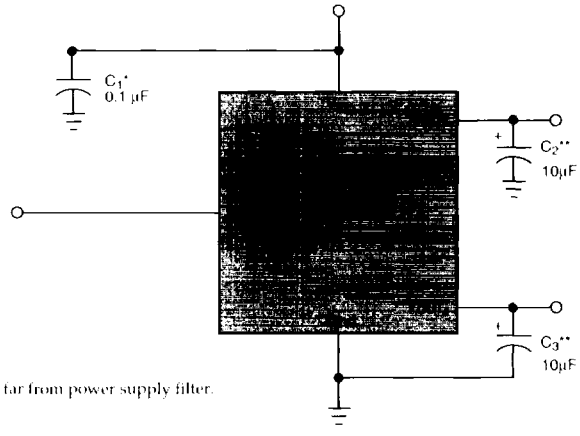
### High Current Output ($V_{OUT_1}$)

Unlike the standby regulated output, which must remain on whenever possible, the high current regulated output is fault protected against overvoltage and overt temperature conditions. If the input voltage rises above approximately 30V (e.g., load dump), this output will automatically shutdown. This protects the internal circuitry and enables the IC to survive higher voltage transients than would otherwise be expected. Thermal shutdown is effective against die overheating since the high current output is the dominant source of power dissipation in the IC.

### ENABLE

The ENABLE function controls $V_{OUT_1}$ When ENABLE is high (5V), $V_{OUT_1}$ is on. When ENABLE is low, $V_{OUT_1}$ is off.

## Application Circuit




NOTES:

* $C_1$ required if regulator is located far from power supply filter.

** $C_2$, $C_3$ required for stability.

## Application Notes

### Stability Considerations

The capacitor value and type should be based on cost, availability, size and temperature constraints. A tantalum or aluminum electrolytic capacitor is best, since a film or ceramic capacitor with almost zero ESR, can cause instability. The aluminum electrolytic capacitor is the cheapest solution, but, if the circuit operates at low temperatures (-25°C to -40°C), both the value and ESR of the capacitor will vary considerably. The capacitor manufacturers data sheet usually provide this information.

The value for the output capacitors C2 and C3 shown in the test and applications circuit should work for most applications, however it is not necessarily the cheapest or best solution.

To determine acceptable values for C2 and C3 for a particular application, start with a tantalum capacitor of the recommended value and work towards a less expensive alternative part for each output.

**Step 1:** Place the completed circuit with the tantalum capacitors of the recommended values in an environmental chamber at the lowest specified operating temperature and monitor the outputs on the oscilloscope. A decade box connected in series with capacitor $C_2$ will simulate the higher ESR of an aluminum capacitor. (Leave the decade box outside the chamber, the small resistance added by the longer leads is negligible)

**Step 2:** With the input voltage at its maximum value, increase the load current slowly from zero to full load on the output under observation. Look for any oscillations on the output. If no oscillations are observed, the capacitor is large enough to ensure a stable design under steady state conditions.

**Step 3:** Increase the ESR of the capacitor from zero using the decade box and vary the load current until oscillations appear. Record the values of load current and ESR that cause the greatest oscillation. This represents the worst case load conditions for the output at low temperature.

**Step 4:** Maintain the worst case load conditions set in step 3 and vary the input voltage until the oscillations increase. This point represents the worst case input voltage conditions.

**Step 5:** If the capacitor is adequate, repeat steps 3 and 4 with the next smaller valued capacitor. (A smaller capacitor will usually cost less and occupy less board space.) If the capacitor oscillates within the range of expected operating conditions, repeat steps 3 and 4 with the next larger standard capacitor value.

**Step 6:** Test the load transient response by switching in various loads at several frequencies to simulate its real work environment. Vary the ESR to reduce ringing.

**Step 7:** Remove the unit from the environmental chamber and heat the IC with a heat gun. Vary the load current as instructed in step 5 to test for any oscillations.

Once the minimum capacitor value with the maximum ESR is found for each output, a safety factor should be added to allow for the tolerance of the capacitor and any variations in regulator performance. Most good quality aluminum electrolytic capacitors have a tolerance of +/- 20% so the minimum value found should be increased by at least 50% to allow for this tolerance plus the variation which will occur at low temperatures. The ESR of the capacitors should be less than 50% of the maximum allowable ESR found in step 3 above.

Repeat steps 1 through 7 with the capacitor on the other output, $C_2$.

## Calculating Power Dissipation in a Dual Output Linear Regulator

The maximum power dissipation for a dual output regulator (Figure 1) is

$$P_{D(max)} = \{V_{IN(max)} - V_{OUT1(min)}\}I_{OUT1(max)} + \{V_{IN(max)} - V_{OUT2(min)}\}I_{OUT2(max)} + V_{IN(max)}IQ \quad (1)$$

Where

$V_{IN(max)}$ is the maximum input voltage,

$V_{OUT1(min)}$ is the minimum output voltage from $V_{OUT1}$,

$V_{OUT2(min)}$ is the minimum output voltage from $V_{OUT2}$,

$I_{OUT1(max)}$ is the maximum output current, for the application

$I_{OUT2(max)}$ is the maximum output current, for the application

$I_Q$ is the quiescent current the regulator consumes at $I_{OUT(max)}$.

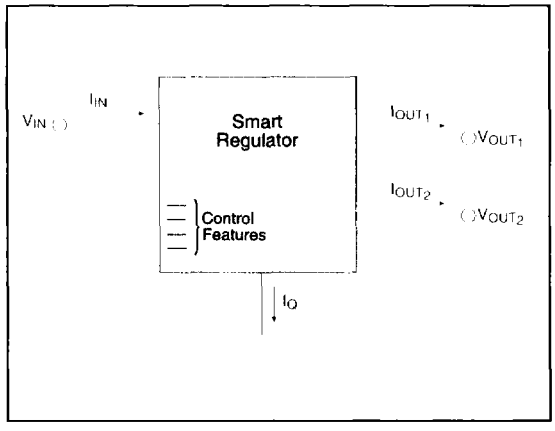



**Figure 1: Dual output regulator with key performance parameters labeled.**

Once the value of $P_{D(max)}$ is known, the maximum permissible value of $R\Theta_{JA}$ can be calculated:

$$R\Theta_{JA} = \frac{150°C - T_A}{P_D} \quad (2)$$

The value of $R\Theta_{JA}$ can then be compared with those in the package section of the data sheet. Those packages with $R\Theta_{JA}$'s less than the calculated value in equation 2 will keep the die temperature below 150°C.

In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required.

## Heat Sinks

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $R\Theta_{JA}$.

$$R\Theta_{JA} = R\Theta_{JC} + R\Theta_{CS} + R\Theta_{SA} \quad (3)$$

where

$R\Theta_{JC}$ = the junction–to–case thermal resistance,
$R\Theta_{CS}$ = the case–to–heatsink thermal resistance, and
$R\Theta_{SA}$ = the heatsink–to–ambient thermal resistance.

$R\Theta_{JC}$ appears in the package section of the data sheet. Like $R\Theta_{JA}$, it too is a function of package type. $R\Theta_{CS}$ and $R\Theta_{SA}$ are functions of the package type, heatsink and the interface between them. These values appear in heat sink data sheets of heat sink manufacturers.

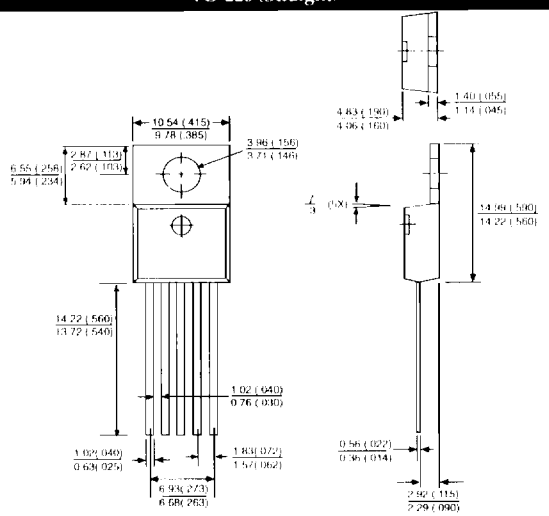
## Package Specification

### PACKAGE DIMENSIONS IN mm(INCHES)

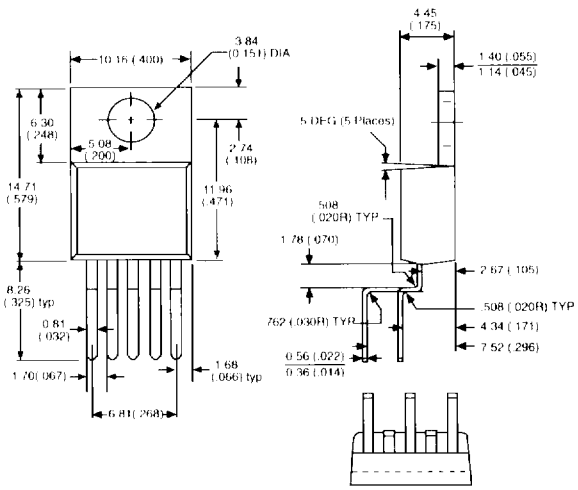
### PACKAGE THERMAL DATA

| Thermal Data | | TO-220 | |
|---|---|---|---|
| $R\Theta_{JC}$ | typ | 3.5 | °C/W |
| $R\Theta_{JA}$ | typ | 50 | °C/W |

### TO-220 (Straight)




### TO-220 (Vertical)




### Ordering Information

| Part Number | Description |
|---|---|
| CS-8165T5 | 5 Lead TO-220 Straight |
| CS-8165TV5 | 5 Lead TO-220 Vertical |
| CS-8165TH5 | 5 Lead TO-220 Horizontal |

### Preliminary

This product is in the preproduction stages of the design process. The data sheet contains preliminary data. CSC reserves the right to make changes to the specifications without notice. Please contact CSC for the latest available information.