FAIRCHILD
A Schlumberger Company

93422
93422F

93422
256 x 4-Bit Static Random Access Memory

Memory and High Speed Logic

Description

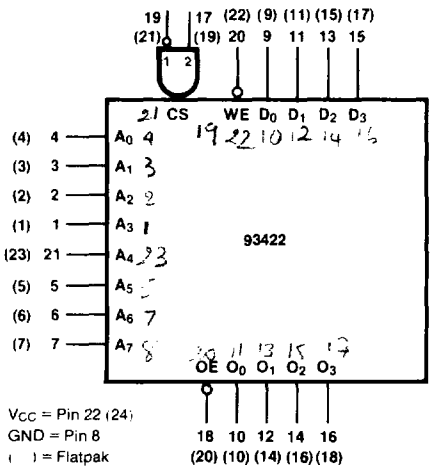
The 93422 is a 1024-bit read/write Random Access Memory (RAM), organized 256 words by four bits. It is designed for high speed cache, control and buffer storage applications. The 93422 is available in two speeds, "standard" speed and an "A" grade. The device includes full on-chip decoding, separate Data inputs and non-inverting Data outputs, as well as two Chip Select lines.

- **Commercial Address Access Time**
  - **93422 — 45 ns Max**
  - **93422A — 35 ns Max**
- **Military Address Access Time**
  - **93422 — 60 ns Max**
  - **93422A — 45 ns Max**
- **Fully TTL Compatible**
- **Features Three State Outputs**
- **Power Dissipation — 0.46 mW/Bit Typ**
- **Power Dissipation Decreases with Increasing Temperature**

Pin Names

A_0-A_7	Address Inputs
D_0-D_3	Data Inputs
$\overline{CS}_1$	Chip Select Input (Active LOW)
CS_2	Chip Select Input (Active HIGH)
$\overline{WE}$	Write Enable Input (Active LOW)
$\overline{OE}$	Output Enable Input (Active LOW)
O_0-O_3	Data Outputs

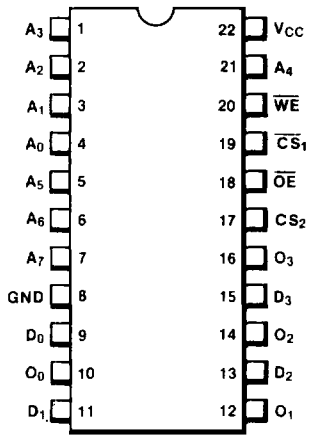
Logic Symbol



VCC = Pin 22 (24)
GND = Pin 8
( ) = Flatpak

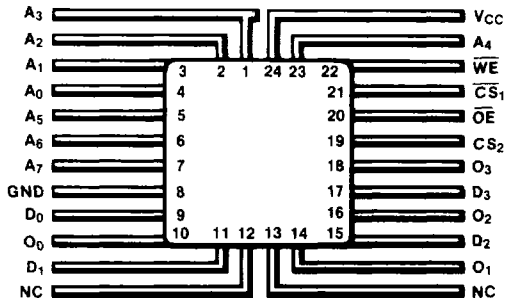
Connection Diagrams

22-Pin DIP (Top View)



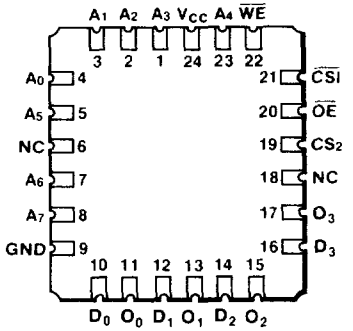
93422

24-Pin Flatpak (Top View)



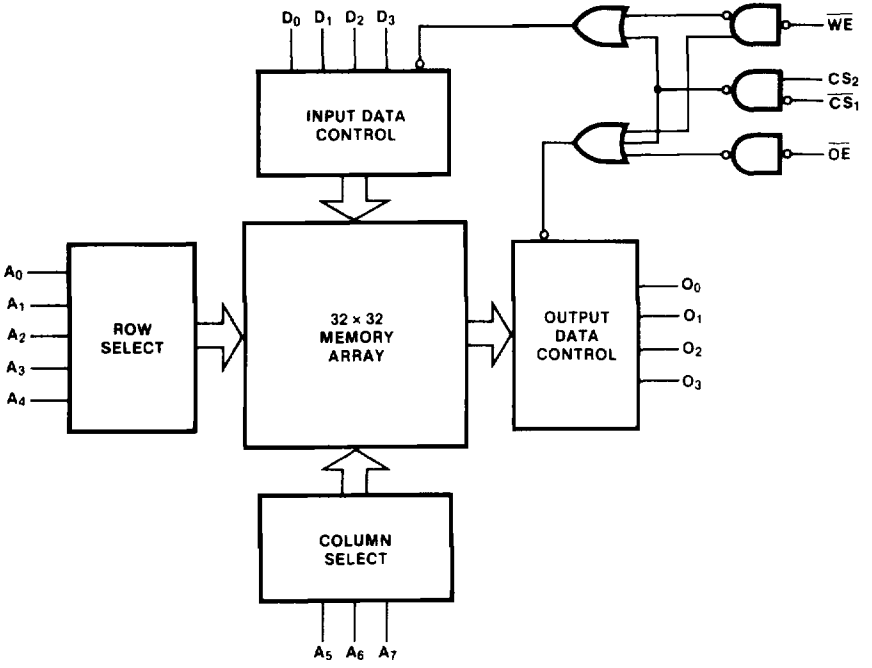
93422F

24-Pin Leadless Chip Carrier (Top View)



93422 LCC

Logic Diagram



Functional Description

The 93422 is a fully decoded 1024-bit Random Access Memory organized 256 words by four bits. Word selection is achieved by means of an 8-bit address, A_0 through A_7.

Two Chip Select inputs, inverting and non-inverting, are provided for logic flexibility. For larger memories, the fast chip select access time permits the decoding of the chip selects from the address without increasing address access time.

The read and write operations are controlled by the state of the active LOW Write Enable ($\overline{WE}$) input. When $\overline{WE}$ is held LOW and the chip is selected, the data at D_0–D_3 is written into the addressed location. Since the write function is level-triggered, data must be held stable for at least $t_{WSD(min)}$ plus $t_{W(min)}$ plus $t_{WHD(min)}$ to insure a valid write. To read, $\overline{WE}$ is held HIGH and the chip selected. Non-inverted data is then presented at the outputs (O_0–O_3).

The 93422 has 3-state outputs which provide active pull-ups when enabled and high output impedance when disabled. This allows optimization of word expansion in bus organized systems.

Truth Table

Inputs				Outputs	
$\overline{OE}$	$\overline{CS_1}$	CS_2	$\overline{WE}$	3-State	Mode
X	H	X	X	HIGH Z	Not Selected
X	X	L	X	HIGH Z	Not Selected
L	L	H	H	D_{OUT}	READ
X	L	H	L	HIGH Z	WRITE
H	X	X	X	HIGH Z	Output Disabled

H = HIGH Voltage Level (2.4 V)
L = LOW Voltage Level (.5 V)
X = Don't Care (HIGH or LOW)
High Z = High-Impedance

DC Performance Characteristics: Over operating temperature ranges (Note 1)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition	
V_{OL}	Output LOW Voltage		0.3	0.45	V	V_{CC} = Min, I_{OL} = 8 mA	
V_{IH}	Input HIGH Voltage	2.1	1.6		V	Guaranteed Input HIGH Voltage for All Inputs [5]	
V_{IL}	Input LOW Voltage		1.5	0 8	V	Guaranteed Input LOW Voltage for All Inputs [5]	
V_{OH}	Output HIGH Voltage	2.4			V	V_{CC} = Min, I_{OH} = −5.2 mA	
I_{IL}	Input LOW Current		−150	−300	μA	V_{CC} = Max. V_{IN} = 0.4 V	
I_{IH}	Input HIGH Current		1.0	40	μA	V_{CC} = Max, V_{IN} = 4.5 V	
I_{IHB}	Input Breakdown Current			1.0	mA	V_{CC} = Max, V_{IN} = V_{CC}	
V_{IC}	Input Diode Clamp Voltage		−1.0	−1.5	V	V_{CC} = Max, I_{IN} = −10 mA	
I_{OZH} I_{OZL}	Output Current (HIGH Z)			50 −50	μA	V_{CC} = Max, V_{OUT} = 2.4 V V_{CC} = Max, V_{OUT} = 0.5 V	
I_{OS}	Output Current Short Circuit to Ground	−10		−70	mA	V_{CC} = Max, Note 3	
I_{CC}	Power Supply Current			120 130	mA	Commercial Military	V_{CC} = Max All Inputs GND All Outputs Open

Notes
1. Typical values are at V_{CC} = 5 0 V T_C = +25°C and maximum loading.
2. The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern
3. Short circuit to ground not to exceed one second.
4. t_W measured at t_{WSA} = Min. t_{WSA} measured at t_W = Min.
5. Static condition only

Commercial
AC Performance Characteristics: V_{CC} = 5.0 V ± 5%, GND = 0 V, T_C = 0° C to +75° C

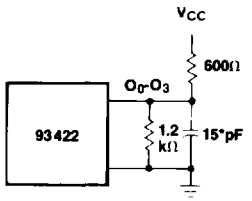
Symbol	Characteristic	A Min	A Max	Std Min	Std Max	Unit	Condition
	Read Timing						
t_{ACS}	Chip Select Access Time		30		30	ns	
t_{ZRCS}	Chip Select to HIGH Z		30		30	ns	
t_{AOS}	Output Enable Access Time		30		30	ns	*Figures 3a, 3b, 3c*
t_{ZROS}	Output Enable to HIGH Z		30		30	ns	
t_{AA}	Address Access Time[2]		35		45	ns	
	Write Timing						
t_W	Write Pulse Width to Guarantee Writing[4]	25		30		ns	
t_{WSD}	Data Setup Time Prior to Write	5		5		ns	
t_{WHD}	Data Hold Time after Write	5		5		ns	
t_{WSA}	Address Setup Time Prior to Write[4]	5		5		ns	*Figure 4*
t_{WHA}	Address Hold Time after Write	5		5		ns	
t_{WSCS}	Chip Select Setup Time Prior to Write	5		5		ns	
t_{WHCS}	Chip Select Hold Time after Write	5		5		ns	
t_{ZWS}	Write Enable to HIGH Z		35		35	ns	
t_{WR}	Write Recovery Time		35		40	ns	

Military
AC Performance Characteristics: V_{CC} = 5.0 V ± 10%, GND = 0 V, T_C = −55° C to +125° C

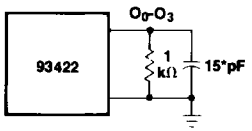
Symbol	Characteristic	A Min	A Max	Std Min	Std Max	Unit	Condition
	Read Timing						
t_{ACS}	Chip Select Access Time		35		45	ns	
t_{ZRCS}	Chip Select to HIGH Z		35		45	ns	
t_{AOS}	Output Enable Access Time		35		45	ns	*Figures 3a, 3b, 3c*
t_{ZROS}	Output Enable to HIGH Z		35		45	ns	
t_{AA}	Address Access Time[2]		45		60	ns	
	Write Timing						
t_W	Write Pulse Width to Guarantee Writing[4]	35		40		ns	
t_{WSD}	Data Setup Time Prior to Write	5		5		ns	
t_{WHD}	Data Hold Time after Write	5		5		ns	
t_{WSA}	Address Setup Time Prior to Write[4]	5		5		ns	*Figure 4*
t_{WHA}	Address Hold Time after Write	5		5		ns	
t_{WSCS}	Chip Select Setup Time Prior to Write	5		5		ns	
t_{WHCS}	Chip Select Hold Time after Write	5		5		ns	
t_{ZWS}	Write Enable to HIGH Z		40		45	ns	
t_{WR}	Write Recovery Time		40		50	ns	

Notes on preceding page

Fig. 1 AC Test Output Load



LOAD A



LOAD B

*Includes jig and probe capacitance

Note: Load A is used for all production testing.

Fig. 2 AC Test Input Levels

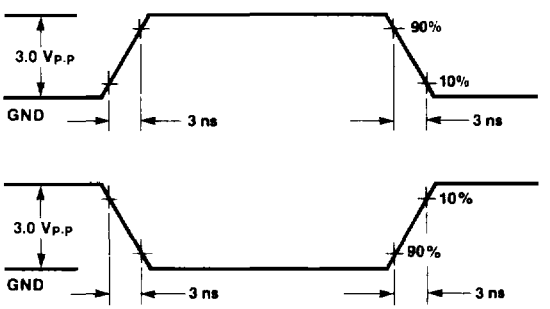
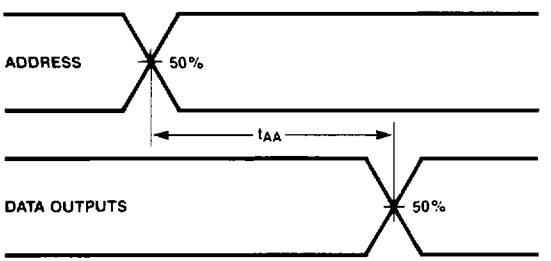
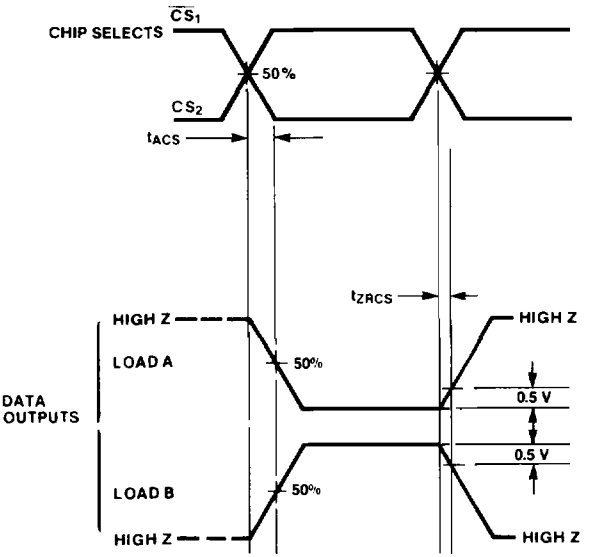


Fig. 3 Read Mode Timing

a Read Mode Propagation Delay from Address



3b Read Mode Propagation Delay from Chip Select



3c Read Mode Propagation Delay from Output Enable

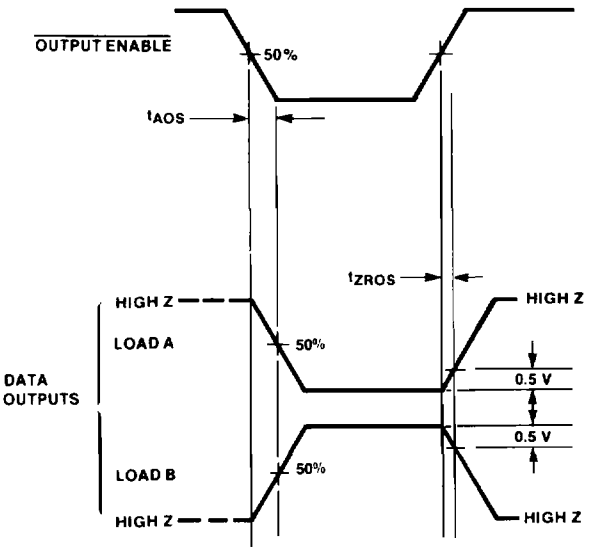


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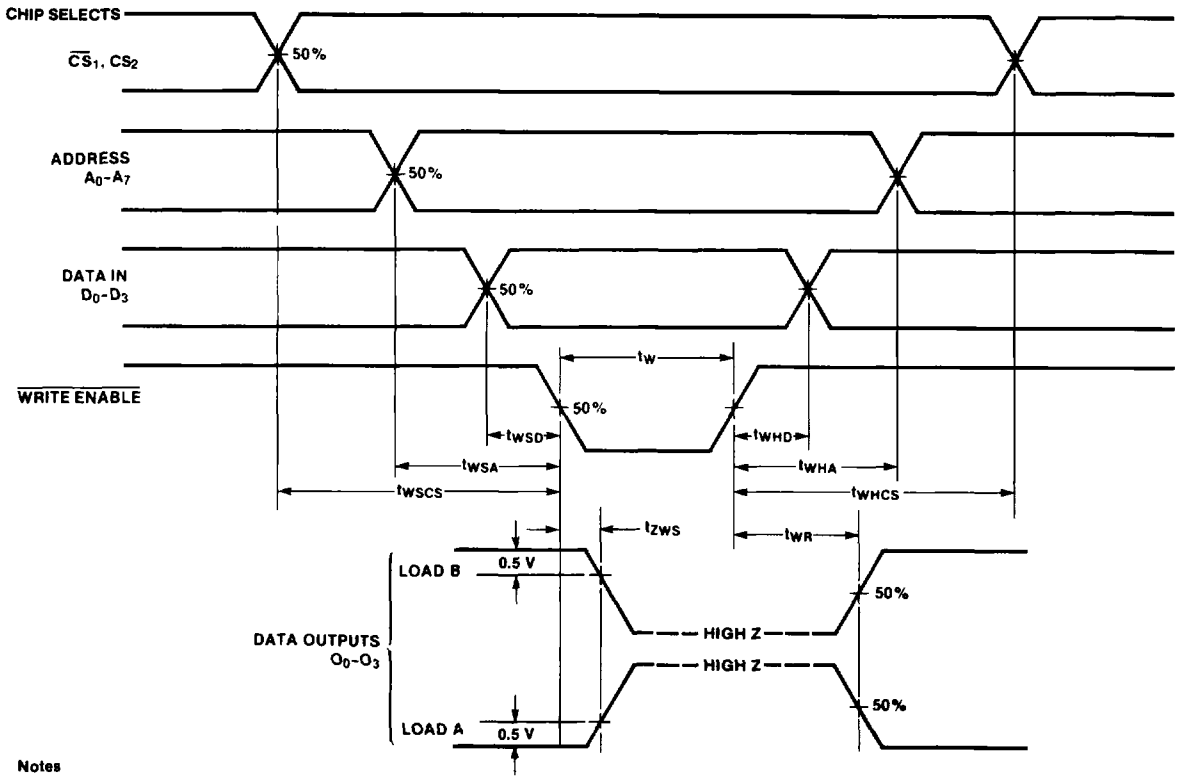
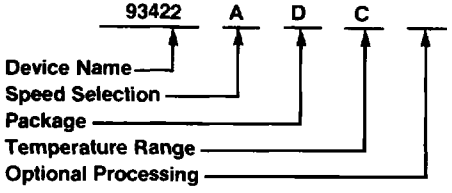
Fig. 4 Write Mode Timing



Notes

1. Timing Diagram represents one solution which results in an optimum cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.
2. Input voltage levels for worst case AC test are 3.0/0.0 V.

Ordering Information



Speed Selection
Blank = Standard Speed
A = 'A' Grade

Packages and Outlines (See Section 9)
D = Ceramic DIP
F = Flatpak
L = Leadless Chip Carrier
P = Plastic DIP

Temperature Range
C = 0°C to +75°C
M = −55°C to +125°C

Optional Processing
QB = Mil Std 883
Method 5004 and 5005, Level B
QR = Commercial Device with
160 Hour Burn In or Equivalent