Philips Semiconductors-Signetics

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Status	Product Specification
FAST Products	

FAST 74F2952, 74F2953 Transceivers

74F2952 Registered Transceiver, Non-Inverting (3-State)
74F2953 Registered Transceiver, Inverting (3-State)

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F2952	160MHz	105mA
74F2953	160MHz	105mA

FEATURES

- **8-bit Registered Transceivers**
- **Two 8-bit , back-to-back registers store data moving in both directions between two bidirectional busses**
- **Separate Clock, Clock Enable and 3-state Enable provided for each register**
- **'F2952 Non-Inverting 'F2953 Inverting**
- **AM2952/2953 functional equivalent**
- **A outputs sink 24mA and source 3mA**
- **B outputs sink 64mA and source 15mA**
- **300 mil wide 24-pin Slim DIP package**

DESCRIPTION

The 74F2952 and 74F2953 are 8-bit Registered Transceivers. Two 8-bit back to back registers store data flowing in both directions between two bi-directional busses. Data applied to the inputs is entered and stored on the rising edge of the Clock (CPXX) provided that the Clock Enable ($\overline{CEXX}$) is Low. The data is then present at the 3-state output buffers, but is only accessible when the Output Enable ($\overline{OEXX}$) is Low. Data flow from A inputs to B outputs is the same as for B inputs to A outputs.

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Plastic Slim DIP (300mil)	N74F2952N, N74F2953N
24-Pin Plastic SOL[1]	N74F2952D, N74F2953D
28-Pin Plastic PLCC	N74F2952A, N74F2953A

NOTE:
1.Thermal mounting techniques are recommended. See SMD Process Applications (page 17) for a discussion of thermal consideration for surface mounted devices.

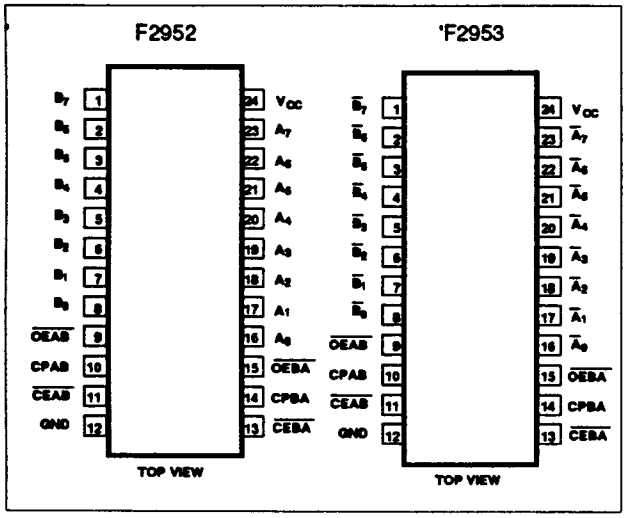
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0 - A_7	Port A, 3-state inputs	3.5/1.0	70µA/0.6mA
B_0 - B_7	Port B, 3-state inputs	3.5/1.0	70µA/0.6mA
CPAB,CPBA	Clock inputs	1.0/1.0	20µA/0.6mA
$\overline{CEAB}$,$\overline{CEBA}$	Clock Enable inputs	1.0/1.0	20µA/0.6mA
$\overline{OEAB}$,$\overline{OEBA}$	Output Enable inputs	1.0/1.0	20µA/0.6mA
A_0 - A_7	Port A, 3-state outputs	150/40	3.0mA/24mA
B_0 - B_7	Port B, 3-state outputs	750/106.7	15mA/64mA

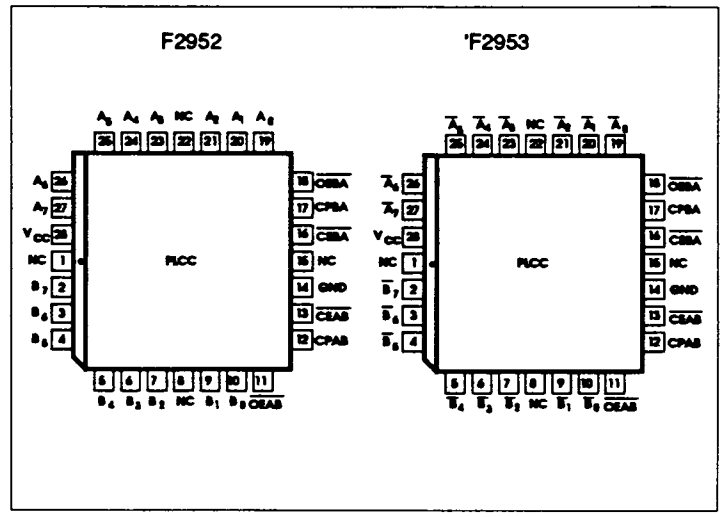
NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

Registered Transceivers | FAST 74F2952, 74F2953

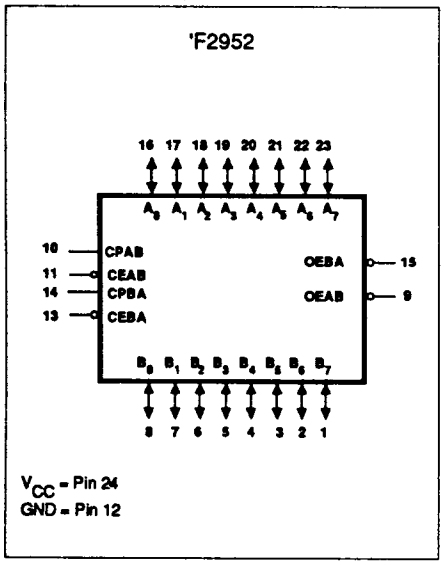
PIN CONFIGURATION DIP



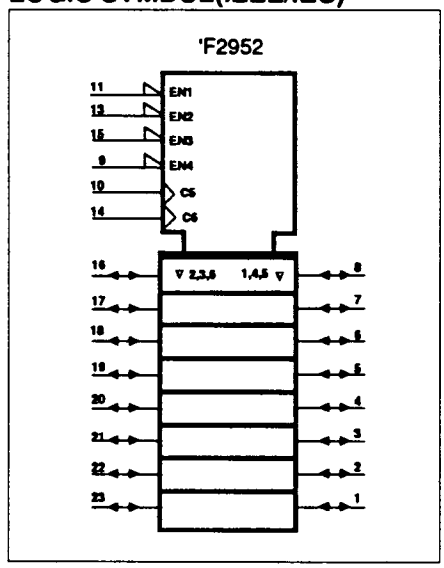
PIN CONFIGURATION PLCC



LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



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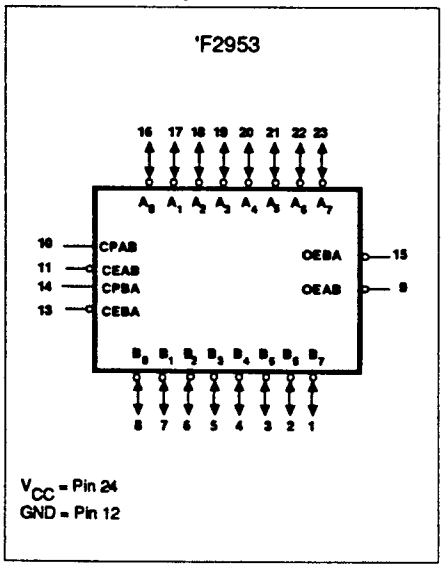

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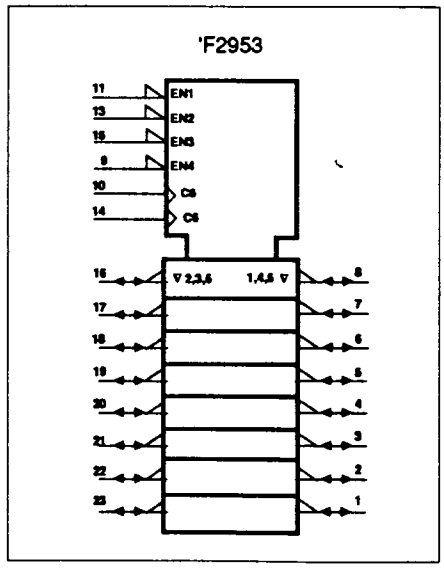
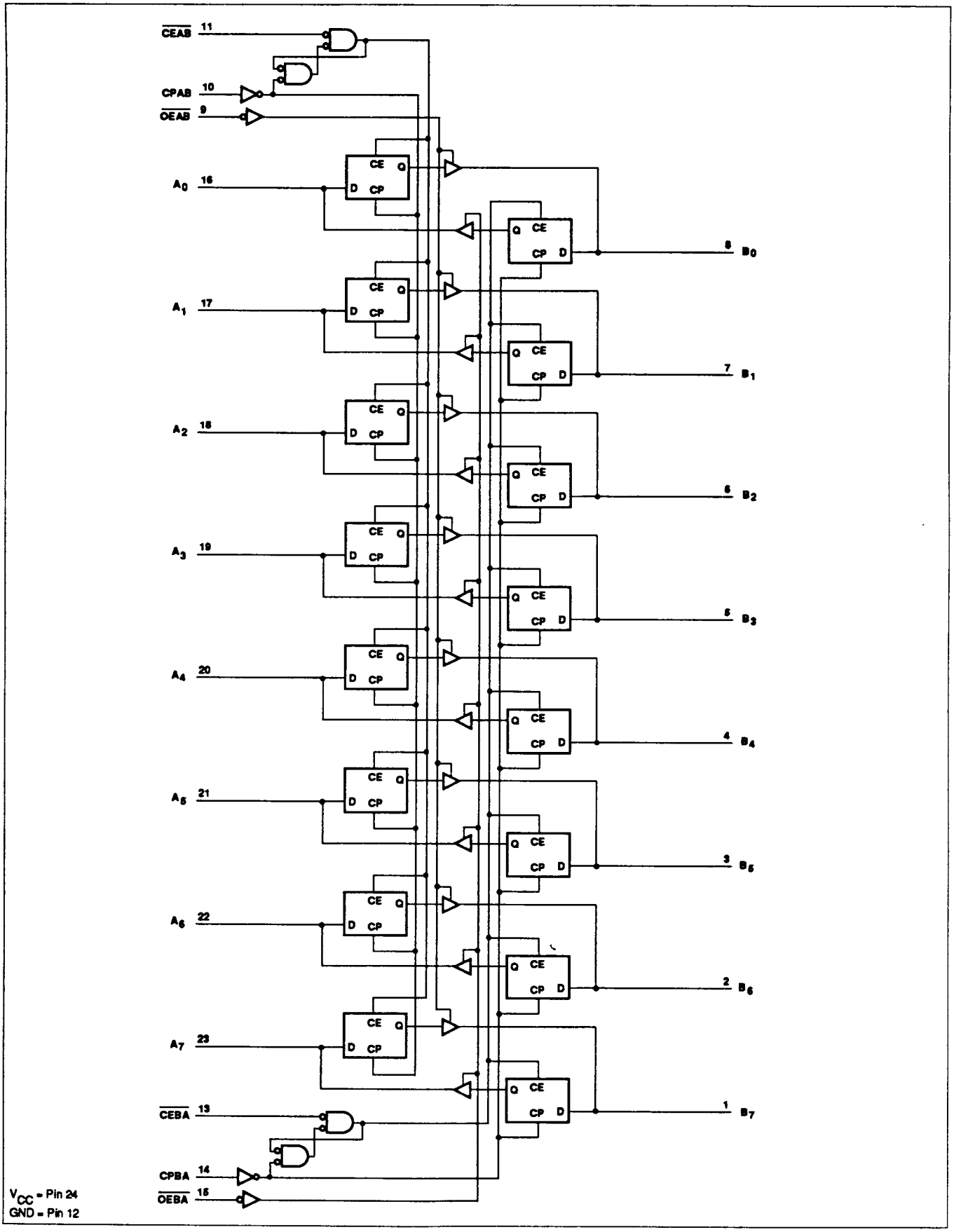
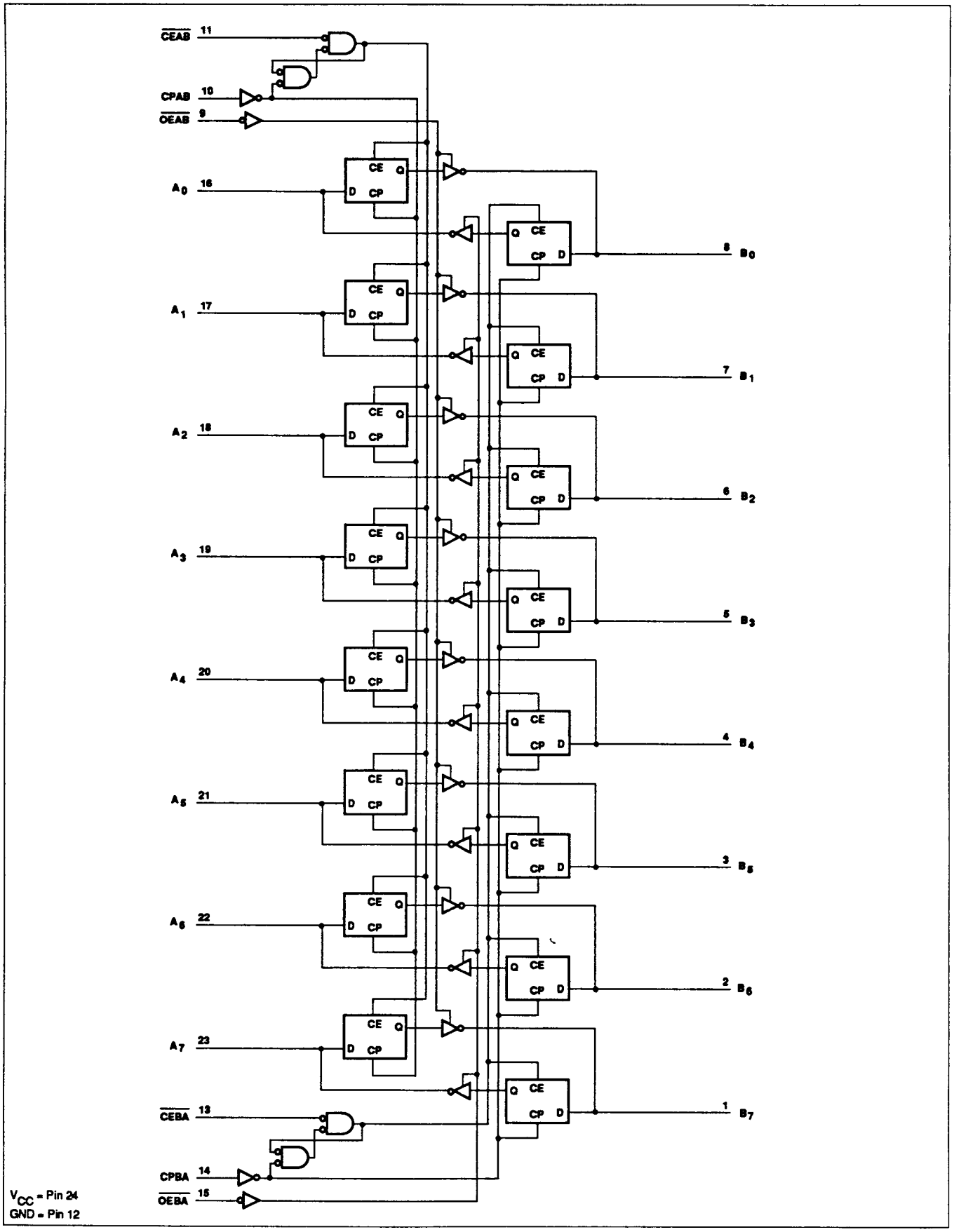


LOGIC DIAGRAM for 'F2952



LOGIC DIAGRAM for 'F2953



FUNCTION TABLE for Register A_n or B_n

INPUTS			INTERNAL	OPERATING MODE
A_n or B_n	CPXX	$\overline{CEXX}$	Q	
X	X	H	NC	Hold data
L	↑	L	L	Load data
H	↑	L	H	

H= High voltage level
L= Low voltage level
↑ =Low-to-High transition
X=Don't care
XX=AB or BA
NC=No change

FUNCTION TABLE for Output Enable

INPUTS	INTERNAL	A_n or B_n OUTPUTS		OPERATING MODE
$\overline{OEXX}$	Q	'F2952	'F2953	
H	X	Z	Z	Disable outputs
L	L	L	H	Enable outputs
L	H	H	L	

H= High voltage level
L= Low voltage level
X=Don't care
XX=AB or BA
Z =High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	A_0-A_7	48	mA
		B_0-B_7	128	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	A_0-A_7			-3	mA
		B_0-B_7			-15	mA
I_{OL}	Low-level output current	A_0-A_7			24	mA
		B_0-B_7			64	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage	A_0-A_7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}=-3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.3		V
		B_0-B_7		I_{OH}=-15mA	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage	A_0-A_7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}=24mA	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
		B_0-B_7		I_{OL}=48mA	±10%V_{CC}		0.38	0.55	V
				I_{OL}=64mA	±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	$\overline{CPAB}$, CPBA, $\overline{OEAB}$ $\overline{OEBA}$,$\overline{CEAB}$, $\overline{CEBA}$	V_{CC} = 5.5V, V_I = 7.0V					100	µA
		A_0-A_7, B_0-B_7	V_{CC} = 5.5V, V_I = 5.5V					1	mA
I_{IH}	High-level input current	$\overline{CPAB}$, CPBA, $\overline{OEAB}$, $\overline{OEBA}$, $\overline{CEAB}$, $\overline{CEBA}$	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					-0.6	mA
I_{IH}+I_{OZH}	Off-state output current High-level voltage applied	A_0-A_7, B_0-B_7	V_{CC} = MAX, V_O= 2.7V					70	µA
I_{IL}+I_{OZL}	Off-state output current Low-level voltage applied	A_0-A_7, B_0-B_7	V_{CC} = MAX, V_O = 0.5V					-600	µA
I_{OS}	Short-circuit output current[3]	A_0-A_7	V_{CC} = MAX, V_O=0.00V			-60		-150	mA
		B_0-B_7				-100		-225	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				90	140	mA
		I_{CCL}					120	175	mA
		I_{CCZ}					105	155	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

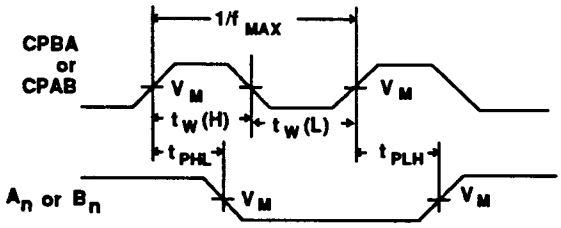
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	145	160		135		MHz
t_{PLH} t_{PHL}	Propagation delay CPBA or CPAB to A_n or B_n	Waveform 1	3.0 3.5	5.0 6.0	7.5 8.5	2.5 3.5	8.0 9.0	ns
t_{PZH} t_{PZH}	Output Enable time $\overline{OEBA}$ or $\overline{OEAB}$ to A_n or B_n	Waveform 3 Waveform 4	2.0 3.5	4.5 6.0	7.0 9.5	2.0 3.0	8.0 10.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OEBA}$ or $\overline{OEAB}$ to A_n or B_n	Waveform 3 Waveform 4	2.0 1.5	4.0 3.5	8.0 6.5	1.5 1.0	9.0 7.0	ns

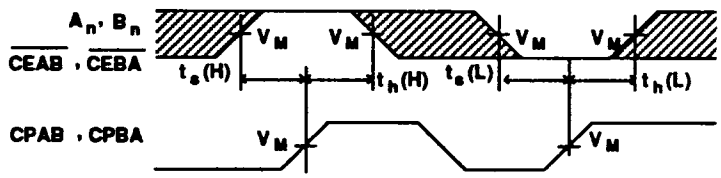
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low A_n or B_n to CPAB or CPBA	'F2952	Waveform 2	4.5 3.5			5.0 4.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low A_n or B_n to CPAB or CPBA	'F2953	Waveform 2	4.0 3.5			4.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low A_n or B_n to CPAB or CPBA		Waveform 2	0.0 0.0			0.0 0.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{CEAB}$,$\overline{CEBA}$ to CPAB , CPBA		Waveform 2	0.0 4.0			0.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{CEAB}$,$\overline{CEBA}$ to CPAB , CPBA		Waveform 2	2.5 2.5			2.5 3.0		ns
$t_w(H)$ $t_w(L)$	CPAB or CPBA Pulse width, High or Low		Waveform 1	3.0 3.5			3.0 3.5		ns

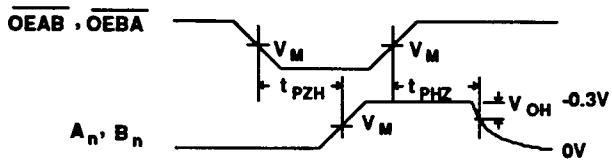
AC WAVEFORMS



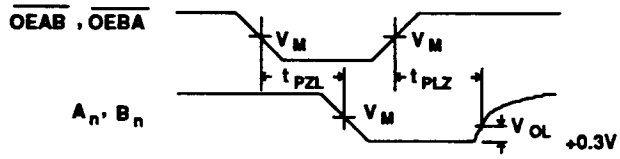
Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency



Waveform 2. Data Setup And Hold Times



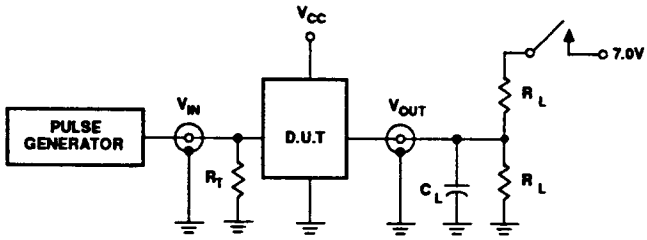
Waveform 3. 3-State Output Enable Time To High Level And Output Disable Time From High Level



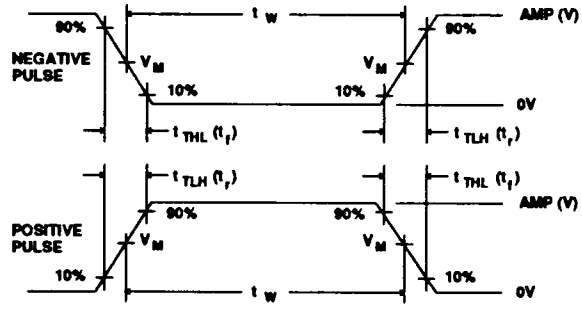
Waveform 4. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.
The shaded area indicate when the input is permitted to change for predictable output

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns