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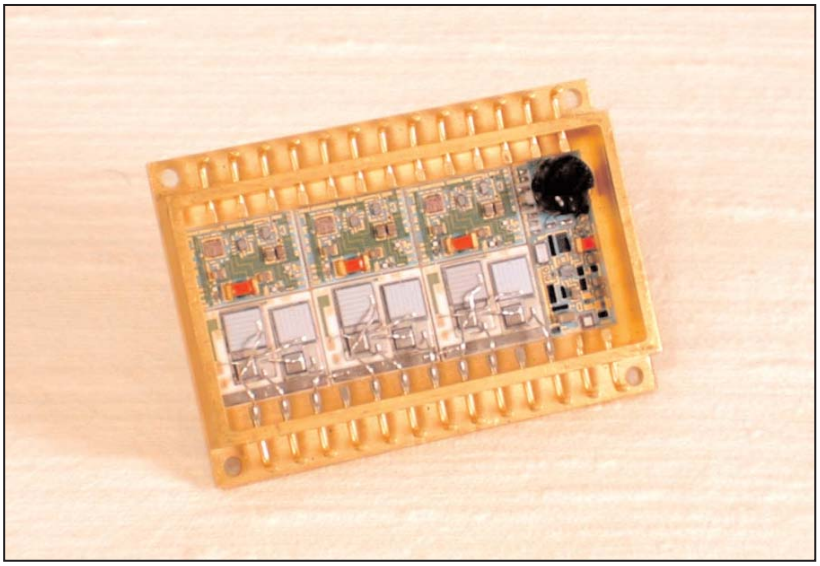
PWR-82331 AND PWR-82333

SMART POWER 3-PHASE MOTOR DRIVES



FEATURES

- Small Size (3.0" x 2.1" x 0.39")
- +200 V and +500 V Capability
- 30 A Current Capability
- High-Efficiency MOSFET or IGBT Drive Stage
- Direct Drive from Commutation Logic
- Six Step Trapezoidal or Sinusoidal Drive
- Four Quadrant Operation
- 0.85° C/W θ_{JC} Max
- Military Processing Available

DESCRIPTION

The PWR-82331 and PWR-82333 are 30 A, 3-phase motor drive hybrids. The PWR-82331 has a +200 V rating and uses MOSFETs in the output stage while the PWR-82333 has a +500 V rating and an IGBT output stage. Both types have individual fast recovery diodes internally connected across the output drive transistors to clamp inductive flyback. These Smart Power Motor Drives have CMOS Schmitt Trigger inputs for high noise immunity. High- and low-side input logic signals are XOR'd in each phase to prevent simultaneous turn-on of in-line transistors, thus eliminating a shoot through condition. The internal logic controls the high- and low-side gate drives for each phase and can operate from +5 to +15 V logic levels. The internal power supply provides a constant voltage source to the floating high-side gate drives, and constant output performance for switching frequencies from dc to 50 kHz.

APPLICATIONS

These hybrids are an excellent choice for high-performance, high-reliability motor drives for Military and Aerospace servo-amps and speed controls. Among the many applications are robotics; electro-mechanical valve assemblies; actuator systems for flight control surfaces on military and commercial aircraft; antenna and radar positioning; fan and blower motors for environmental conditioning; thrust and vector position control of mini-subs, drones, and RPV's; compressor motors for cryogenic coolers; and high power inverters.

The PWR-82331/82333 hybrids are ideal for harsh military environments where shock, vibration, and temperature extremes are evident, such as missile applications where fin actuator systems control missile direction.

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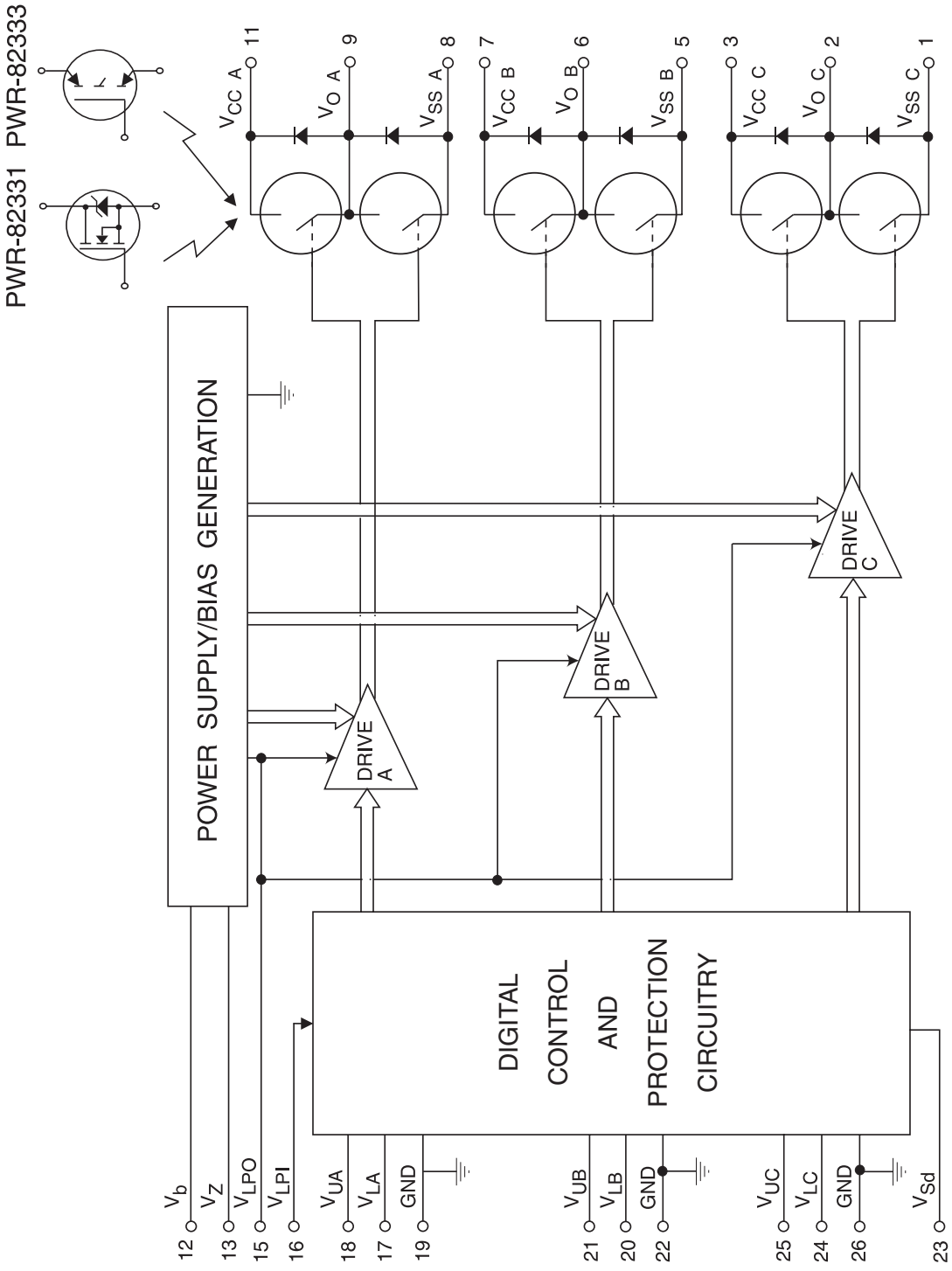


FIGURE 1. PWR-82331/82333 BLOCK DIAGRAM

TABLE 1. PWR-82331 AND PWR-82333 ABSOLUTE MAXIMUM RATINGS (TC = +25°C UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	PWR-82331	PWR-82333	UNITS
SUPPLY VOLTAGE	V_{CC}	200	500	V
BIAS VOLTAGE	V_B	50	50	V
LOGIC POWER-IN VOLTAGE	V_{LPI}	18	18	V
INPUT LOGIC VOLTAGE	V_U, V_L, V_{Sd}	V_{LPI} + 0.5	V_{LPI} + 0.5	V
OUTPUT CURRENT Continuous Pulsed	 I_O I_{OP}	 30 50	 30 50	 A A
OPERATING FREQUENCY	fo	50	25	kHz
CASE OPERATING TEMPERATURE	T_C	-55 to +125	-55 to +125	°C
CASE STORAGE TEMPERATURE RANGE	T_{CS}	-55 to +150	-55 to +150	°C
GND - VSS DIFFERENTIAL VOLTAGE		± 3	± 3	Vdc-peak

TABLE 2. PWR-82331 AND PWR-82333 SPECIFICATIONS (TC = +25°C UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	TEST CONDITIONS	PWR-82331			PWR-82333			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
OUTPUT									
Output Current Continuous (see FIG.'s 15 & 19)	I_O				30			30	A
Supply Voltage	V_{CC}	see note 1		28	140		270	350	V
Output On-Resistance (each FET)(see FIG. 14A)	R_{ON}	I_O=30 A			0.1				ohm
Output Voltage drop (each IGBT) (see FIG. 14B)	$V_{CE(SAT)}$	I_O=30 A						3.8	V
Instant Forward Voltage (flyback diode) (see FIG.'s 13A/B	V_F	I_{OP}=30 A, see note 2			1.15			1.70	V
Reverse Recovery Time (flyback diode)	trr	If=1 A, Ir=1 A			50			50	nsec
Reverse Leakage Current at TC = +25°C	Ir	see note 3			10			10	µA
Reverse Leakage Current at TC = +125°C	Ir	see note 3			1			1	mA
BIAS SUPPLY									
Input Bias Voltage (T_C= -55°C to +125°C)	Vb		14		50	14		50	V
Quiescent Bias Current (see note 4)(see FIG. 16)	Ibq	Vb = 28 V		32			32		mA
Bias Current (T_C= -55°C to +125°C)(see FIG.'s 17 & 18)	Ib	Vb=28 V, see note 5	35		65	35		65	mA
In-rush Current (T_C= -55°C to +125°C)	Iir	Vb = 28 V			1.4			1.4	A
Logic power Input Current	I_{LPI}	see note 6			2			2	mA
INPUT SIGNALS (SEE FIG. 7)		**Pin Connections**							
Positive Trigger Threshold Voltage	V_P	Pin 15 &16 connect.			12.9			12.9	V
Negative Trigger Threshold Voltage	V_N	Pin 15 &16 connect.	2.1			2.1			V
Hysteresis Voltage	V_H	Pin 15 &16 connect	1.6		10.8	1.6		10.8	V
Positive Trigger Threshold Voltage	V_P	See note 6			4.3			4.3	V
Negative Trigger Threshold Voltage	V_N	See note 6	0.9			0.9			V
Hysteresis Voltage	V_H	See note 6	0.3		3.6	0.3		3.6	V
SWITCHING CHARACTERISTICS (SEE FIG. 2)		**Test 1 Conditions**							
Upper Drive:		Pin 15 &16 connect.							
Turn-on propagation delay	td(on)	+15 V Logic			840			810	nsec
Turn-off propagation delay	td(off)	Io=30 A peak			1020			860	nsec
Shut-down propagation delay	t_{Sd}				800			810	nsec
Turn-on Rise Time	tr	PWR-82331,			125			100	nsec
Turn-off Fall Time	tf	V_{CC} = 140 V			125			150	nsec
Lower Drive:		PWR-82333,							
Turn-on propagation delay	td(on)	V_{CC} = 270 V			850			800	nsec
Turn-off propagation delay	td(off)				1000			870	nsec
Shut-down propagation delay	t_{Sd}				800			770	nsec
Turn-on Rise Time	tr				125			100	nsec
Turn-off Fall Time	tf				125			150	nsec
SWITCHING CHARACTERISTICS (SEE FIG. 2)		**Test 2 Conditions**							
Upper Drive:		see note 6							
Turn-on propagation delay	td(on)	+5 V, Io=30 A peak			1090			1050	nsec
Turn-off propagation delay	td(off)	PWR-82331,			1315			1150	nsec
Shut-down propagation delay	t_{Sd}	Vcc = 140 V			1100			850	nsec
Turn-on Rise Time	tr				125			100	nsec
Turn-off Fall Time	tf	PWR-82333,			125			150	nsec
		V_{CC} = 270 V							

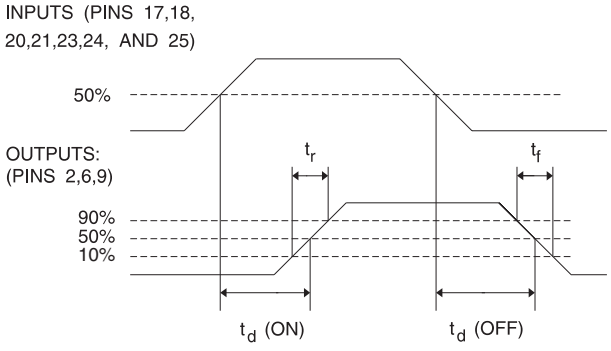
TABLE 2. PWR-82331 AND PWR-82333 SPECIFICATIONS (CONT'D) (TC = +25°C UNLESS OTHERWISE SPECIFIED)									
PARAMETER	SYMBOL	TEST CONDITIONS	PWR-82331			PWR-82333			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
SWITCHING CHARACTERISTICS (CONT'D)		**Test 2 Conditions**							
Lower Drive:		see note 6							
Turn-on Propagation delay	td(on)	+5 V, Io=30 A peak			1125			1050	nsec
Turn-off Propagation delay	td(off)	PWR-82331,			1290			1150	nsec
Shut-down propagation delay (see FIG. 10)	tsd	Vcc=140 V			1100			850	nsec
Turn-on Rise Time	tr				125			100	nsec
Turn-off Fall Time	tf	PWR-82333, 270 V			125			150	nsec
DEAD TIME	tdt		400			500			nsec
MINIMUM PULSE WIDTH	tpw		150			150			nsec
THERMAL		each transistor							
Maximum Thermal Resistance	θjc				0.85			0.85	°C/W
Maximum Lead Soldering Temperature (Note 7)	Ts				250			250	°C
Junction Temperature Range	Tj		-55		150	-55		150	°C
Case Operating Temperature	Tco		-55		125	-55		125	°C
Case Storage Temperature	Tcs		-55		150	-55		150	°C
WEIGHT					4.9 (140)			4.9 (140)	oz (g)

Notes:
1. For Hi-Rel applications, derating per MIL-S-19500 should be observed. (Derate Vcc to 70%.)
2. Pulse width ≤ 300 ms, duty cycle ≤ 2%.
3. For PWR-82331, Vcc = 140 V, VU, VL = Logic '0' and for PWR-82333, Vcc = 350 V, VU, VL = Logic '0.'
4. VU, VL = Logic '0' on pins 17, 18, 20, 21, 24 and 25.
5. For PWR-82331, fo = 30 kHz and for PWR-82333, fo = 10 kHz.
6. Pin 16 connected to external +5 V supply.
7. Solder 1/8" from case for 5 seconds maximum.

INTRODUCTION

The 3-phase PWR-82331 and PWR-82333 are 30 A motor drive hybrids rated at +200 V and +500 V respectively. The PWR-82331 uses a MOSFET output stage and the PWR-82333 has an IGBT output stage for high speed, high current, and high efficiency operation. The PWR-82333 also offers high-voltage performance of an IGBT for use in +270 V systems. These motor drives are ideal for use in high-performance motion control systems, servo amplifiers, and motor speed control designs. Furthermore, multi-axis systems requiring multiple drive stages can benefit from the small size of these power drives.

The PWR-82331/82333 can be driven directly from the commutation logic, DSP, or a custom ASIC that supplies digital signals to control the upper and lower transistors of each phase. These highly integrated drive stages have Schmitt trigger digital inputs that control the high and low side of each phase. Digital protection of each phase eliminates an in-line firing condition by preventing simultaneous turn-on of both the upper and lower transistors. The logic controls the high- and low-side gate drivers. Operation from +5 to +15 V logic levels can be programmed by applying the appropriate voltage to pin 16 (VLPI). The PWR-82331/82333 has a ground referenced low-side gate drive. An internal dc-dc converter supplies a floating output to each side of the three high-side drives. This provides a continuous high-side gate drive even during the motor stall. Pin 15 (VLPO) supplies a +15 V output, which can be used to power the internal logic when system usage requires +15 V logic. The high- and low-side gate drivers control the N-channel MOSFET or IGBT output stage.



(REFERENCE TABLE 2. ALSO.)

FIGURE 2. INPUT/OUTPUT TIMING RELATIONSHIPS

The MOSFETs used in the PWR-82331 allow output switching up to 50 kHz, while the high-speed IGBTs in the PWR-82333 can switch at 25 kHz. A flyback diode parallels each output transistor and controls the regenerative energy produced by the motor. These fast recovery diodes have faster reverse switching times than the intrinsic body diode of the MOSFETs used in the PWR-82331. They also protect the IGBTs used in the PWR-82333 from exceeding their emitter-to-collector breakdown voltage. Use of a copper case and solder attachment of the output transistors achieves a low thermal resistance of 0.85° C/W maximum. Care should be taken to adequately heatsink these motor drives to maintain a case temperature of 125°C. Junction temperatures should not exceed 150°C. The PWR-82331/82333 do not have internal short-circuit or overcurrent protection. For protection of the output transistors, these features must be added externally to the hybrid.

BIAS VOLTAGES

The PWR-82331/82333 motor drive hybrids require only a single power supply for operation. The hybrid generates three independent floating supplies, eliminating the need for external bias voltages for each phase.

In order for the internal power supply to generate these voltages, the input bias voltage (Vb) must be from +15 to +50 Vdc. In most avionic systems this can be accomplished by connecting the Vb pin to the MIL-STD-704D, +28 Volt bus. See FIGURE 3A.

If the system bus voltage is greater than +50 Vdc (and a lower voltage is not available), then the Vb pin and Vz pin can be tied together with an external power resistor (Rb) and connected from these pins to the system power bus. (See FIGURE 3B).

See FIGURES 4 and 5 for bias resistor characteristics.

If additional power dissipation in Rb is a concern, FIGURE 3C shows a more efficient design, using a low-power resistor (RT) and an additional transistor. To determine the proper resistor to use, refer to FIGURE 6.

If there is another voltage available in the system in the +15 to +50 Vdc range, then this voltage can be directly connected to the Vb pin of the hybrid.

In any case, a 0.01 mF decoupling capacitor (Cb) must be connected between Vb (pin 12) and GND.

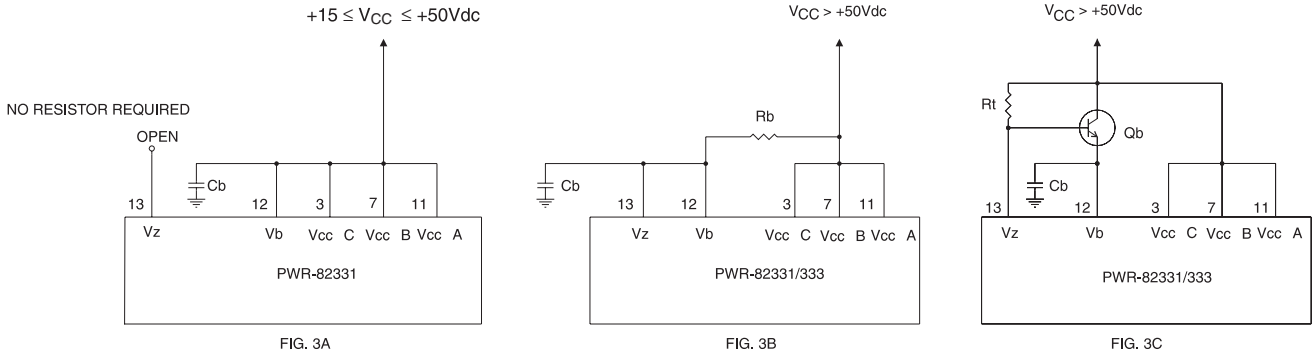


FIG. 3A FIG. 3B FIG. 3C

NOTE: Cb = 0.01mF, 100V, CERAMIC; FOR PWR-82331, Qb = 200V, 6W TRANSISTOR; FOR PWR-82333, Qb = 500V, 12W TRANSISTOR

FIGURE 3. CONNECTION TO BUS VOLTAGE TO DEVELOP PROPER INPUT BIAS VOLTAGE

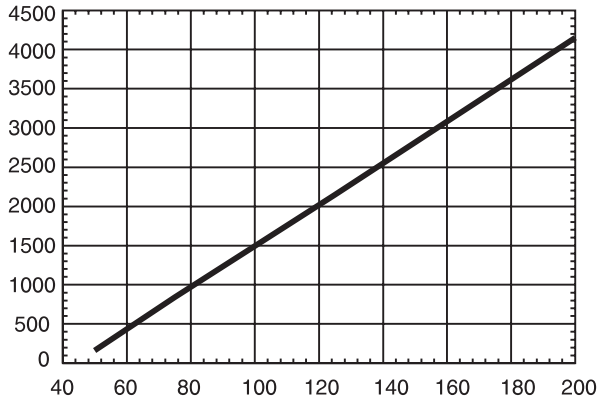


FIGURE 4A. PWR-82331

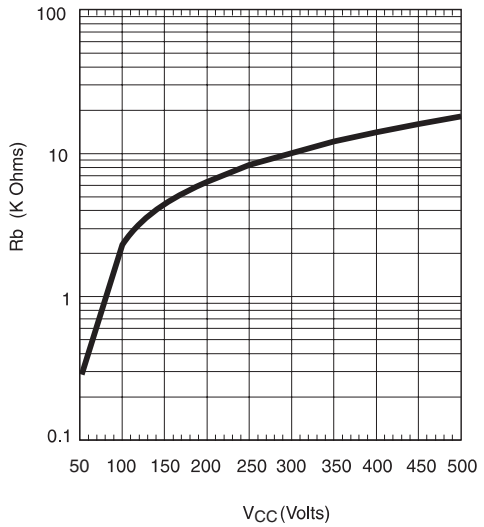


FIGURE 4B. PWR-82333

FIGURE 4. BIAS RESISTOR VALUE (R_b) VS. BUS VOLTAGE (V_{CC})

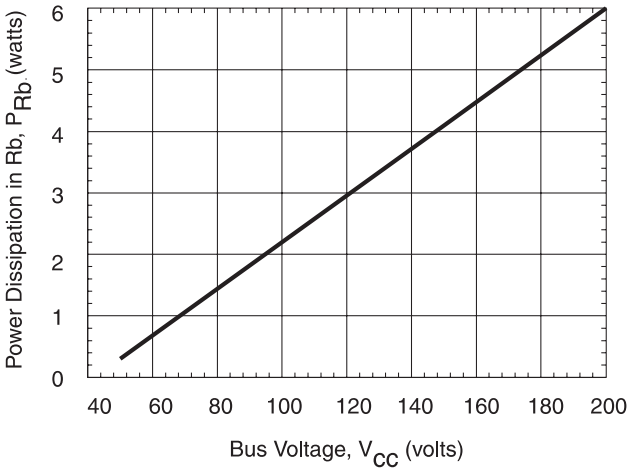


FIGURE 5A. PWR-82331

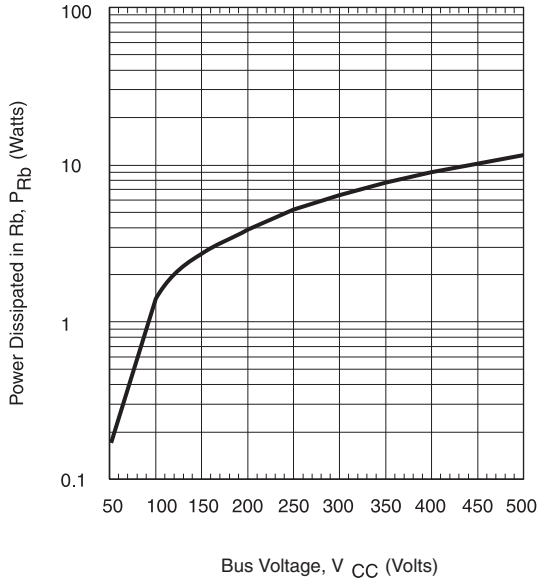


FIGURE 5B. PWR-82333

FIGURE 5. POWER DISSIPATED IN BIAS RESISTOR (R_b) VS. BUS VOLTAGE (V_{CC})

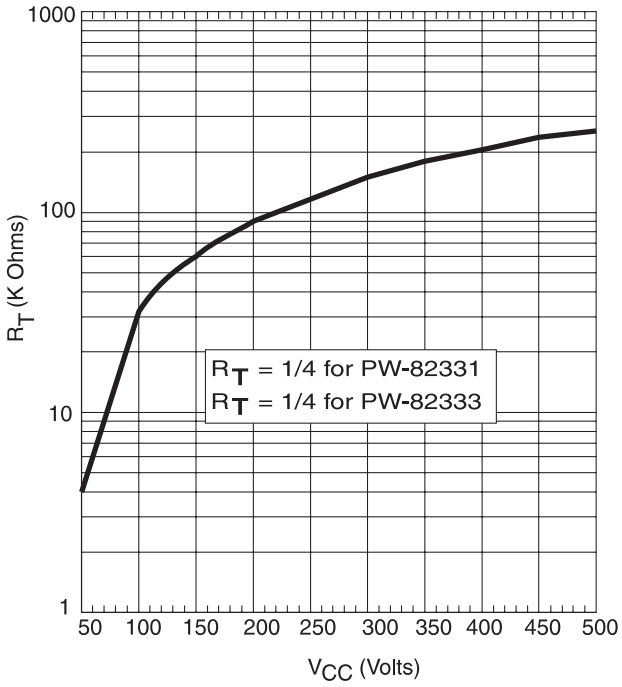


FIGURE 6. R_T RESISTOR VALUE VS. BUS VOLTAGE

DIGITALLY CONTROLLED INPUTS

The PWR-82331/82333 uses Schmitt triggered digital inputs (with hysteresis) to ensure high-noise immunity. The trigger switches at different points for positive and negative going signals. The hysteresis voltage (VH) is the difference between the positive going voltage (VP) and the negative going voltage(VN) (see FIGURE 7). The digital inputs have programmable logic levels, which allows the hybrid to be used with different types of commutation logic with an input voltage range of +5 V to +15 V, such as TTL or CMOS logic. The PWR-82331/82333 internal power supply generates a +15 Vdc (VLPO) on pin 15. This output can only be used to power the internal digital circuitry within the hybrid. **Do not use this +15 V output to power any circuitry external to the hybrid.** Pin 16 is the logic power input (VLPI) for the digital circuitry inside the hybrid. **A 0.01 mF, +50 V ceramic capacitor must be placed between this pin (16) and GND as close to the hybrid as possible.** When using +15 V control circuitry, the logic power input (pin 16) can be connected directly to logic power output (pin 15) of the hybrid. There is no need for an additional external power supply.

When using +5 V control logic, an external +5 Vdc supply must be connected between pin 16 of the hybrid and the GND - leave Pin 15 open (N/C). The commutation/control circuitry can be as simple as discrete logic with PWM, or as sophisticated as a microprocessor or custom ASIC, depending on the system requirements. The block diagram in FIGURE 8 shows a typical interface of the PWR-82331/82333 with a motor and commutation logic in a servo-amp system.

INTERFACING WITH OPTOCOUPLERS

Optocouplers should be used when the commutation logic cannot be located directly next to the motor drive (within 1"- 2" from the input) or a current sensing resistor is placed between VSS and POWER RTN (see FIGURE 9). The optocouplers minimize the differential ground voltage drop between the logic grounds and the VSS connections. Optocouplers are also required when +5 V logic is used to control the motor drive.

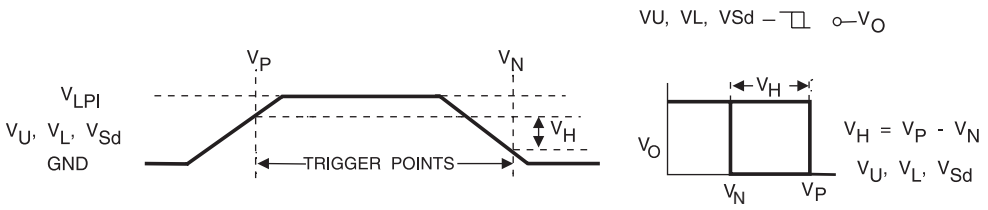
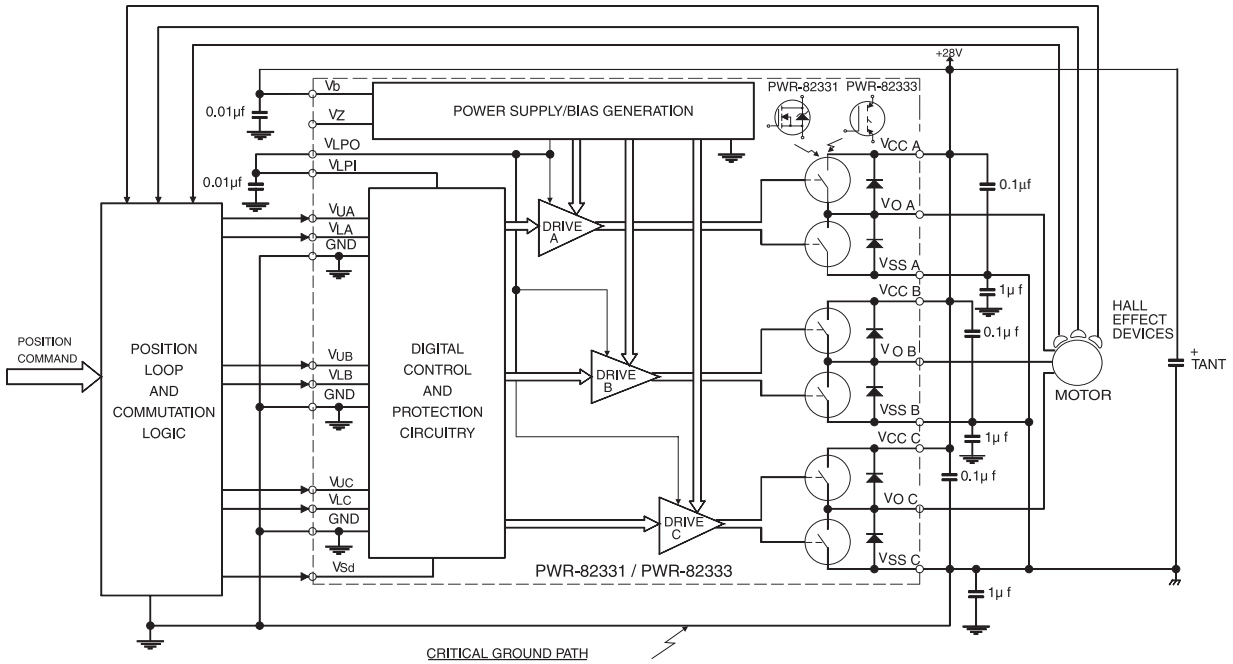


FIGURE 7. HYSTERESIS DEFINITION AND CHARACTERISTICS



To prevent damage to the internal drive circuitry, the differential voltage between GND (pins 19,22,26) and Vss (pins 1,5,8) must not exceed ±3 V max, dc or peak.

FIGURE 8. PWR-82331/82333 TYPICAL INTERFACE WITH A MOTOR AND COMMUTATION LOGIC

SHUT-DOWN INPUT (VSD)

Pin 23 (Vsd) provides a digital shut-down input, which allows the user to completely turn-off both the upper and lower output transistors in all 3-phases. Application of a logic “1” to the Vsd input will latch the Digital Control/Protection circuitry thereby turning off all output transistors. The Digital Control/Protection circuitry remains latched in the off-state and will not respond to signals on the VL or VU inputs while the Vsd has a logic “1” applied. When the user or the sense circuitry (as in FIGURE 9) returns the Vsd input to a logic “0,” and then the user sets the VL and VU inputs to a logic “0” the output of the Digital Control/Protection circuitry will clear the internal latch. When the next rising edge (see FIGURE 10) occurs on the VL or VU digital inputs, the output transistors will respond to the corresponding digital input. This feature can be used with external current limit or temperature sense circuitry to disable the drive if a fault condition occurs.

INTERNAL PROTECTION CIRCUITRY

The hybrid contains digital protection circuitry, which prevents in-line transistors from conducting simultaneously. This, in effect, would short circuit the power supply and would damage the output stage of the hybrid. The circuitry allows only proper input signal patterns to cause output conduction. FIGURE 10 and TABLE 3 show these timing relationships. If an improper input requested that the upper and lower transistors of the same phase conduct together, the output would be a high impedance until removal of the illegal code from the input of the PWR-82331/82333. A dead time of 500 ns minimum should still be maintained between the signals at the VU and VL pins; this ensures the complete turn off of any transistor before turning on its associated in-line transistor.

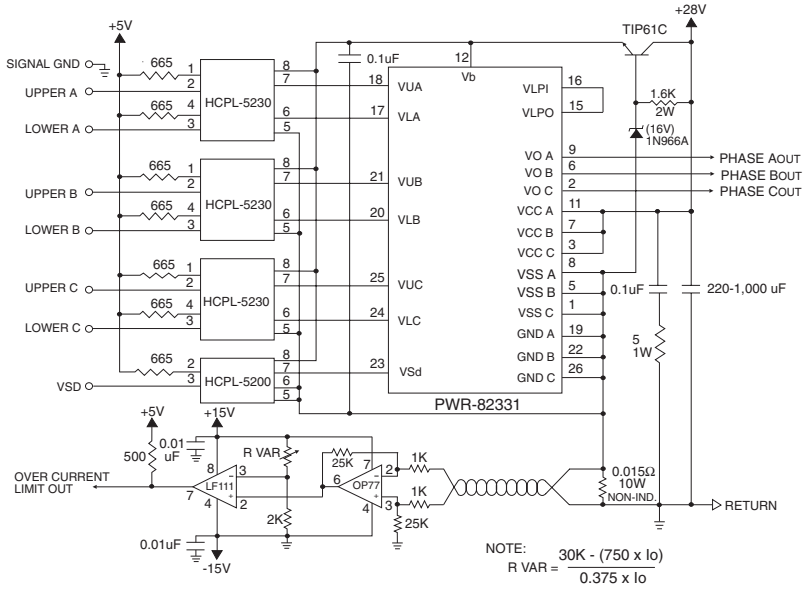


FIGURE 9. TYPICAL OPTOCOUPLER APPLICATION

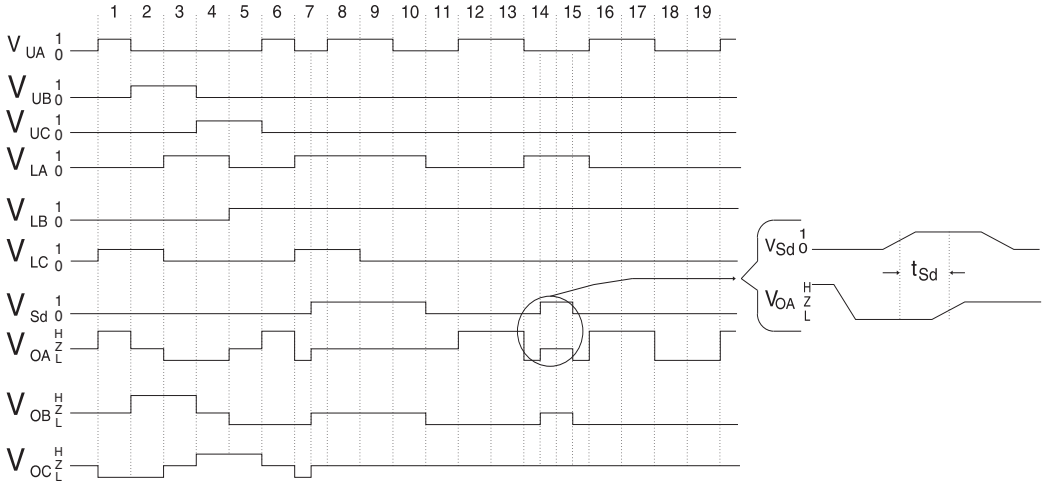


FIGURE 10. SHUT-DOWN (Vsd) TIMING RELATIONSHIPS

PWR-82331 POWER DISSIPATION (SEE FIGURE 11)

There are three major contributors to power dissipation in the motor driver: conduction losses, switching losses, and flyback diode losses.

V_{CC} = +140 V (Bus Voltage)
I_{OA} = 20 A (See FIGURE 11); I_{OB} = 30 A; (See FIGURE 11)
ton = 20 µs (See FIGURE 11); T= 40 µs (period)
Ron = 0.1 Ω (on-resistance see TABLE 2, I_O = 30 A,T_C = +25° C)
ts1 = 250 ns (see FIGURE 11); ts2 = 250 ns (see FIGURE 11)
fo = 25 kHz (switching frequency)
V_F is the diode forward voltage, Table 2, I_O = 30 A, T_C= +25° C
V_F(avg) = +1.15 V; I_F is the diode forward current

1. Conduction Losses (P_C)

$P_C = (I_{motor\ rms})^2 \times Ron$

$$I_{motor\ rms} = \sqrt{\left(IOB^2 - IOB\,(IOB - IOA) + \frac{(IOB - IOA)^2}{3}\right)\left(\frac{ton}{T}\right)}$$

$$I_{motor\ rms} = \sqrt{\left(30^2 - 30\,(30 - 20) + \frac{(30 - 20)^2}{3}\right)\left(\frac{20}{40}\right)}$$

$P_C = (17.80\ A)^2 \times (0.1\ \Omega)$
P_C = 31.68 Watts

2. Switching Losses (Ps)

$P_S = [V_{CC}\,(I_{OA}\,(ts1) + I_{OB}\,(ts2))\,fo]\,/2$
$P_S = [140\,(20\,(250\ ns) + 30(250\ ns))25k]/2$
P_S = 21.88 Watts

3. Flyback Diode Losses (P_{df})

$P_{df} = I_F\,(avg) \times V_F\,(avg)$
$I_F\,(avg) = [(I_{OB} + I_{OA})\,/2]\,/2 = [(30 + 20)/2]/2 = 12.5$ A
Pdf = 12.5 A x 1.15 V
Pdf = 14.38 Watts

Transistor Power Dissipation (P_Q)

To calculate the maximum power dissipation of the output transistor as a function of the case temperature use the following equation. (Reference FIGURE 20 to ensure you don't exceed the maximum allowable power dissipation of each transistor.)

$$P_Q = P_C + P_S$$

Total Hybrid Power Dissipation (P_{TOTAL})

To calculate Total Power dissipated in the hybrid use:

$$P_{TOTAL} = \sum_{i=1}^{6} [P_{Qi} + P_{dfi}]$$ where i = each transistor or diode.

PWR-82333 POWER DISSIPATION (SEE FIGURE 11)

There are three major contributors to power dissipation in the motor driver: conduction losses, switching losses, and flyback diode losses.

V_{CC} = + 270 V (Bus Voltage)
I_{OA} = 20 A (See FIGURE 11); I_{OB} = 30 A; (See FIGURE 11)
ton = 50 µs (See FIGURE 11); T=100 µs (period)
$V_{CE(SAT)}$ = 3.8 V (see TABLE 2, I_O = 30 A,T_C= +25° C)
ts1 = 300 ns (see FIGURE 11); ts2 = 300 ns (see FIGURE 11)
fo = 10 kHz (switching frequency)
V_F is the diode forward voltage, TABLE 2, I_O = 30 A, T_C= +25° C
V_F (avg) = +1.70 V; I_F is the diode forward current

1. Conduction Losses (P_C)

$P_C = (I_{motor\ rms}) \times V_{CE(SAT)}$

$$I_{motor\ rms} = \sqrt{\left(IOB^2 - IOB\,(IOB - IOA) + \frac{(IOB - IOA)^2}{3}\right)\left(\frac{ton}{T}\right)}$$

$$I_{motor\ rms} = \sqrt{\left(30^2 - 30\,(30 - 20) + \frac{(30 - 20)^2}{3}\right)\left(\frac{50}{100}\right)}$$

$P_C = (17.80\ A) \times (3.8\ V)$
P_C = 67.64 Watts

2. Switching Losses (Ps)

$P_S = [V_{CC}\,(I_{OA}\,(ts1) + I_{OB}\,(ts2))\,fo]\,/2$
$P_S = [\,270\,(20\,(300\ ns) + 30\,(300\ ns))10k]/2$
P_S = 20.25 Watts

3. Flyback Diode Losses (P_{df})

$P_{df} = I_F\,(avg) \times V_F\,(avg)$
$I_F\,(avg) = [(I_{OB} + I_{OA})\,/2]\,/2 = [(30 + 20)/2]\,/2 = 12.5$ A
P_{df} = 12 5 A x 1.70 V
P_{df} = 21.25 Watts

Transistor Power Dissipation (P_Q)

To calculate the maximum power dissipation of the output transistor as a function of the case temperature use the following equation. (Reference FIGURE 20 to ensure you don't exceed the maximum allowable power dissipation of each transistor.)

$$P_Q = P_C + P_S$$

Total Hybrid Power Dissipation (P_{TOTAL})

To calculate Total Power dissipated in the hybrid use:

$$P_{TOTAL} = \sum_{i=1}^{6} [P_{Qi} + P_{dfi}]$$ where i = each transistor or diode.

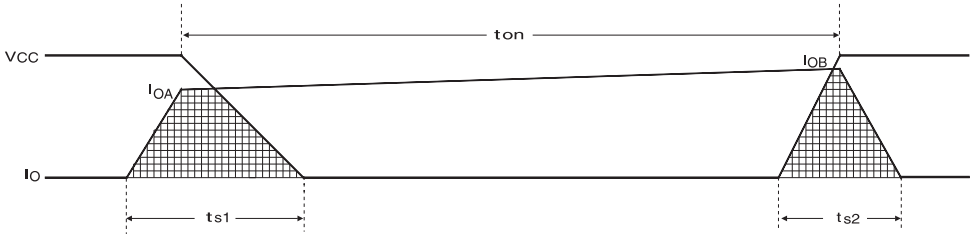


FIGURE 11. OUTPUT CHARACTERISTICS

GROUND CONNECTIONS

LAYOUT AND EXTERNAL COMPONENTS

Important: The following layout guidelines and required external components are critical to the proper operation of these motor drives.

External connections can be easily made to the hybrid by any of the following methods:

- Solder a wire around each pin.
- Use pin extenders to raise the height of each pin so a printed circuit board can be mounted on top of the hybrid.
- Use a printed circuit board with a cutout that will enable the printed circuit board to slide over the pins.

Permanent damage will result to the motor drive if the user does not make the following recommended ground connections that will ensure the proper orientation of the hybrid.

The Vb and logic grounds are on pins 19, 22 and 26 (GND). The VSS connections for the output stage are on pins 1, 5, and 8 (VSS). **To prevent damage to the internal drive circuitry, the differential voltage between the GND (pins 19, 22, 26) and VSS (pins 1, 5, 8) must not exceed ± 3 V max, dc or peak.** This includes the combined voltage drop of the associated ground paths and the voltage drop across RSENSE (see FIGURE 12).

For example, a value for RSENSE of 0.025 Ω will give a voltage drop of +1.25 V at 50 A and allow enough margin for the voltage drop in the ground conductors. Locate RSENSE 1" - 2" maximum from the hybrid. It is critical that all ground connections be as short, and of lowest impedance, as the system allows.

C1, C2, and C3 are 1 mF, +10 V ceramic capacitors that provide a low ac impedance between Vss pin and GND. You must use one capacitor for each VSS pin-to-GND connection (total of three capacitors in all), these capacitors are independent of the type of drive scheme used. (i.e., Trapezoidal or Sinusoidal drive). Since placement of these capacitors is critical, place these capacitors across the hybrid, if possible. Please note, on FIGURE 12, that C1, C2, and C3 must go directly from terminal-to-terminal on the hybrid - do not daisy chain along the ground return.

C4, C5, and C6 are the 0.1 mF ceramic bypass capacitors that suppress high frequency spiking. The voltage rating should be two times the maximum system voltage. These capacitors should be located as close to the hybrid as possible.

Care must be taken to control the regenerative energy produced by the motor in order to prevent excessive spiking on the Vcc line. Accomplish this by placing a capacitor or clamping diode between the Vcc and the high-power ground return.

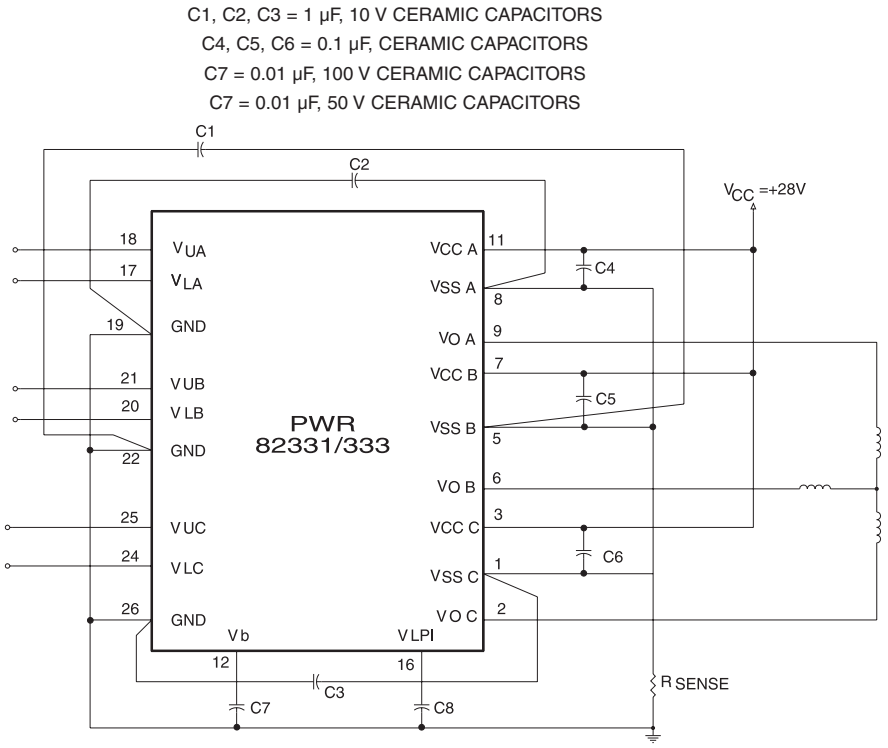


FIGURE 12. PWR-82331/82333 GROUND CONNECTIONS

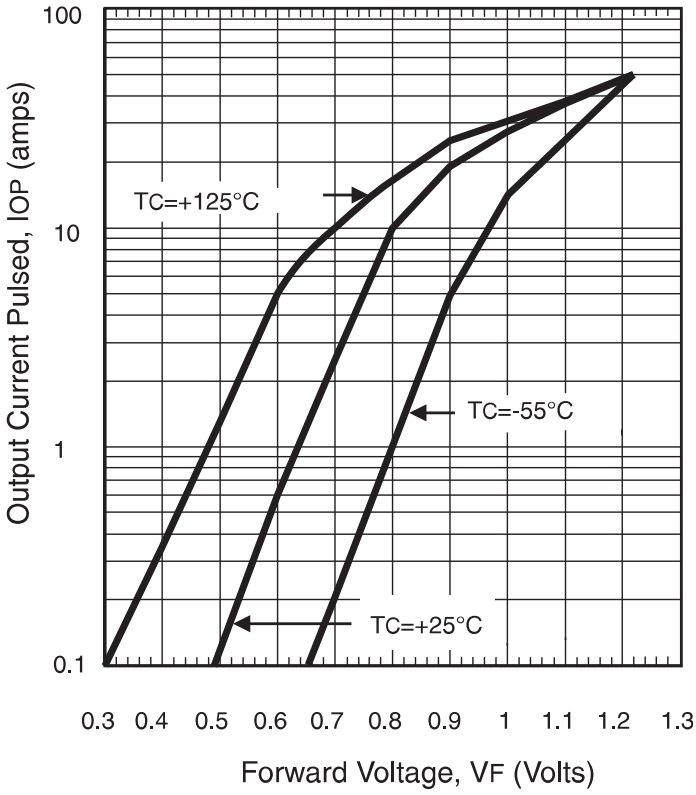


FIGURE 13A. PWR-82331 TYPICAL FORWARD VOLTAGE DROP OF FLYBACK DIODES

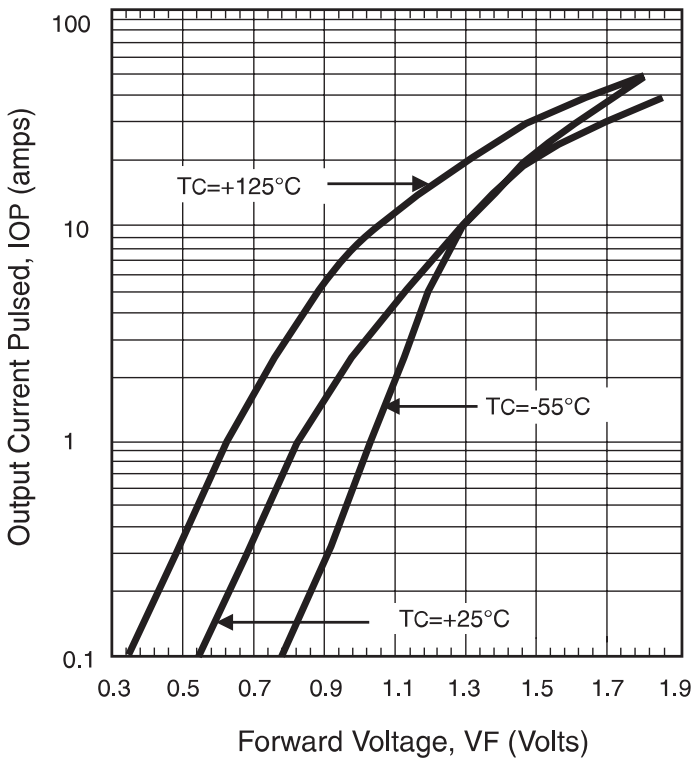


FIGURE 13B. PWR-82333 TYPICAL FORWARD VOLTAGE DROP OF FLYBACK DIODES

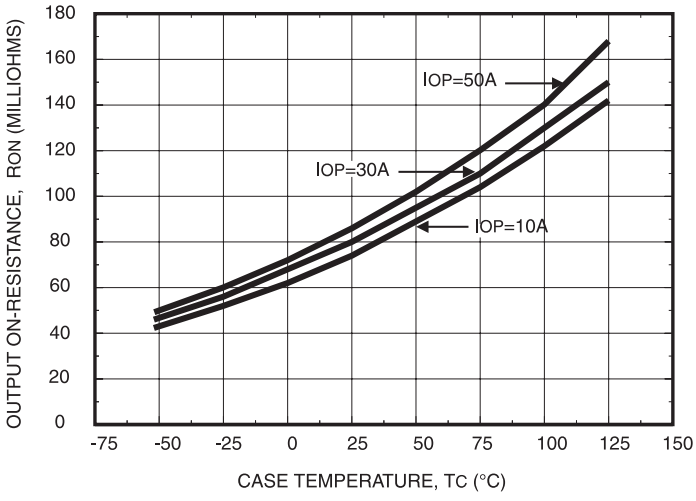


FIGURE 14A. PWR-82331 TYPICAL ON RESISTANCE VARIATION WITH TEMPERATURE

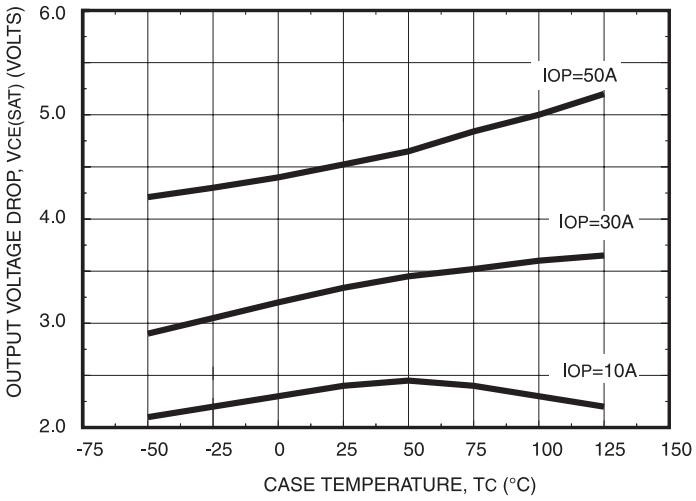


FIGURE 14B. PWR-82333 TYPICAL $V_{CE(SAT)}$ VARIATION WITH TEMPERATURE

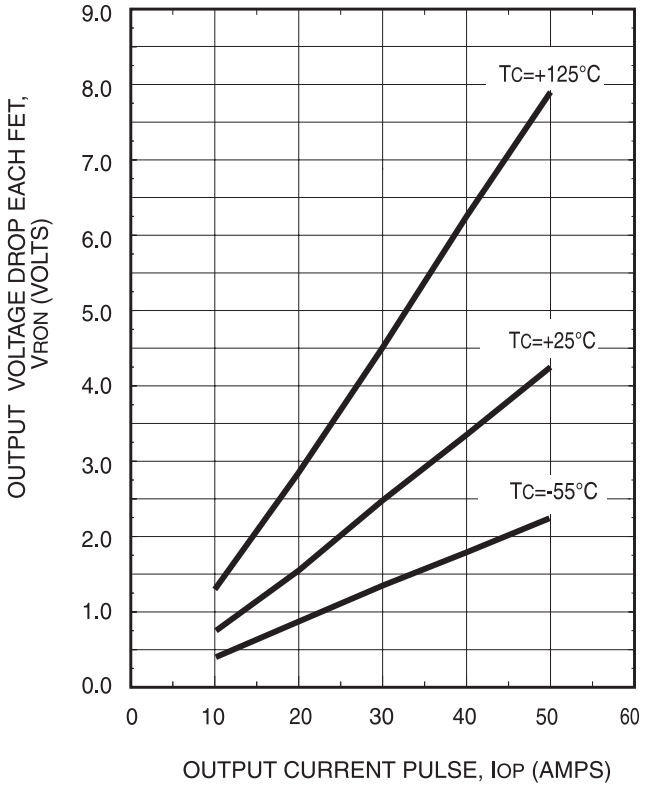


FIGURE 15A. PWR-82331 TYPICAL OUTPUT ON VOLTAGE DROP VERSUS OUTPUT CURRENT

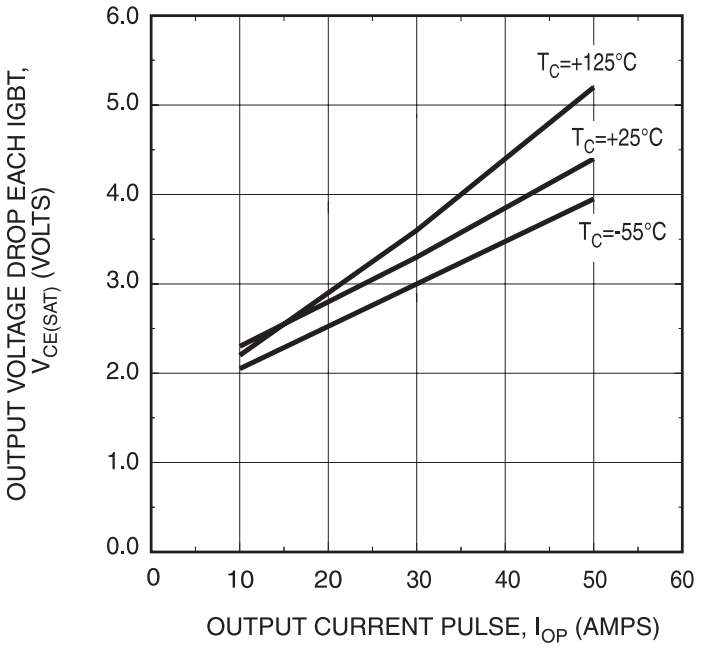


FIGURE 15B. PWR-82333 TYPICAL OUTPUT ON VOLTAGE VERSUS OUTPUT CURRENT

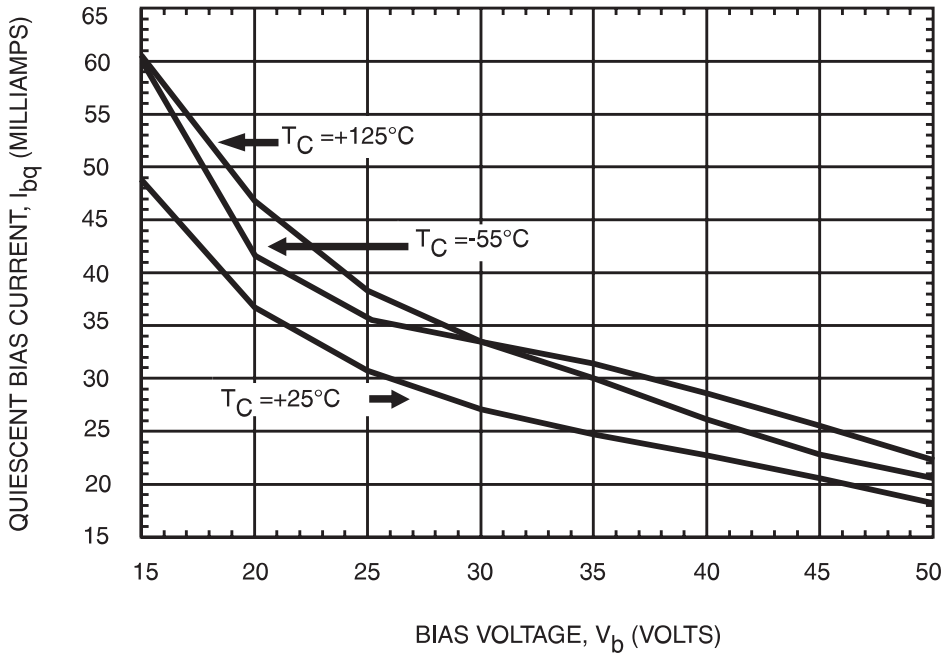


FIGURE 16. PWR-82331/82333 TYPICAL QUIESCENT BIAS CURRENT VERSUS BIAS VOLTAGE

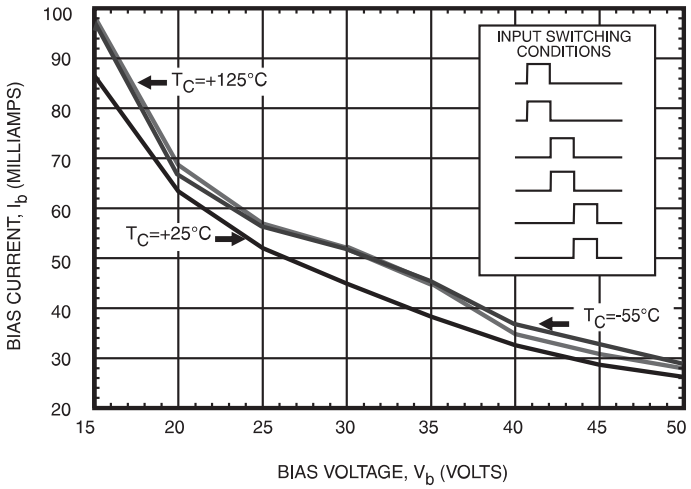


FIGURE 17A. PWR-82331 TYPICAL BIAS CURRENT VERSUS BIAS VOLTAGE AT fo = 30 kHz

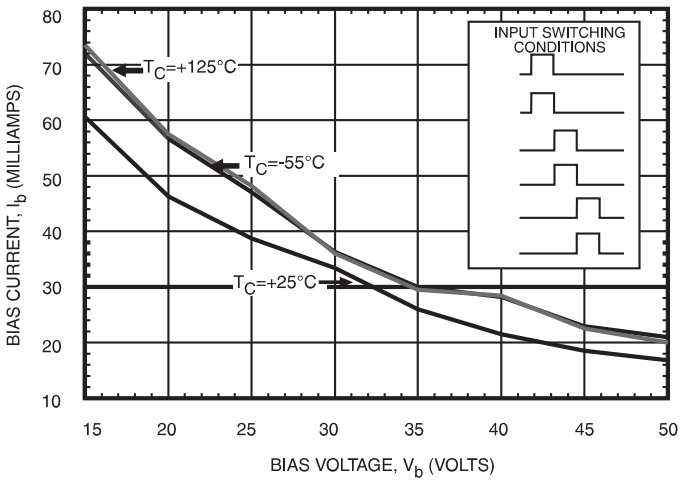


FIGURE 17B. PWR-82333 TYPICAL BIAS CURRENT VERSUS BIAS VOLTAGE AT fo = 10 kHz

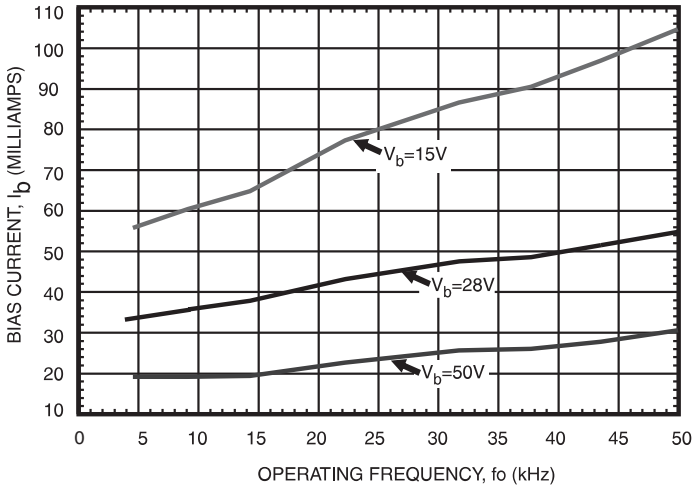


FIGURE 18A. PWR-82331 BIAS CURRENT VERSUS OPERATING FREQUENCY

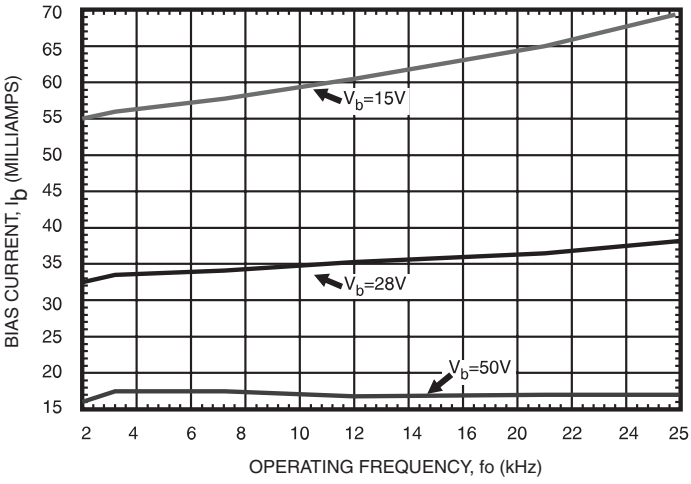


FIGURE 18B. PWR-82333 BIAS CURRENT VERSUS OPERATING FREQUENCY

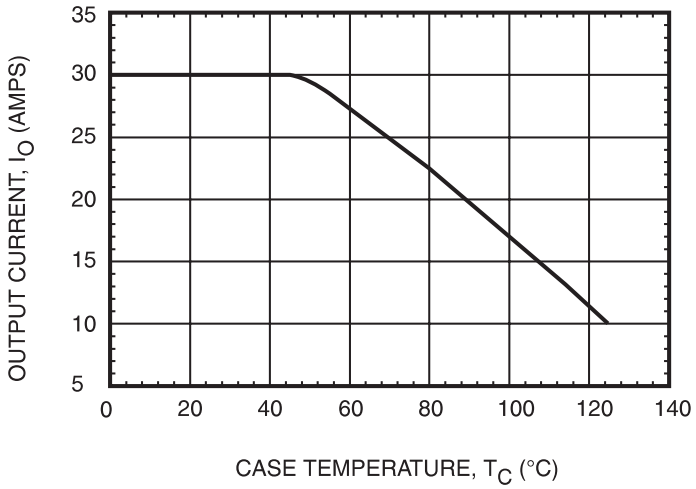


FIGURE 19A. PWR-82331
MAXIMUM ALLOWABLE CONTINUOUS OUTPUT CURRENT VERSUS CASE TEMPERATURE

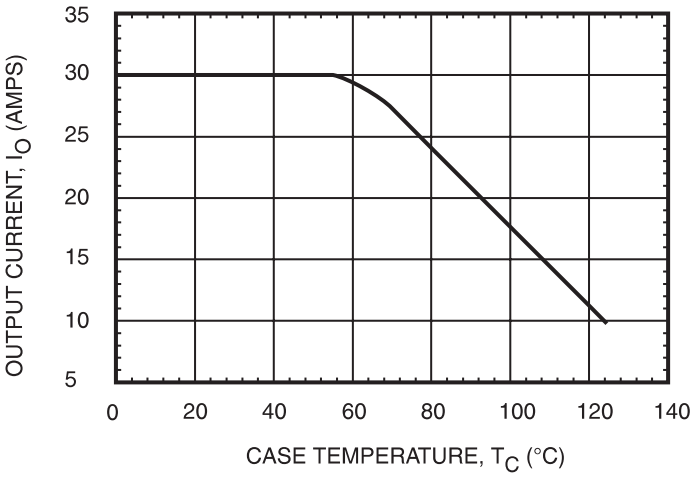


FIGURE 19B. PWR-82333
MAXIMUM ALLOWABLE CONTINUOUS OUTPUT CURRENT VERSUS CASE TEMPERATURE

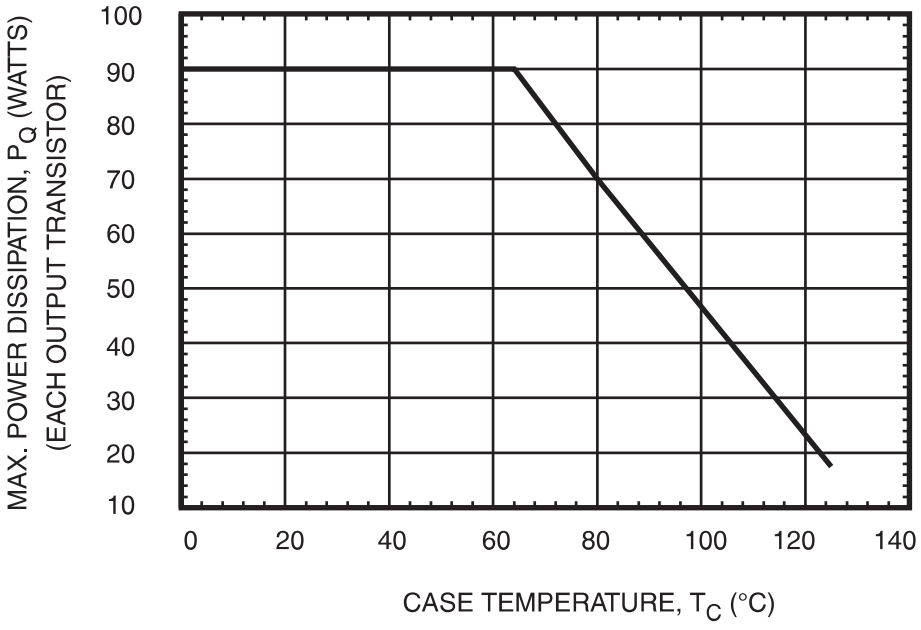


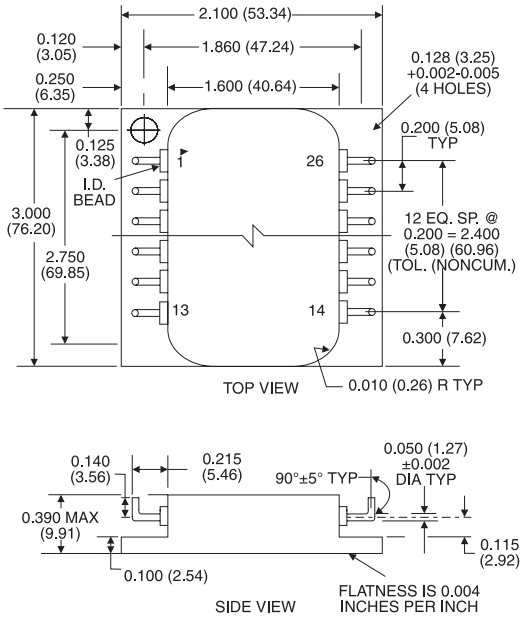
FIGURE 20. PWR-82331/82333
MAXIMUM ALLOWABLE POWER DISSIPATION OF EACH OUTPUT TRANSISTOR VERSUS CASE TEMPERATURE

TABLE 3. INPUT-OUTPUT TRUTH TABLE									
INPUTS							OUTPUTS		
UPPERS			LOWERS			CONTROL			
V_{UA}	V_{UB}	V_{UC}	V_{LA}	V_{LB}	V_{LC}	V_{Sd}	$V_{O\,A}$	$V_{O\,B}$	$V_{O\,C}$
1	0	0	0	1	0	0	H	L	Z
1	0	0	0	0	1	0	H	Z	L
0	1	0	0	0	1	0	Z	H	L
0	1	0	1	0	0	0	L	H	Z
0	0	1	1	0	0	0	L	Z	H
0	0	1	0	1	0	0	Z	L	H
0	0	1	1	1	0	0	L	L	H
0	1	0	1	0	1	0	L	H	L
0	1	1	1	0	0	0	L	H	H
1	0	0	0	1	1	0	H	L	L
1	0	1	0	1	0	0	H	L	H
1	1	0	0	0	1	0	H	H	L
0	1	1	1	0	1	0	L	H	Z
0	1	1	1	1	0	0	L	Z	H
1	0	1	0	1	1	0	H	L	Z
1	0	1	1	1	0	0	Z	L	H
1	1	0	0	1	1	0	H	Z	L
1	1	0	1	0	1	0	Z	H	L
0	0	0	0	0	0	0	Z	Z	Z
0	0	0	1	1	1	0	L	L	L
1	1	1	0	0	0	0	H	H	H
x	x	x	x	x	x	1	Z	Z	Z
H = High Level, L = Low Level, X = Irrelevant, Z = High Impedance									

TABLE 4. PIN ASSIGNMENTS			
PIN	FUNCTION	PIN	FUNCTION
1	$V_{SS\,C}$	26	GND
2	$V_{O\,C}$	25	V_{UC}
3	$V_{CC\,C}$	24	V_{LC}
4	N/C	23	V_{Sd}
5	$V_{SS\,B}$	22	GND
6	$V_{O\,B}$	21	V_{UB}
7	$V_{CC\,B}$	20	V_{LB}
8	$V_{SS\,A}$	19	GND
9	$V_{O\,A}$	18	V_{UA}
10	N/C	17	V_{LA}
11	$V_{CC\,A}$	16	V_{LPI}
12	V_b	15	V_{LPO}
13	V_z	14	N/C
Notes: 1. Pins 3, 7, and 11 are internally connected. 2. Pins 19, 22 and 26 are internally connected.			

MOUNTING

The package bolts to part of the chassis or even the motor assembly itself, depending on system requirements. In applications where this isn't convenient, the hybrid can be mounted to its own heatsink. The heat transfer in the hybrid is from semiconductor junction to the bottom of the hybrid case. The flatness and maximum temperature of this mounting surface are critical to proper performance and reliability, because this is the only method of dissipating the power created in the hybrid. Use a mounting surface flatness of 0.004 inches/inch maximum. This interface can be improved with the use of a thermal compound or pad. The heatsink should be designed to insure that the case temperature does not exceed +125°C.



NOTE: Dimensions in inches (mm)

FIGURE 21. PWR-82331/82333 MECHANICAL OUTLINE

ORDERING INFORMATION

PWR-8233X-XX0X

Supplemental Process Requirements:
S = Pre-Cap Source Inspection
L = 100% Pull Test
Q = 100% Pull Test and Pre-Cap Source Inspection
Blank = None of the Above

Process Requirements:
0 = Standard DDC Processing, no Burn-In (See table below.)
1 = MIL-PRF-38534 Compliant **
2 = B*
3 = MIL-PRF-38534 Compliant with PIND Testing **
6 = B* with PIND Testing

Temperature Grade/Data Requirements:
1 = -55°C to +125°C
2 = -40°C to +85°C
3 = 0°C to +70°C
4 = -55°C to +125°C with Variables Test Data
5 = -40°C to +85°C with Variables Test Data
8 = 0°C to +70°C with Variables Test Data

Rating:
1 = 200 V using MOSFETs
3 = 500 V using IGBTs

*Standard DDC Processing with burn-in and full temperature test — see table below.
** Contact factory for availability.

STANDARD DDC PROCESSING FOR HYBRID AND MONOLITHIC HERMETIC PRODUCTS

TEST	MIL-STD-883	
	METHOD(S)	CONDITION(S)
INSPECTION	2009, 2010, 2017, and 2032	—
SEAL	1014	A and C
TEMPERATURE CYCLE	1010	C
CONSTANT ACCELERATION	2001	3000g
BURN-IN	1015 (note 1), 1030 (note 2)	TABLE 1

Notes:
1. For Process Requirement "B*" (refer to ordering information), devices may be non-compliant with MIL-STD-883, Test Method 1015, Paragraph 3.2. Contact factory for details.
2. When applicable.

Please visit our Web site at **www.ddc-web.com** for the latest information.

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