CY7C1020CV26

512 Kb (32 K × 16) Static RAM

Features

- Temperature range
  - Automotive: –40 °C to 125 °C
- High speed
  - t_{AA} = 15 ns
- Optimized voltage range: 2.5 V to 2.7 V
- Automatic power down when deselected
- Independent control of upper and lower bits
- CMOS for optimum speed and power
- Package offered: 44-pin TSOP II

Functional Description

The CY7C1020CV26 is a high performance CMOS static RAM organized as 32,768 words by 16 bits. This device has an automatic power down feature that significantly reduces power consumption when deselected.

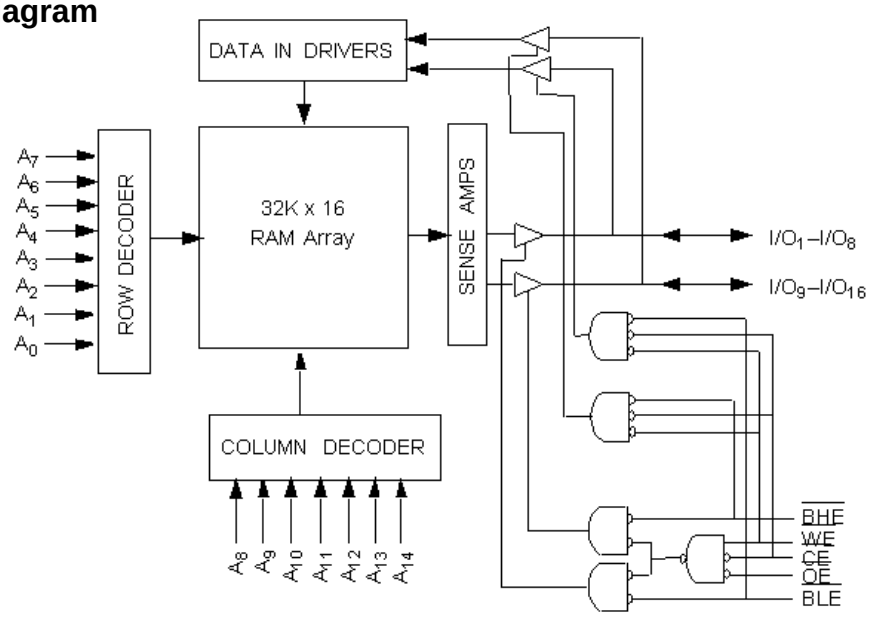
Writing to the device is accomplished by taking chip enable (CE) and write enable (WE) inputs LOW. If byte low enable (BLE) is LOW, then data from I/O pins (I/O_1 through I/O_8), is written into the location specified on the address pins (A_0 through A_{14}). If byte high enable (BHE) is LOW, then data from I/O pins (I/O_9 through I/O_{16}) is written into the location specified on the address pins (A_0 through A_{14}).

Reading from the device is accomplished by taking chip enable (ce) and Output Enable (OE) LOW while forcing the write enable (WE) HIGH. If byte low enable (BLE) is LOW, then data from the memory location specified by the address pins appears on I/O_1 to I/O_8. If Byte High Enable (BHE) is LOW, then data from memory appears on I/O_9 to I/O_{16}. See the Truth Table on page 7 for a complete description of read and write modes.

The input/output pins (I/O_1 through I/O_{16}) are placed in a high impedance state when the device is deselected (CE HIGH), the outputs are disabled (OE HIGH), the BHE and BLE are disabled (BHE, BLE HIGH), or during a write operation (CE LOW, and WE LOW).

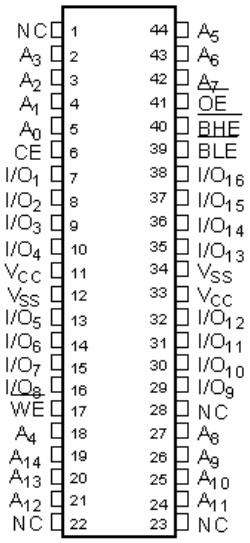
The CY7C1020CV26 is available in a standard 44-pin TSOP Type II.

Logic Block Diagram



Pin Configuration

Figure 1. 44-Pin TSOP II (Top View)



Selection Guide

Description	CY7C1020CV26-15	Unit
Maximum access time	15	ns
Maximum operating current	100	mA
Maximum CMOS standby current	5	mA

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power applied ..... –55 °C to +125 °C

Supply voltage on V_{CC} to relative GND[1].....–0.5 V to +4.6 V

DC voltage applied to outputs in High-Z State[1].....–0.5 V to V_{CC}+0.5 V

DC input voltage[1].....–0.5 V to V_{CC}+0.5 V

Current into outputs (LOW) ..... 20 mA

Static discharge voltage..... > 2001 V (per MIL-STD-883, Method 3015)

Latch up current..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Automotive	–40 °C to +125 °C	2.5 V to 2.7 V

Electrical Characteristics Over the Operating Range

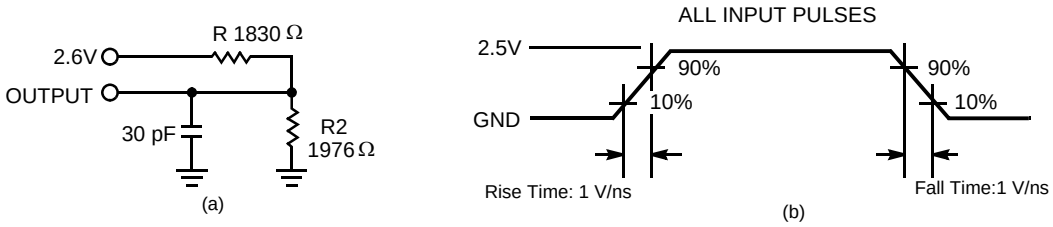
Parameter	Description	Test Conditions	CY7C1020CV26		Unit
			Min	Max	
V_{OH}	Output HIGH voltage	V_{CC} = Minimum, I_{OH} = –1.0 mA	2.3		V
V_{OL}	Output LOW voltage	V_{CC} = Minimum, I_{OL} = 1.0 mA		0.4	V
V_{IH}	Input HIGH voltage		2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW voltage[1]		–0.3	0.8	V
I_{IX}	Input load current	GND ≤ V_I ≤ V_{CC}	–5	+5	µA
I_{OZ}	Output leakage current	GND ≤ V_I ≤ V_{CC}, Output Disabled	–5	+5	µA
I_{OS}[2]	Output short circuit current	V_{CC} = Maximum, V_{OUT} = GND		–300	mA
I_{CC}	V_{CC} operating supply current	V_{CC} = Maximum, I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$		100	mA
I_{SB1}	Automatic CE power-down Current —TTL Inputs	Maximum V_{CC}, $\overline{CE}$ ≥ V_{IH} V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}		40	mA
I_{SB2}	Automatic CE power-down Current —CMOS Inputs	Maximum V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.3 V, V_{IN} ≥ V_{CC} – 0.3 V, or V_{IN} ≤ 0.3 V, f = 0		5	mA

Capacitance[3]

Parameter	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = 2.6 V	8	pF
C_{OUT}	Output capacitance		8	pF

Notes
1. VIL (min.) = –2.0V for pulse durations of less than 20 ns.
2. Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
3. Tested initially and after any design or process changes that may affect these parameters.

Figure 2. AC Test Loads and Waveforms[4]



AC Switching Characteristics Over the Operating Range

Parameter	Description	CY7C1020CV26		Unit
		Min	Max	
READ CYCLE				
t_{RC}	Read cycle time	15		ns
t_{AA}	Address to data valid		15	ns
t_{OHA}	Data hold from address change	3		ns
t_{ACE}	$\overline{CE}$ LOW to data valid		15	ns
t_{DOE}	$\overline{OE}$ LOW to data valid		7	ns
t_{LZOE}	$\overline{OE}$ LOW to low Z[5]	0		ns
t_{HZOE}	$\overline{OE}$ HIGH to high Z[5, 6]		7	ns
t_{LZCE}	$\overline{CE}$ LOW to low Z[5]	3		ns
t_{HZCE}	$\overline{CE}$ HIGH to high Z[5, 6]		7	ns
t_{PU}[7]	$\overline{CE}$ LOW to power-up	0		ns
t_{PD}[7]	$\overline{CE}$ HIGH to power-down		15	ns
t_{DBE}	Byte enable to data valid		7	ns
t_{LZBE}	Byte enable to low Z	0		ns
t_{HZBE}	Byte disable to high Z		7	ns
WRITE CYCLE[8]				
t_{WC}	Write cycle time	15		ns
t_{SCE}	$\overline{CE}$ LOW to write end	10		ns
t_{AW}	Address setup to write end	10		ns
t_{HA}	Address hold from write end	0		ns
t_{SA}	Address setup to write start	0		ns
t_{PWE}	$\overline{WE}$ pulse width	10		ns
t_{SD}	Data setup to write end	8		ns
t_{HD}	Data hold from write end	0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[5]	3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[5, 6]		4	ns
t_{BW}	Byte enable to end of write	10		ns

Notes
4. Test conditions assume signal transition time of 1V/ns or less, timing reference levels of 1.3 V, input pulse levels of 0 to 2.5 V and transmission line loads as in (a) of AC Test Loads.
5. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any device.
6. t_{HZOE}, t_{HZBE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
7. This parameter is guaranteed by design and is not)
8. The internal write time of the memory is defined by the overlap of CE LOW, WE LOW and BHE / BLE LOW. CE, WE and BHE / BLE must be LOW to initiate a write, and the transition of these signals can terminate the write. The input data setup and hold timing should be referenced to the leading edge of the signal that terminates

Switching Waveforms

Figure 3. Read Cycle No. 1[9, 10]

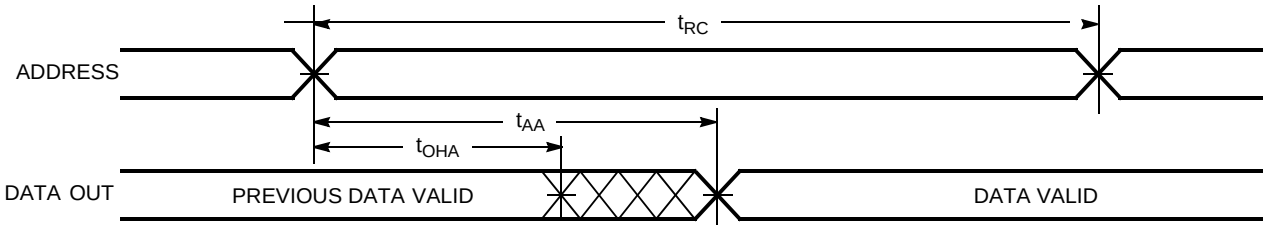
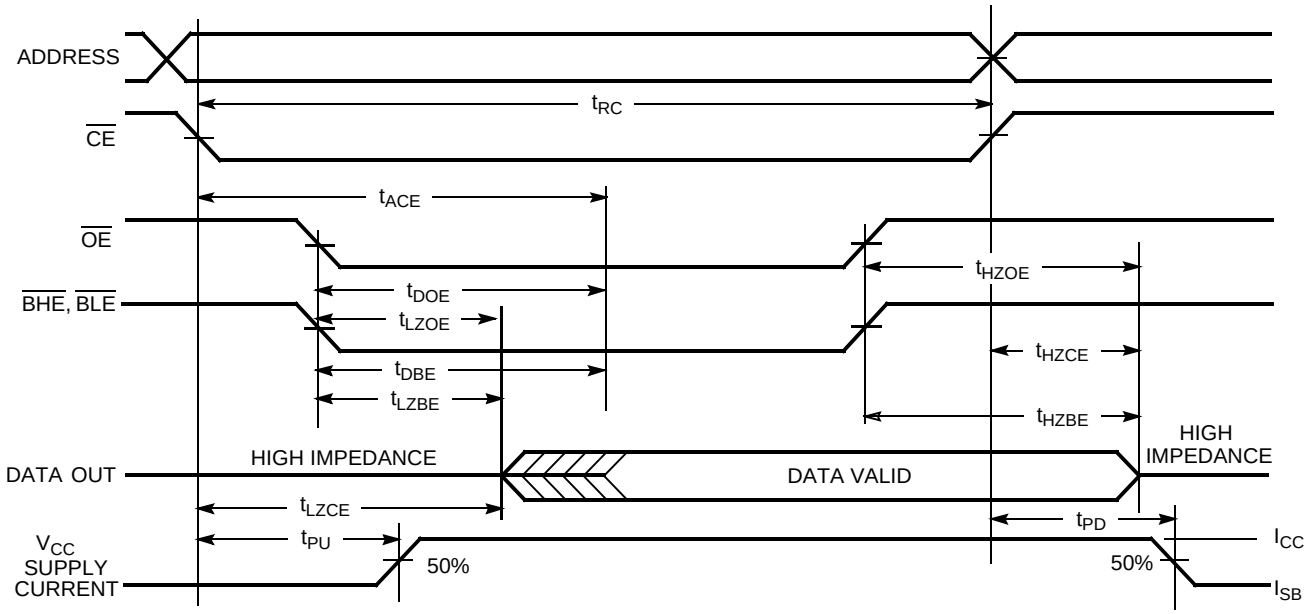


Figure 4. Read Cycle No. 2 ($\overline{OE}$ Controlled)[10, 11]



Notes
9. Device is continuously selected. $\overline{OE}$, $\overline{CE}$, $\overline{BHE}$ and/or $\overline{BHE}$ = V_{IL}.
10. $\overline{WE}$ is HIGH for read cycle.
11. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

Switching Waveforms

Figure 5. Write Cycle No. 1 ($\overline{CE}$ Controlled)[12, 13]

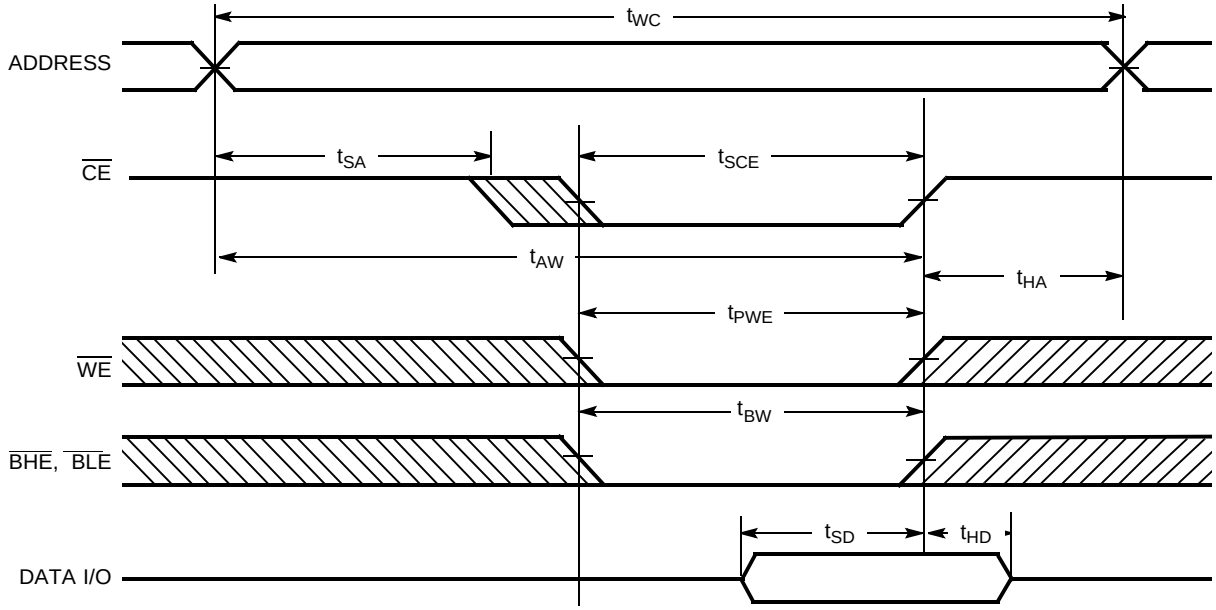
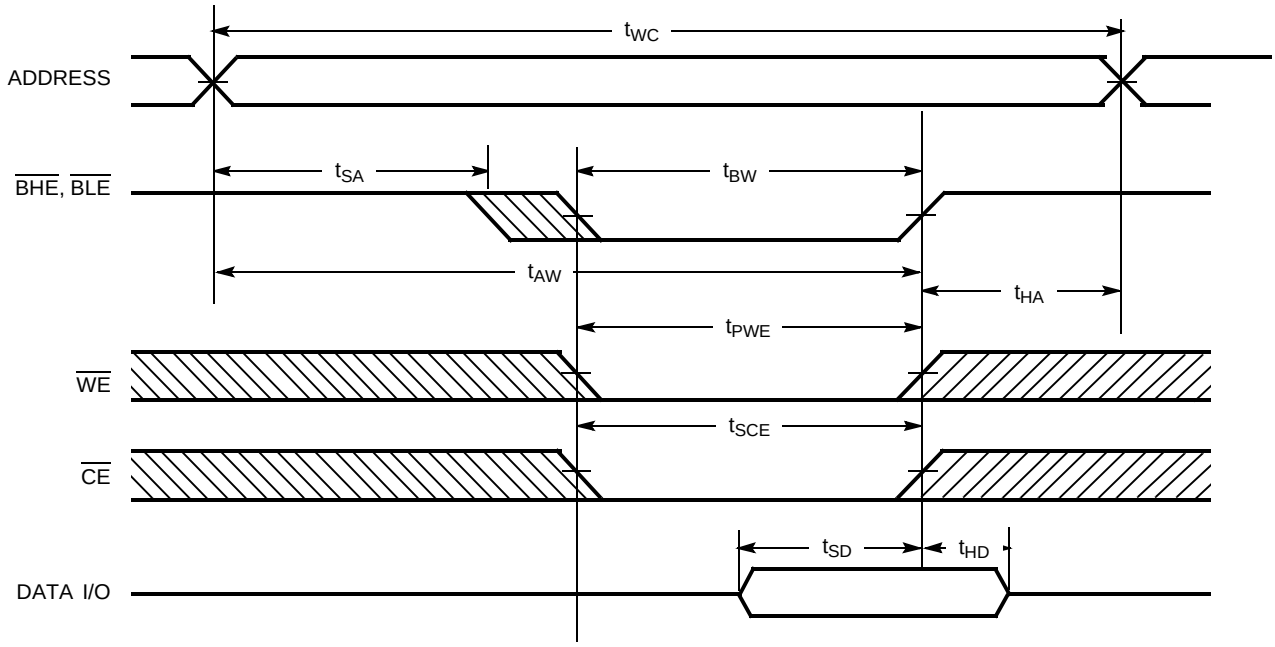


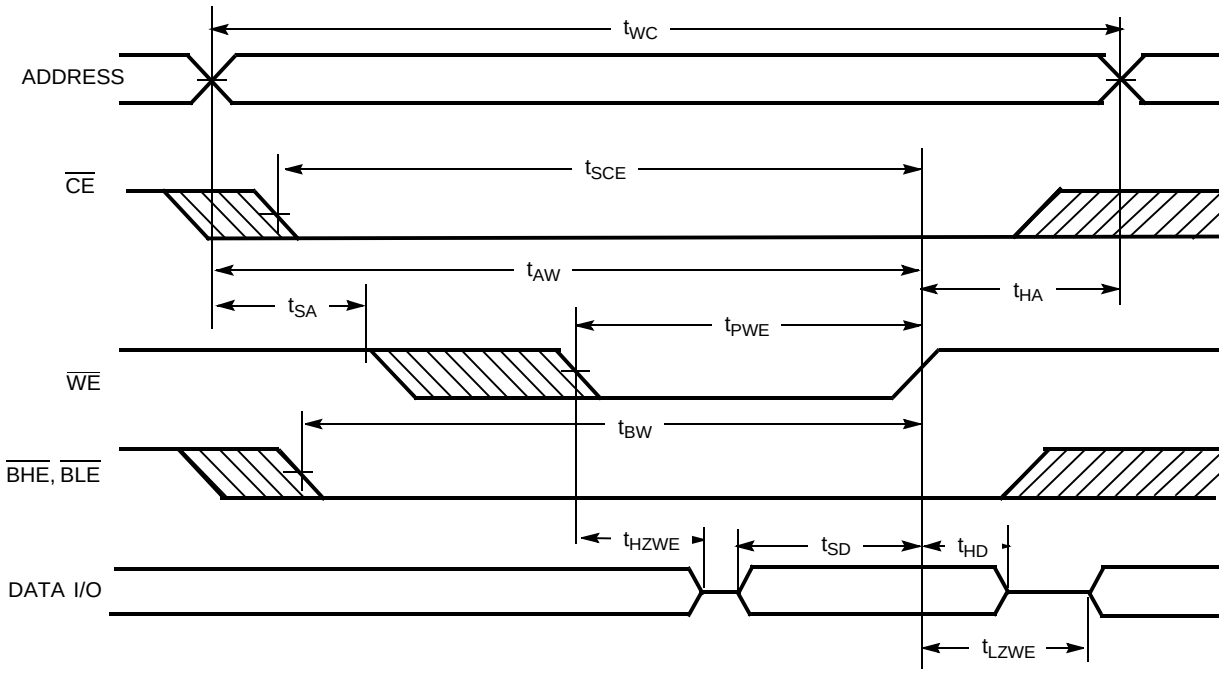
Figure 6. Write Cycle No. 2 ($\overline{BLE}$ or $\overline{BHE}$ Controlled)



Notes
12. Data I/O is high impedance if $\overline{OE}$ or $\overline{BHE}$ and $\overline{BLE}$ = V_{IH}.
13. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high impedance state.

Switching Waveforms

Figure 7. Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)



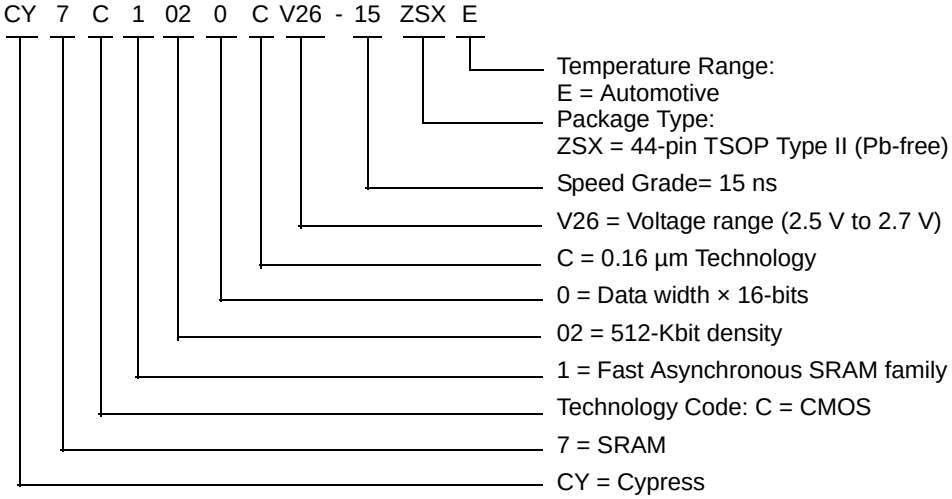
Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	I/O_1–I/O_8	I/O_9–I/O_{16}	Mode	Power
H	X	X	X	X	High Z	High Z	Power-Down	Standby (I_{SB})
L	L	H	L	L	Data Out	Data Out	Read – All bits	Active (I_{CC})
			L	H	Data Out	High Z	Read – Lower bits only	Active (I_{CC})
			H	L	High Z	Data Out	Read – Upper bits only	Active (I_{CC})
L	X	L	L	L	Data In	Data In	Write – All bits	Active (I_{CC})
			L	H	Data In	High Z	Write – Lower bits only	Active (I_{CC})
			H	L	High Z	Data In	Write – Upper bits only	Active (I_{CC})
L	H	H	X	X	High Z	High Z	Selected, Outputs Disabled	Active (I_{CC})
L	X	X	H	H	High Z	High Z	Selected, Outputs Disabled	Active (I_{CC})

Ordering Information

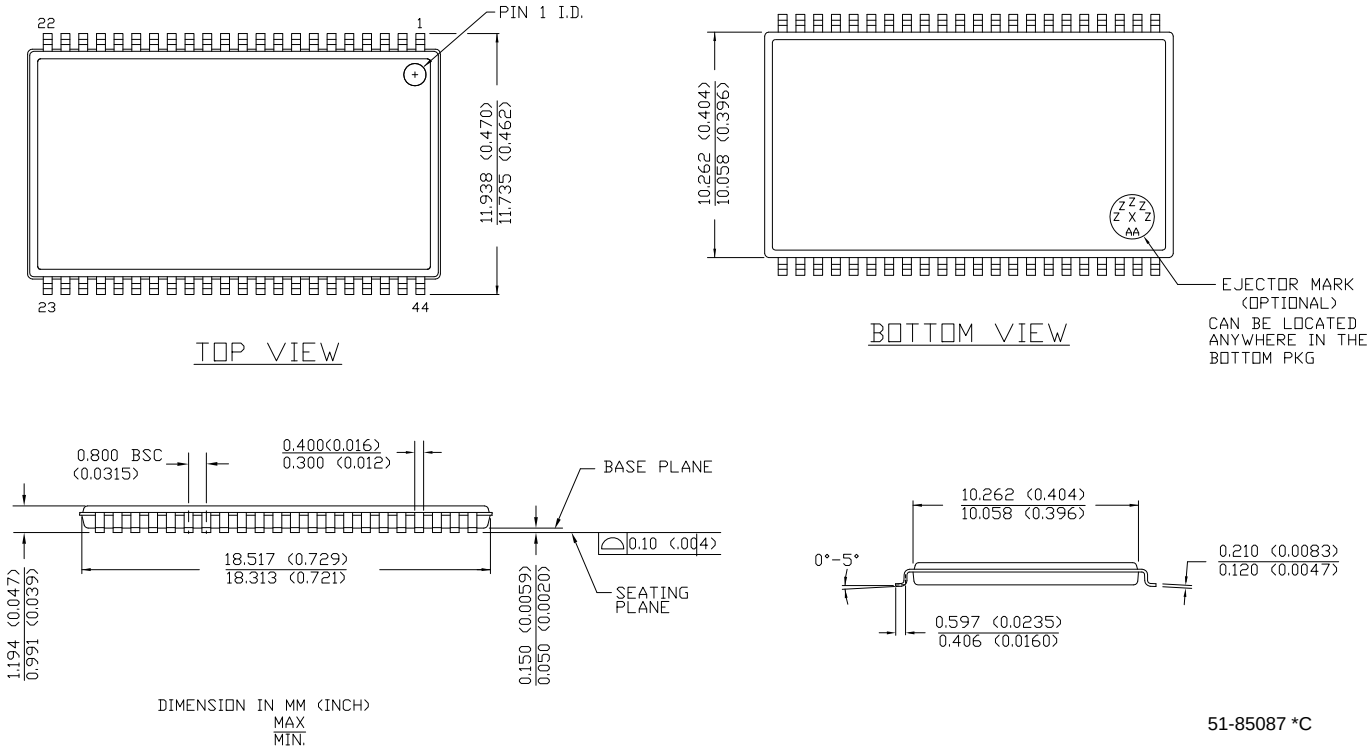
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C1020CV26-15ZSXE	Z44	44-pin TSOP Type II (Pb-free)	Automotive

Ordering Code Definitions



Package Diagrams

Figure 8. 44-Pin TSOP II



Document History Page

Document Title: CY7C1020CV26 512 Kb (32 K × 16) Static RAM Document Number: 38-05406				
REV.	**ECN NO.**	**Submission Date**	**Orig. of Change**	**Description of Change**
**	128060	07/30/03	EJH	Customized data sheet to meet special requirements for CG5988AF Automotive temperature range: –40°C / +125°C
*A	352999	See ECN	SYT	Removed ‘CG5988AF’ from the Datasheet Edited the features section for better structure on Page 1 Edited the title to include the mention of ‘512Kb’
*B	2903127	04/01/2010	VIVG	Updated template. Updated package diagram. Added Sales, Solutions, and Legal Information.
*C	3109992	12/14/2010	AJU	Added Ordering Code Definitions.
*D	3346414	08/16/2011	RAME	Update Ordering Code Definitions

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

Automotive	cypress.com/go/automotive
Clocks & Buffers	cypress.com/go/clocks
Interface	cypress.com/go/interface
Lighting & Power Control	cypress.com/go/powerpsoc cypress.com/go/plc
Memory	cypress.com/go/memory
Optical & Image Sensing	cypress.com/go/image
PSoC	cypress.com/go/psoc
Touch Sensing	cypress.com/go/touch
USB Controllers	cypress.com/go/USB
Wireless/RF	cypress.com/go/wireless

PSoC Solutions

psoc.cypress.com/solutions

PSoC 1 | PSoC 3 | PSoC 5

© Cypress Semiconductor Corporation, 2003-2011. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.

All products and company names mentioned in this document may be the trademarks of their respective holders.