DSC-11524

16-BIT HYBRID D/S AND D/R CONVERTER PIN PROGRAMMABLE FOR SYNCHRO OR RESOLVER OUTPUT

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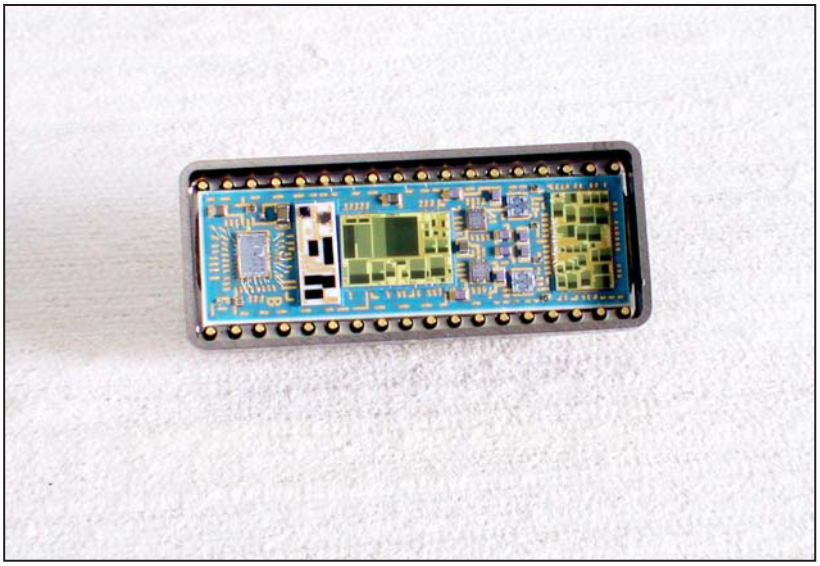

DESCRIPTION

The DSC-11524 is a versatile multiplying Digital-to-Synchro/Resolver converter. The digital input represents an angle, and the output is pin programmable for either Resolver, SIN/COS, or three-line synchro type output. The reference input will accept any waveform, even a sawtooth for CRT drive. Because the reference is DC coupled to the output, the DSC-11524 can be used in many configurations, such as: a Digital-to-Synchro/Resolver converter using a sinusoidal reference as an input; a Digital-to-SIN/COS DC converter using a DC reference; a polar-to-rectangular converter using a reference input proportional to the radius vector; a rotating cartwheel sweep generator for PPI displays using a sawtooth reference.

Packaged in a 36-pin DDIP, the DSC-11524 is a complete D/S and D/R converter in one hybrid module. Hybrid technology results in low weight, low power consumption, very high reliability, and a wide operating temperature range. The DSC-11524 circuit design allows for higher accuracy and reduces the output scale factor variation so that the output can drive displays directly. The output line-to-line voltage can be scaled by external resistors. Other features include high AC and DC common mode rejection at the reference input, and output short circuit protection.

APPLICATIONS

Because of its high reliability, small size and low power consumption the hybrid DSC-11524 is ideal for the most stringent and severe industrial and military ground or avionics applications. All units are available with MIL-PRF-38534 processing as a standard option.

Among the many possible applications are computer-based systems in which digital information is processed, such as simulators, flight trainers, flight instrumentation, fire control systems, radar and navigation systems, and PPI displays including moving target indicators.

FEATURES

- 15 mA RMS Output
- 11.8 V_{L-L} Synchro, 11.8 V_{L-L} Resolver, or 6.81 V_{L-L} Resolver Output
- 8 Bit/2 Byte Double-Buffered Transparent Latches
- Pin Programmable for Synchro or Resolver Output
- 16-Bit Resolution
- Complete D/S and D/R Converter
- Mate to DSC-36020 IBM® PC Card
- DC-Coupled Reference Accepts Any Waveform
- Generates SIN/COS DC or Rotating PPI Sweep
- High-Rel CMOS D/R Chip
- No +5 V Supply Required
- LVDT Simulation

DDC® Data Device Corporation

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1-800-DDC-5757 ext. 7771

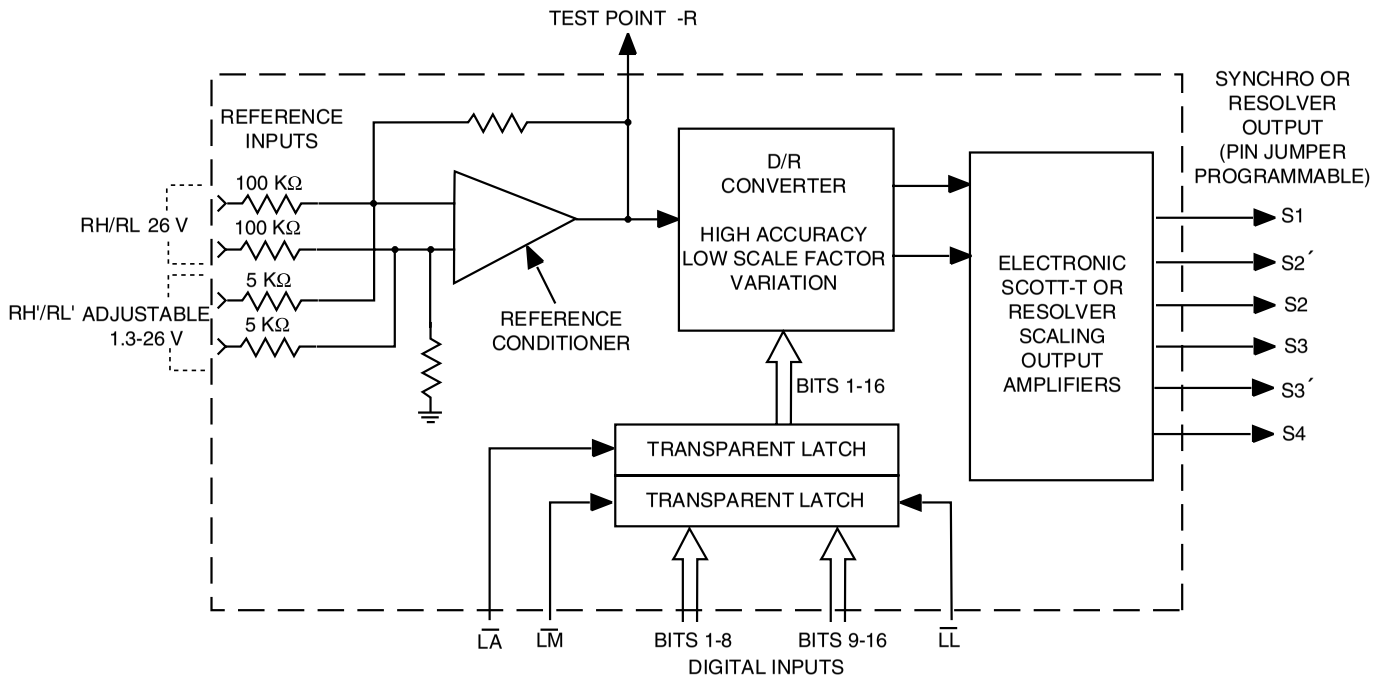


FIGURE 1. DSC-11524 BLOCK DIAGRAM

TABLE 1. DSC-11524 SPECIFICATIONS
Apply over temperature range, power supply range, reference voltage and frequency range, and 10% harmonic distortion in the reference.

PARAMETER	UNIT	VALUE	
RESOLUTION	Bits	16	
ACCURACY and DYNAMICS			
Output Accuracy	Minutes	±4 to ±2 min. (See Ordering Information.)	
Differential Linearity	LSB	±1 max	
Output Setting Time	µsec	Less than 20 for any digital step change	
DIGITAL INPUT			
Logic Type		Natural binary angle, parallel positive logic CMOS and TTL compatible. Inputs are CMOS transient protected.	
Logic Voltage Level		Logic 0 = 0 to +0.8 V Logic 1 = 2 V to 1/3 of V_{DD} +10%	
Load Current	µA	20 max (bits 1-16) 65 max ($\overline{LL}$, $\overline{LM}$, $\overline{LA}$) See Timing Diagrams (FIGURES 2A/2B.).	
REFERENCE INPUT			
Type		Two differential solid-state inputs: one for standard 26 V, one programmable.	
Frequency Range	Hz	DC to 1k	
		Standard Input	**Programmable Input**
Voltage	V	26 (Note 1)	1.3 minimum for full output; higher voltages are scaled by adding two series resistors
Input Impedance			
■Single Ended	k ohm	100 ±0.5%	5 ±0.5%
■Differential	k ohm	200 ±0.5%	10 ±0.5%
ANALOG OUTPUT			
Type		Pin programmable for synchro or resolver	
Output Current	mA rms	15 max	
Output Voltage		(Tracks Reference Input Voltage)	
■Synchro mode	$Vrms_{L-L}$	11.8 nominal	
■Resolver mode	$Vrms_{L-L}$	6.81 or 11.8 nominal	
Transform. Ratio Tol.	%	±0.5 max	
Scale Factor Varation	%	±0.1 max	
DC Offset (Each Line to Gnd)	mV	±15 max. Varies with input angle.	
POWER SUPPLIES			
Voltage	V	+15 ± 5%	-15 ± 5%
Max voltage without damage		+18 V	-18 V
Max Current or Impedance	mA	35+ load current	35+ load current
TEMPERATURE RANGES (CASE)			
Operation			
■-1 Option	°C	-55 to +125	
■-3 Option	°C	0 to +70	
Storage	°C	-55 to +135	
PHYSICAL CHARACTERISTICS			
Type		36-pin DDIP	
Size	in.(mm)	0.78 x 1.9 x 0.21 (19.7 x 48.3 x 5.3)	
Weight	oz. (g)	0.85 (24)	

Notes: 1) Maximum reference input voltage for RH/RL is 26 V +10%.
2) Differential is Line-to-Line (L-L); single-ended is Line-to-Ground (L-Gnd).

INTRODUCTION

As shown in FIGURE 1, the signal conversion in the DSC-11524 is performed by a high-accuracy Digital-to-Resolver converter whose SIN and COS outputs have a low scale factor variation as a function of the digital input angle. This resolver output is either amplified by scaling amplifiers for resolver output, or is both amplified and converted to a synchro output by an electronic Scott-T. In both cases the output line currents can be 15 mA rms max, which is sufficient for driving S/D converters, solid-state control transformers and displays. Output power amplifiers will be required, however, for driving electromechanical devices such as synchros and resolvers.

The reference conditioner has a differential input with high ac and DC common mode rejection, so that a reference isolation transformer will seldom be required. There are two sets of reference inputs. The RH, RL input provides the maximum synchro or resolver output voltage for a standard 26 V rms reference input. The RH´, RL´ input is used to scale the output for other reference voltage levels. Series resistors can be added to the reference input as described below, either to accommodate higher reference levels, or to reduce the output level. The reference conditioner output -R is intended for test purposes. A signal between 6 V and 7.5 V at -R indicates that a reference input signal is present.

DIGITAL INPUT

The converter contains three input latches. The input is controlled by $\overline{LM}$ and $\overline{LL}$. Each of these enable the converter to interface with an 8-bit bus. $\overline{LM}$ controls bits 1-8 and $\overline{LL}$ controls bits 9-16. Ensure that the data is stable for 50ns before enabling a latch ($\overline{LL}$, $\overline{LM}$), and allow 100ns for the latch to input the data.

Input Bit Weights are as follows:
BIT 1, MSB = 180 degrees
Bit 16, LSB = 0.0054 degrees (See Table 2)

POWER SUPPLY CYCLING

Power supply cycling of the DDC converter should follow the guidelines below to avoid any potential problems.

Strictly maintain proper sequencing of supplies and signals per typical CMOS circuit guidelines:
- Apply power supplies first (+15V, -15V and Ground).
- Apply analog signals last.

The reverse sequence should be followed during power down of the circuit.

TABLE 2. ANGLES IN DEGREES CROSS REFERENCED TO A 16-BIT DIGITAL WORD

DEGREES (HEX)	16 BIT DIGITAL WORD (Φ) (1 = MSB, 16 = LSB)															
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
0° (0000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15° (0AAB)	0	0	0	0	1	0	1	0	1	0	1	0	1	0	1	1
30° (1555)	0	0	0	1	0	1	0	1	0	1	0	1	0	1	0	1
45° (2000)	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
60° (2AAB)	0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	1
75° (3666)	0	0	1	1	0	1	0	1	0	1	0	1	0	1	0	1
90° (4000)	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
120° (5555)	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
135° (6000)	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
180° (8000)	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
240° (AAAB)	1	0	1	0	1	0	1	0	0	0	1	0	1	0	1	1
270° (C000)	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
285° (CAAB)	1	1	0	0	1	0	1	0	1	0	0	0	1	0	1	1
300° (D555)	1	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
315° (E000)	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
330° (EAAB)	1	1	1	0	1	0	1	0	1	0	1	0	1	0	1	1
345° (F555)	1	1	1	1	0	1	0	1	0	1	0	1	0	1	0	1
359° (FFFF)	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

OUTPUT SCALING AND REF LEVEL ADJUSTMENT

The DSC-11524 operates like a multiplying D/A converter in that the voltage of each output line is directly proportional to the reference voltage. The maximum line-to-line levels are determined by the output amplifiers and are nominally 11.8 V for synchro output and 6.81 V or 11.8 V for resolver output. The RH, RL reference input is designed to provide this nominal output for the standard 26 V reference level. The scaling adjustment is made by two internal 100k ohm resistors in series with the reference conditioner input (see FIGURE 1).

The RH´, RL´ reference input has only 5k ohm internal resistors in series with the reference conditioner input, so that nominal line-to-line output is obtained for a reference input of 1.3 V. For higher reference voltages, two resistors, R', must be inserted in series with the inputs. These resistors scale the DSC-11524 to accommodate higher reference levels, or to reduce the output levels. The magnitude of the resistors, R´, in ohms is calculated as follows:

$$R' = \frac{5K}{1.3}\left(V_{RH'\,RL'} \times \left[\frac{\text{NOM } V_{LL}}{\text{DESIRED } V_{LL}}\right] - 1.3\right)$$

$V_{RH'\,RL'}$ = Reference Input Voltage to Pins 11 & 9

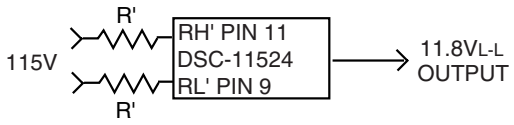
NomV_{LL} = Analog Output Voltage (L-L) Configuration as per Figure 4

Desired V_{LL} = Scaled Analog Output Voltage

Example to scale reference input RH'/RL' to 115 Vrms
(Configured for 11.8V nominal output)

$$R' = \frac{5K}{1.3}\left(115 \times \left[\frac{11.8}{11.8}\right] - 1.3\right)$$

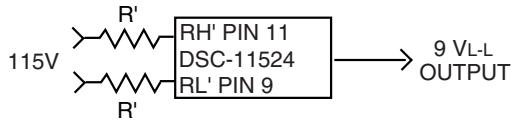
$R' \approx 437K\Omega$



Example to scale Output Voltage line-to-line of 9 volts
(Configured for 115V Reference Input)

$$R' = \frac{5K}{1.3}\left(115 \times \left[\frac{11.8}{9}\right] - 1.3\right)$$

$R' = 575\ K\Omega$



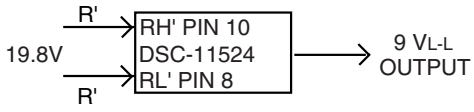
Output Voltage Scaling without external R' resistors.

The Output Voltage can be scaled down from the nominal voltage L-L. Input/Output ratio is 0.45 for the RH/RL 26V Reference Input.

Example to scale a 9V L-L Output using the 26V RH/RL Reference Voltage on Input pins 10 & 8.

$$\text{REF INPUT VOLTAGE} = \frac{\text{Desired Output (L-L)}}{0.45} = \frac{9}{0.45}$$

REF INPUT VOLTAGE = 19.8V



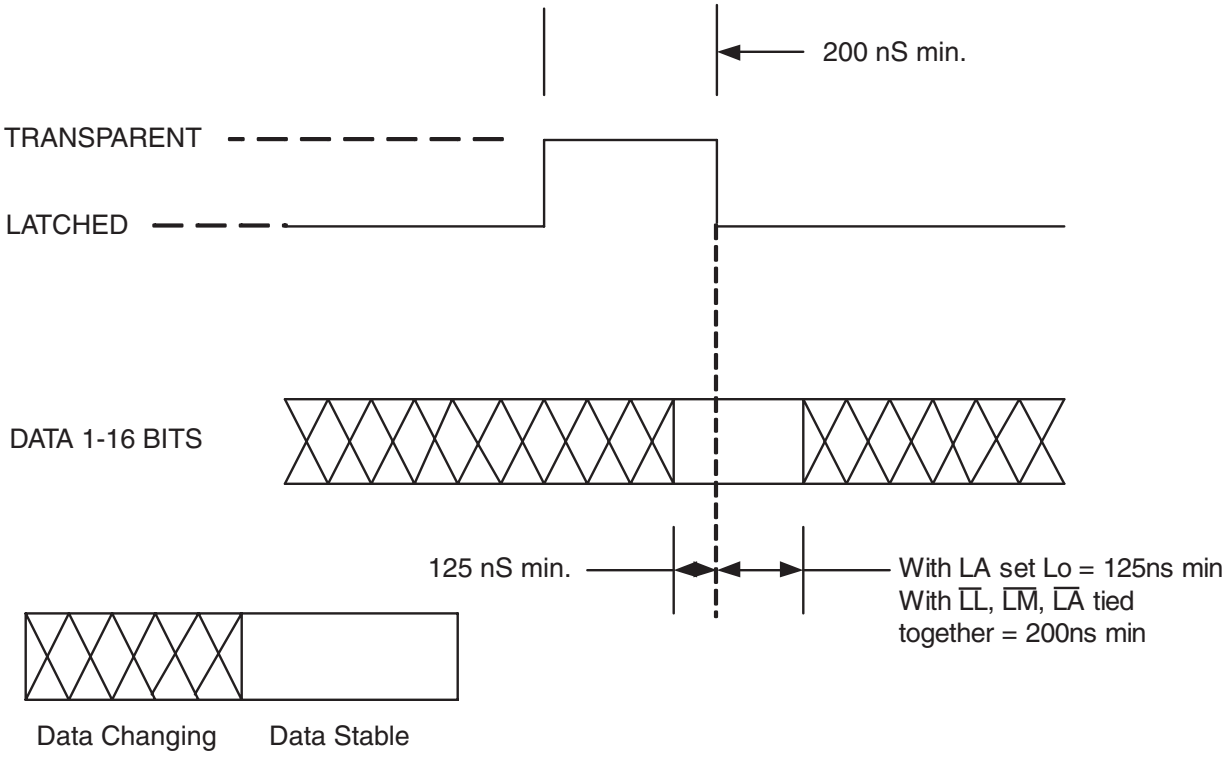


FIGURE 2A. $\overline{LL}$, $\overline{LM}$, $\overline{LA}$ TIMING DIAGRAM (16-BIT)

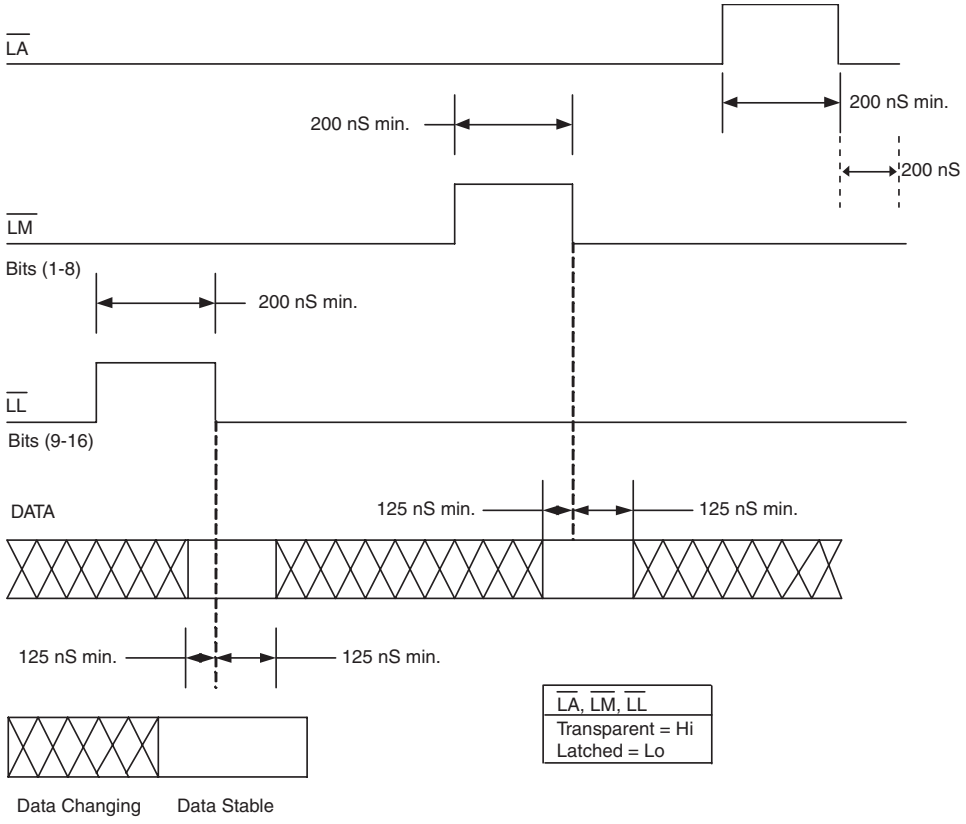


FIGURE 2B. $\overline{LL}$, $\overline{LM}$, $\overline{LA}$ TIMING DIAGRAM (8-BIT)

OUTPUT CONFIGURATION

The output amplifier section can be configured for Synchro and Resolver outputs, as shown in FIGURE 3.

OUTPUT PHASING AND OUTPUT SCALE FACTOR

The analog output signals have the following phasing:

Synchro output:
S3—S1 = (RH - RL)A_o(1 + A(θ)) sin θ
S2—S3 = (RH - RL)A_o(1 + A(θ)) sin(θ + 120°)
S1—S2 = (RH - RL)A_o(1 + A(θ)) sin(θ + 240°)

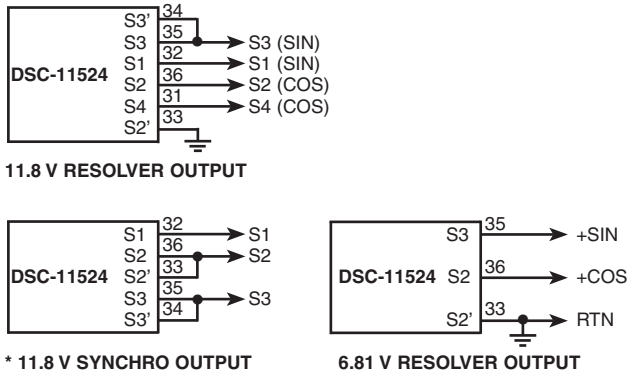
Resolver output:
S3—S1 = (RH - RL)A_o(1 + A(θ)) sin θ
S2—S4 = (RH - RL)A_o(1 + A(θ)) cos θ

The output amplifiers simultaneously track reference voltage fluctuations because they are proportional to (RH - RL). The transformation ratio A_o is 11.8/26 for 11.8 V rms L-L output. The maximum variation in A_o from all causes is ± 0.5%. The term A(θ) represents the variation of the amplitude with the digital signal input angle. A(θ), which is called the scale factor variation, is a smooth function of (θ) without discontinuities and is less than ±0.1% for all values of (θ). The total maximum variation in A_o(1 + A(θ)) is therefore ± 0.6%.

Because the amplitude factor (RH - RL)A_o(1 + A(θ)) varies simultaneously on all output lines, it will not be a source of error when the DSC-11524 is to drive a ratiometric system such as a synchro or resolver. However, if the outputs are used independently, as in x-y plotters, the amplitude variations must be taken into account.

OUTPUT TRANSFORMER

The DSC-11524 uses the 51538 step-up transformer to drive 90 V_{L-L} synchro loads. The 51538 transformer specifications are shown in TABLE 3 and the schematic and mechanical outline drawings are shown in FIGURE 4.



*For S2(z) grounded applications use Beta transformer P/N 42929, Synchro-to-Synchro, 11.8v to 11.8v 400 Hz.

FIGURE 3. OUTPUT PIN PROGRAMMING

TABLE 3. ELECTRICAL SPECIFICATIONS FOR THE 51538 TRANSFORMER	
Synchro Input	11.8 Vrms line-to-line ±10% at 400 Hz ±10%
Synchro Output	90 Vrms ±1% Full Scale with a line-to-line input voltage of 11.8 Vrms
Input Impedance	1000 Ohms minimum
Output Impedance	500 Ohms maximum
Accuracy	The maximum additional error shall be 1.5 min. loaded with an SDC-14560 (130k Ohm)
HIPOT	Between windings and windings-to-case 900 Vrms at 60 Hz

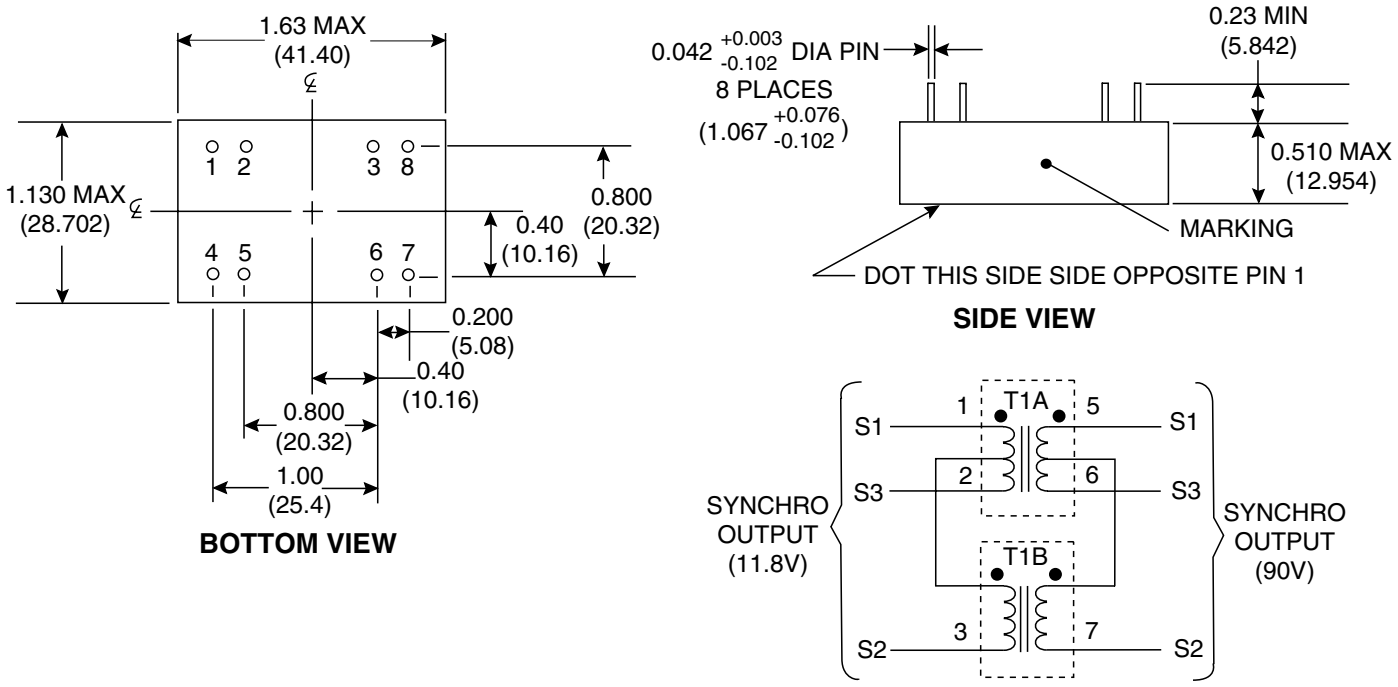
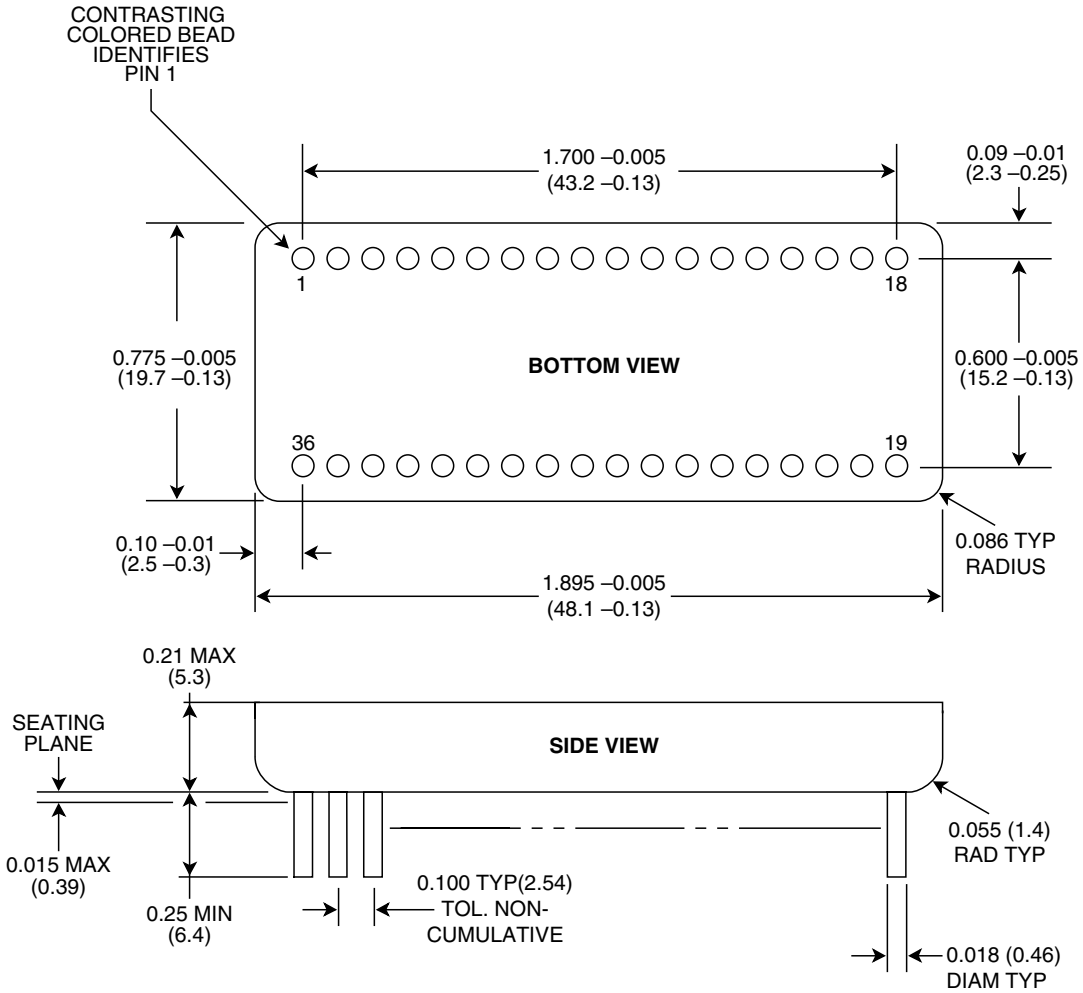


FIGURE 4. 90 V_{L-L}, 400 HZ SYNCHRO OUTPUT TRANSFORMER (P/N 51538)

TABLE 4. PIN CONNECTION TABLE					
PIN	**NAME**	**PIN**	**NAME**	**PIN**	**NAME**
1	NC	13	Bit 13	25	Bit 1 (MSB)
2	+15V	14	Bit 12	26	Bit 15
3	GND	15	Bit 11	27	Bit 16 (LSB)
4	-15V	16	Bit 10	28	$\overline{LM}$
5	NC	17	Bit 9	29	$\overline{LL}$
6	NC	18	Bit 8	30	$\overline{LA}$
7	-R	19	Bit 7	31	S4
8	RL	20	Bit 6	32	S1
9	RL´	21	Bit 5	33	S2'
10	RH	22	Bit 4	34	S3'
11	RH´	23	Bit 3	35	S3 (+SIN)
12	Bit 14	24	Bit 2	36	S2 (+COS)

Notes:
1. -R (Pin 7) can be used for test purposes to detect whether a reference signal is present. See block diagram.
2. Functions $\overline{LL}$, $\overline{LA}$, and $\overline{LM}$ may be left unconnected when not used.
3. NC, Means no internal wire connection.



Notes:
1. Dimensions shown are in inches (millimeters).
2. Lead identification numbers are for referenced only.
3. Lead cluster shall be centered within of outline dimensions. Lead spacing dimensions apply only at seating plane.
4. Pin material meets solderability requirements of MIL-STD-202E, Method 208C.
5. Package is Kovar with electroless nickel plating.
6. Case is electrically floating.

FIGURE 5. DSC-11524 36-PIN DDIP MECHANICAL OUTLINE

LVDT SIMULATION

To test an LVDT application using a Synchro/Resolver simulator, the angular bit weights of the R/D converter, in the linear mode, are modified as follows (Also see Table 5):

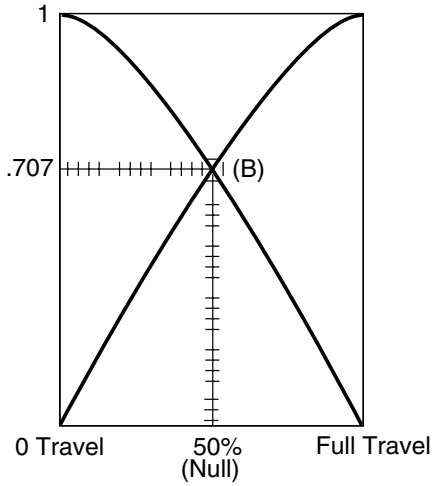
BIT 3: 0.5/0.5 = 1 Arc Tan (1) = 45°

BIT 4: 0.25/0.75 = 0.333 Arc Tan (0.333) = 18.435°

BIT 5: 0.125/0.875 = 0.143 Arc Tan (0.143) = 8.130°

TABLE 5. ANGULAR BIT WEIGHTS FOR LVDT SIMULATION

DATA BIT ON	ANGLE	% OF FULL TRAVEL
3	45°	.5(Center Null Point)
4	18.435°	0.333
5	8.130°	0.143
6	3.814°	0.0667
7	1.848°	0.03226
8	0.911°	0.01587
9	0.451°	0.00787
10	0.225°	0.00392
11	0.112°	0.00196
12	0.056°	0.00098
13	0.028°	0.00049
14	0.014°	0.00024
15	0.007°	0.00012
16	0.0035°	0.00006



B=D/R output simulating 50% travel
Sum = .707 + .707 = 1.4

FIGURE 6. LVDT OUTPUT

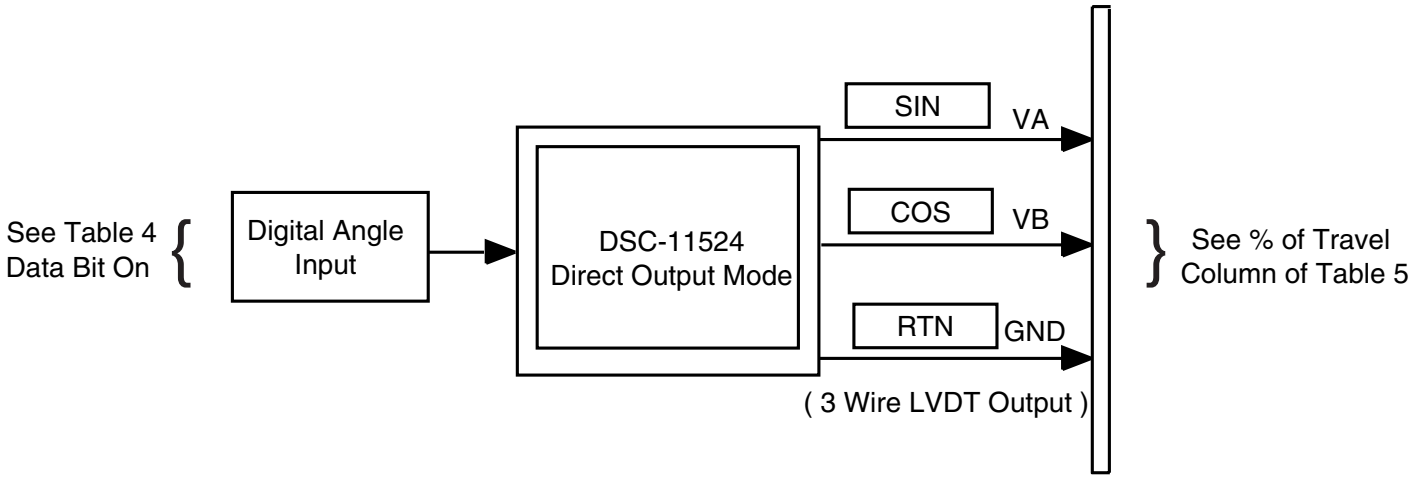


FIGURE 7. LVDT SIMULATION

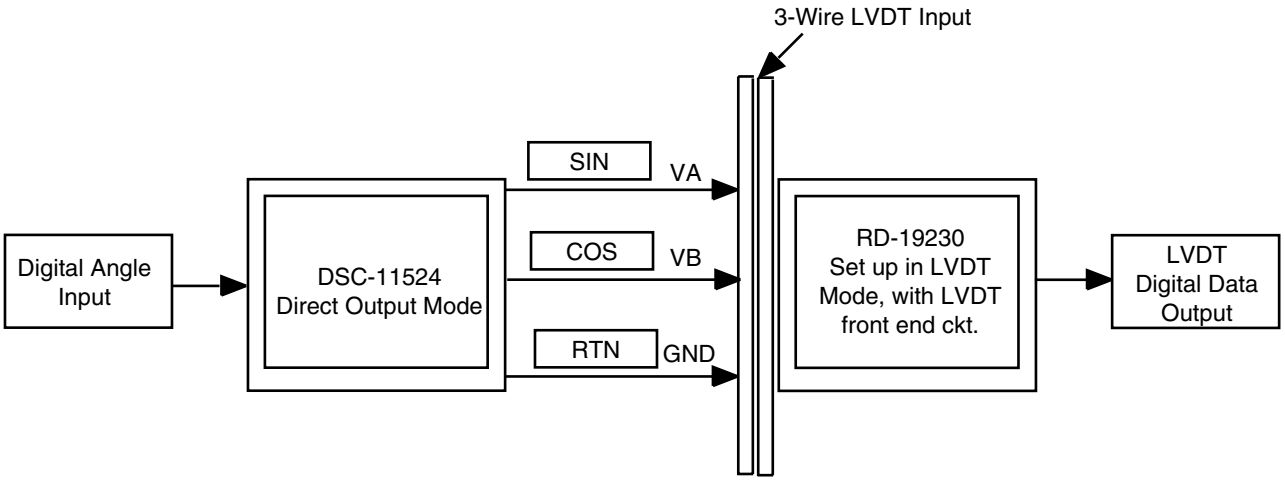


FIGURE 8. CONNECTING TO AN RD-19230FX CONVERTER

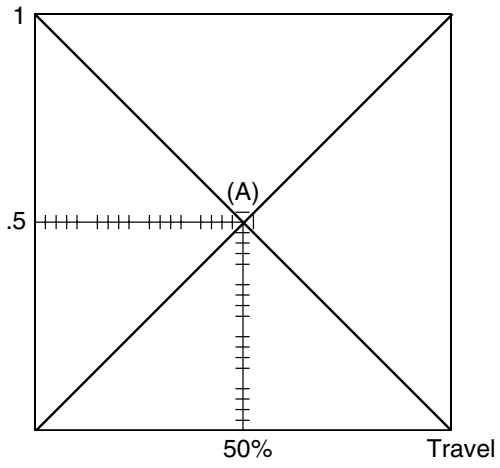
TABLE 6. DIGITAL OUTPUT OF RD-19230FX

LVDT OUTPUT	RD-19230FX OUTPUT															
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
+ OVER FULL SCALE	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X
+ FULL TRAVEL - 1LSB	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
+0.5 TRAVEL	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
+1 LSB	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1
NULL	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
- 1 LSB	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1
- 0.5 TRAVEL	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
- FULL TRAVEL	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
- OVER FULL SCALE	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X
	Full Scale	MSB							LSB's 8 Bit		LSB's 10 Bit		LSB's 12 Bit		LSB's 14 Bit	

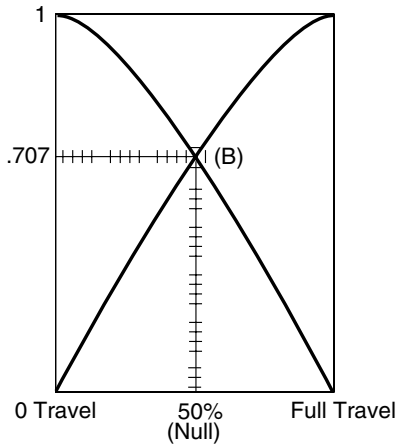
Use Table 6 to read RD-19230FX outputs and relate to LVDT movement.

Note: See the RD/RDC MN-19220XX application manual for LVDT to digital conversion theory. These can be downloaded from our Website www.ddc-web.com.

Note: 2-wire LVDT outputs when summed equal a constant. The DSC-11524 SIN & COS when summed will not be a constant. Therefore to minimize RD-19230 gain effects full scale (i.e. 90° or 0° input to D/R) at the R-to-D should be ≈ 1.7 Vrms instead of 2 Vrms only when using a D-R converter for testing.



A = LVDT output when @ 50% travel
Sum = .5 + .5 = 1



B=D/R output simulating 50% travel
Sum = .707 + .707 = 1.4

Note: A feedback circuit using the SIN & COS sum to adjust RH-RL gain can be used to overcome this gain issue.

FIGURE 9. LVDT OUTPUT VS D/R LVDT SIMULATION OUTPUT

ORDERING INFORMATION

DSC-11524-XXXX

Supplemental Process Requirements:
- S = Pre-Cap Source Inspection
- L = Pull Test
- Q = Pull Test and Pre-Cap Inspection
- K = One Lot Date Code
- W = One Lot Date Code and Pre-Cap Source
- Y = One Lot Date Code and 100% Pull Test
- Z = One Lot Date Code, Pre-Cap Source and 100% Pull Test
- Blank = None of the Above

Accuracy:
- 3 = ±4 minutes
- 4 = ±2 minutes

Process Requirements:
- 0 = Standard DDC Processing, no Burn-In (See table below.)
- 1 = MIL-PRF-38534 Compliant
- 2 = B[1]
- 3 = MIL-PRF-38534 Compliant with PIND Testing[2]
- 4 = MIL-PRF-38534 Compliant with Solder Dip[2]
- 5 = MIL-PRF-38534 Compliant with PIND Testing and Solder Dip[2]
- 6 = B[1] with PIND Testing
- 7 = B[1] with Solder Dip
- 8 = B[1] with PIND Testing and Solder Dip
- 9 = Standard DDC Processing with Solder Dip, no Burn-In (See table below.)

Temperature Grade/Data Requirements:
- 1 = -55°C to +125°C
- 2 = -40°C to +85°C
- 3 = 0°C to +70°C
- 4 = -55°C to +125°C with Variables Test Data
- 5 = -40°C to +85°C with Variables Test Data
- 8 = 0°C to +70°C with Variables Test Data

1. Standard DDC Processing with burn-in and full temperature test — see table below.

2. MIL-PRF-38534 product grading is designated with the following dash numbers:
   Class H is a -11X, 13X, 14X, 15X, 41X, 43X, 44X, 45X
   Class G is a -21X, 23X, 24X, 25X, 51X, 53X, 54X, 55X
   Class D is a -31X, 33X, 34X, 35X, 81X, 83X, 84X, 85X

These products contain tin-lead solder finish as applicable to solder dip requirements.

STANDARD DDC PROCESSING FOR HYBRID AND MONOLITHIC HERMETIC PRODUCTS

TEST	MIL-STD-883	
	METHOD(S)	CONDITION(S)
INSPECTION	2009, 2010, 2017, and 2032	—
SEAL	1014	A and C
TEMPERATURE CYCLE	1010	C
CONSTANT ACCELERATION	2001	3000g
BURN-IN	1015 (note 1), 1030 (note 2)	TABLE 1

Notes:
1. For Process Requirement "B*" (refer to ordering information), devices may be non-compliant with MIL-STD-883, Test Method 1015, Paragraph 3.2. Contact factory for details.
2. When applicable.

The information in this data sheet is believed to be accurate; however, no responsibility is assumed by Data Device Corporation for its use, and no license or rights are granted by implication or otherwise in connection therewith.
Specifications are subject to change without notice.

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