HARRIS SEMICONDUCTOR

HS-6551RH

Radiation Hardened 256 x 4 CMOS RAM

December 1992

Features

- Functional Total Dose 2×10^4 RAD(Si)
- Latch-Up Free To > 5.0×10^{11} RAD(Si)/s
- Data Upset > 10^8 RAD(Si)/s
- Low Standby Power 550µW Max.
- Low Operating Power 22mW/MHz Max.
- Fast Access Time 300ns Max. 160ns Typ.
- TTL Compatible Outputs
- High Output Drive - 1 TTL Loads
- High Noise Immunity
- On-Chip Address Register
- Three-State Outputs
- 22 Pin Package for High Density
- Military Temperature Range -55°C to +125°C

Description

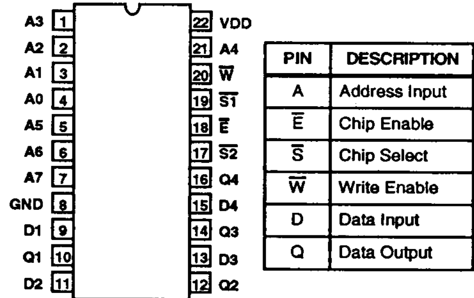
The HS-6551RH is a 256 by 4 static CMOS RAM fabricated using the Harris radiation hardened self-aligned silicon gate technology. Synchronous circuit design techniques are employed to achieve high performance and low power operation. Latch-up free operation is achieved by the use of epitaxial starting material to eliminate the parasitic SCR effect seen in conventional bulk CMOS devices.

On-chip latches are provided for addresses, and data outputs allowing efficient interfacing with microprocessor systems. The data output buffers can be forced to a high impedance state for use in expanded memory arrays.

The HS-6551RH is a fully static RAM and may be maintained in any state for an indefinite period of time.

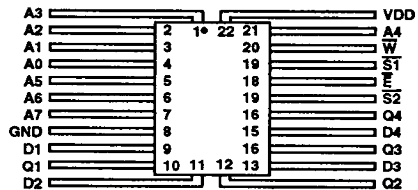
Pinouts

HS1-6551RH 22 PIN CERAMIC DIP
CASE OUTLINE D7, CONFIGURATION 3
TOP VIEW

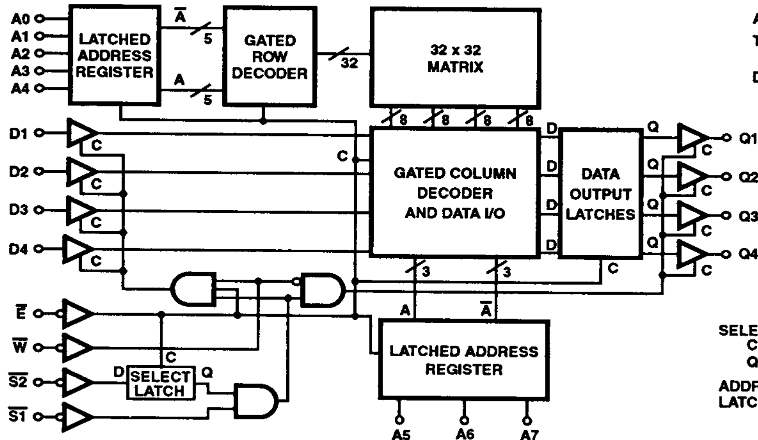


PIN	DESCRIPTION
A	Address Input
Ē	Chip Enable
S̄	Chip Select
W̄	Write Enable
D	Data Input
Q	Data Output

HS9-6551RH 22 PIN FLATPACK
INTERNAL PACKAGE CODE "HRE"



Functional Diagram



ALL LINES POSITIVE LOGIC-ACTIVE HIGH
THREE STATE BUFFERS:
C HIGH → OUTPUT ACTIVE
DATA LATCHES:
C HIGH → Q = D
Q LATCHES ON FALLING EDGE OF C

SELECT LATCH:
C LOW → Q = D
Q LATCHES ON RISING EDGE OF C
ADDRESS LATCHES AND DECODERS LATCH AND GATE ON RISING EDGE OF C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

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Absolute Maximum Ratings

Supply Voltage (VDD) .... -0.3 to +7.0V
Input, Output or I/O Voltage .... GND-0.3V to VDD+0.3V
Storage Temperature Range .... -65°C to +150°C
Junction Temperature .... +175°C
Lead Temperature (Soldering 10s) .... +300°C
Typical Derating Factor .... 1.5mA/MHz Increase in IDDOP
ESD Classification .... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	73.9°C/W	11.3°C/W
Ceramic Flatpack Package	69.8°C/W	12.2°C/W

Maximum Package Power Dissipation at +125°C
Ceramic DIP Package 0.67W
Ceramic Flatpack Package 0.72W
Gate Count .... 1841 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range .... +4.5V to +5.5V
Operating Temperature Range .... -55°C to +125°C
Input Rise and Fall Time .... 40ns Max

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	LIMITS		UNITS
			MIN	MAX	
Standby Supply Current	IDDSB	IO = 0, VI = VDD or GND	-	100	µA
Operating Supply Current (Note 1)	IDDOP	f = 1MHz, IO = 0, VI = VDD or GND	-	4	mA
Input Leakage Current	II	GND ≤ VI ≤ VDD	-1.0	+1.0	µA
Output Leakage Current	IOZ	GND ≤ VI ≤ VDD	-1.0	+1.0	µA
Output High Voltage	VOH	IOH = -1.0mA	2.4	-	V
Output Low Voltage	VOL	IOL = 2.0mA	-	0.4	V
Input High Voltage	VIH		VDD-2.0	VDD	V
Input Low Voltage	VIL		0.0	0.8	V

NOTE:

1. Operating Supply Current (IDDOP) is proportional to Operating Frequency. Example: Typical IDDOP = 1.5mA/MHz

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	LIMITS		UNITS
			MIN	MAX	
Chip Enable Access Time	TELQV	Note 1	-	300	ns
Address Access Time	TAVQV	Note 1	-	315	ns
Chip Enable Pulse Negative Width	TELEH	Note 1	300	-	ns
Chip Enable Pulse Positive Width	TEHEL	Note 1	150	-	ns
Address Setup Time	TAVEL	Note 1	15	-	ns
Chip Select 2 Setup Time	TS2LEL	Note 1	15	-	ns
Address Hold Time	TELAX	Note 1	70	-	ns
Chip Select 2 Hold Time	TELS2X	Note 1	70	-	ns
Data Setup Time	TDVWH	Note 1	180	-	ns
Data Hold Time	TWHDX	Note 1	0	-	ns
Chip Select 1 Write Pulse Setup Time	TWLS1H	Note 1	315	-	ns
Chip Enable Write Pulse Setup Time	TWLEH	Note 1	300	-	ns
Chip Select 1 Write Pulse Hold Time	TS1LWH	Note 1	195	-	ns
Chip Enable Write Pulse Hold Time	TELWH	Note 1	180	-	ns
Write Enable Pulse Width	TWLWH	Note 1	180	-	ns

NOTE:

1. Inputs - TRISE = TFALL ≤ 20ns; Outputs - 1 TTL load and 50pF. All timing measurements at $^1/_2$ VDD.

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TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Guaranteed, but not tested)

PARAMETER	SYMBOL	CONDITIONS	LIMITS		UNITS
			MIN	MAX	
Input Capacitance	CI	VI = VDD or GND, f = 1MHz	-	6	pF
Output Capacitance	CO	VI = VDD or GND, f = 1MHz	-	10	pF
Chip Select 1 Output Enable Time	TS1LQX	Note 1	-	150	ns
Write Enable Output Disable Time	TWLQZ	Note 1	-	150	ns
Chip Select 1 Output Disable Time	TS1HQZ	Note 1	-	150	ns
Read or Write Cycle Time	TELEL	Note 1	450	-	ns

NOTE:

1. Inputs - TRISE = TFALL ≤ 20ns; Outputs - 1 TTL load and 50pF. All timing measurements at $^1/_2$ VDD.

TABLE 4. POST RAD ELECTRICAL PERFORMANCE CHARACTERISTICS

DC PARAMETER	SYMBOL	CONDITIONS	TEMPERATURE	LIMITS		UNITS
				MIN	MAX	
Stand By Current	IDDSB	VDD = 5 ± 0.5V	+25°C	-	10	mA

NOTE:

1. Based on the average of the entire sample.

TABLE 5. BURN-IN DELTA PARAMETERS (+25°C)

PARAMETER	SYMBOL	DELTA LIMITS
Output Low Voltage	VOL	± 0.15V
Output High Voltage	VOH	± 0.40V
Output Leakage Current	IOZ	± 300nA
Stand By Current	IDDSB	± 30μA

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	-Q SUBGROUPS	-8 SUBGROUPS
Initial Test		100%/5004	1, 7, 9	1, 7, 9
Interim Test 1 and 2		100%/5004	1, 7, 9	N/A
PDA 1 and 2		100%/5004	1, 7, Δ	1, 7
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	2, 3, 8A, 8B, 10, 11
Group A		Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group B (Optional)	B5	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	N/A
	Others	Samples/5005	1, 7	N/A
Group C (Optional)		Samples/5005	N/A	1, 7
Group D (Optional)		Samples/5005	1, 7	1, 7
Group E, Subgroup 2		Samples/5005	1, 7, 9	1, 7, 9

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MEMORIES

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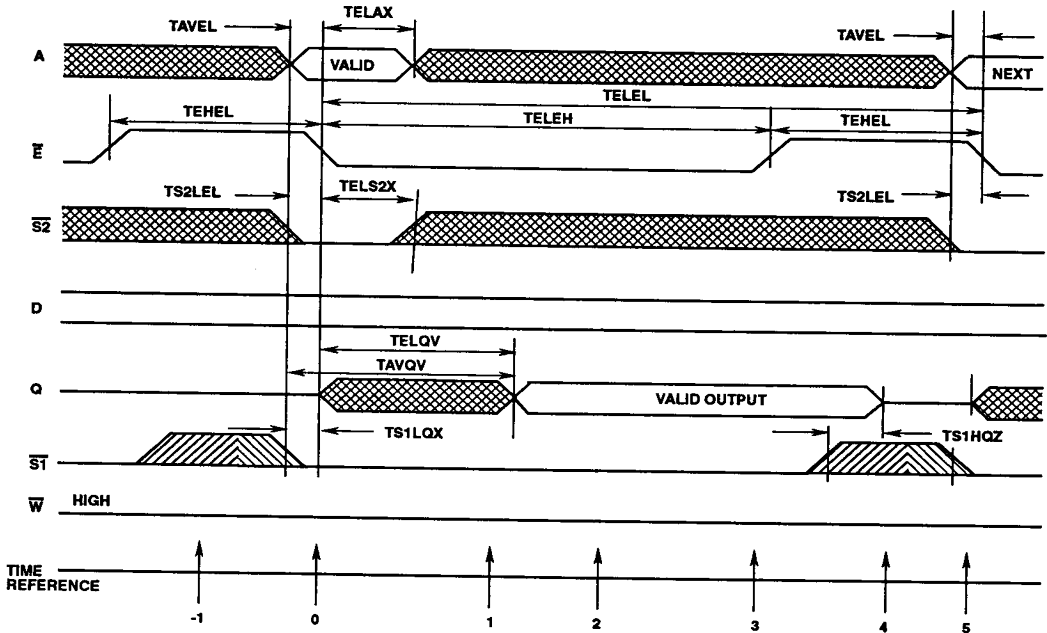
Timing Waveforms

READ CYCLE



TRUTH TABLE

TIME REFERENCE	INPUTS						OUTPUTS	FUNCTION
	$\overline{E}$	$\overline{S1}$	$\overline{S2}$	$\overline{W}$	A	D	Q	
-1	H	H	X	X	X	X	Z	Memory Disabled
0	↘	L	L	H	V	X	Z	Addresses and $\overline{S2}$ are Latched, Cycle Begins
1	L	L	X	H	X	X	X	Output Enabled but Undefined
2	L	L	X	H	X	X	V	Data Output Valid
3	↗	L	X	H	X	X	V	Outputs Latched, Valid Data
4	H	H	X	X	X	X	Z	Prepare for Next Cycle (Same as -1)
5	↘	X	L	H	V	X	Z	Cycle Ends, Next Cycle Begins (Same as 0)

The HS-6551RH Read Cycle is initiated by the falling edge of $\overline{E}$. This signal latches the input address word and $\overline{S2}$ into on chip registers providing the minimum setup and hold times are met. After the required hold time, these inputs may change state without affecting device operation. $\overline{S2}$ acts as a high order address and simplifies decoding. For the output to be read, $\overline{E}$, $\overline{S1}$ must be low and $\overline{W}$ must be high. $\overline{S2}$ must have been latched low on the falling edge of $\overline{E}$. The output data will be valid at access time (TELQV).

The HS-6551RH has output data latches that are controlled by $\overline{E}$. On the rising edge of $\overline{E}$ the present data is latched and remains in that state until $\overline{E}$ falls. Either or both $\overline{S1}$ or $\overline{S2}$ may be used to force the output buffers into a high impedance state.

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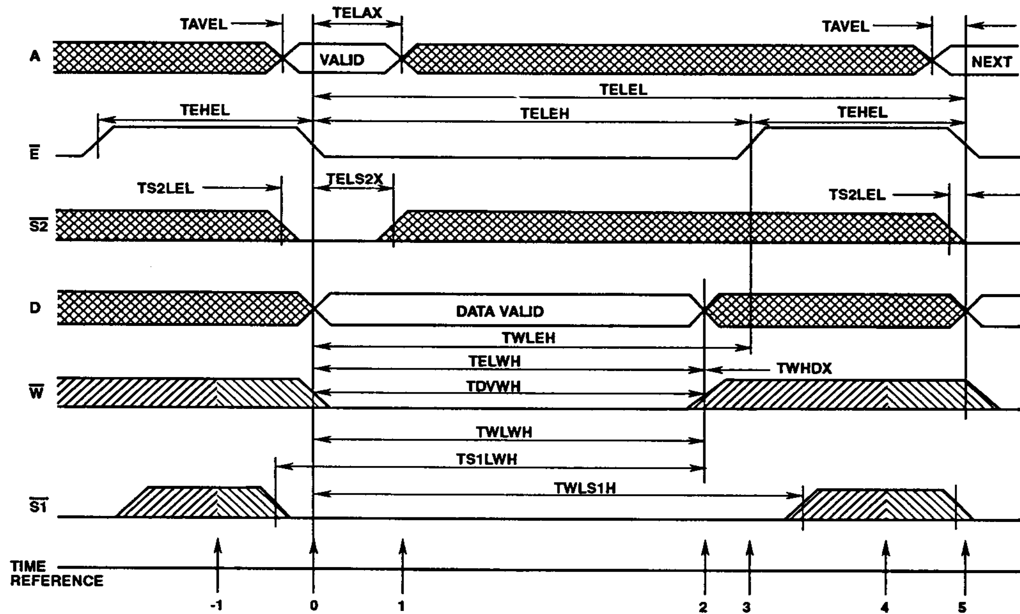
Timing Waveforms (Continued)

WRITE CYCLE



TRUTH TABLE

TIME REFERENCE	INPUTS						OUTPUTS	FUNCTION
	$\overline{E}$	$\overline{S1}$	$\overline{S2}$	$\overline{W}$	A	D	Q	
-1	H	H	X	X	X	X	Z	Memory Disabled
0	↘	L	L	↘	V	X	Z	Cycle Begins, Addresses and $\overline{S2}$ are Latched
1	L	L	X	L	X	V	Z	Write Period Begins
2	L	L	X	↗	X	X	Z	Data In is Written
3	↗	L	X	H	X	X	Z	Write is Completed
4	H	H	X	X	X	X	Z	Prepare for Next Cycle (Same as -1)
5	↘	X	L	X	V	X	Z	Cycle Ends, Next Cycle Begins (Same as 0)

In the Write Cycle the falling edge of $\overline{E}$ latches the addresses and $\overline{S2}$ into on chip registers. $\overline{S2}$ must be latched in the low state to enable the device. The write portion of the cycle is defined as $\overline{E}$, $\overline{W}$, $\overline{S1}$ being low and $\overline{S2}$ being latched low simultaneously. The $\overline{W}$ line may go low at any time during the cycle providing that the write pulse setup times (TWLEH and TWLS1H) are met. The write portion of the cycle is terminated on the first rising edge of either $\overline{E}$, $\overline{W}$, or $\overline{S1}$.

If a series of consecutive write cycles are to be executed, the $\overline{W}$ line may be held low until all desired locations have been written. If this method is used, data setup and hold times must be referenced to the first rising edge of $\overline{E}$ or $\overline{S1}$. By positioning the write pulse at different times within the $\overline{E}$ and $\overline{S1}$ low time (TELEH), various types of write cycles may be performed. If the $\overline{S1}$ low time (TS1LS1H) is greater than the $\overline{W}$ pulse plus an output enable time (TS1LQX), a combination read-write cycle is executed. Data may be modified an indefinite number of times during any write cycle (TELEH).

The HS-6551RH may be used on a common I/O bus structure by tying the input and output pins together. The multiplexing is accomplished internally by the $\overline{W}$ line. In the write cycle, when $\overline{W}$ goes low, the output buffers are forced to a high impedance state. One output disable time delay (TWLQZ) must be allowed before applying input data to the bus.

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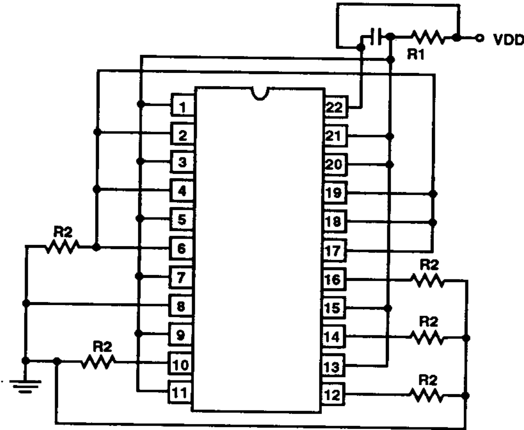
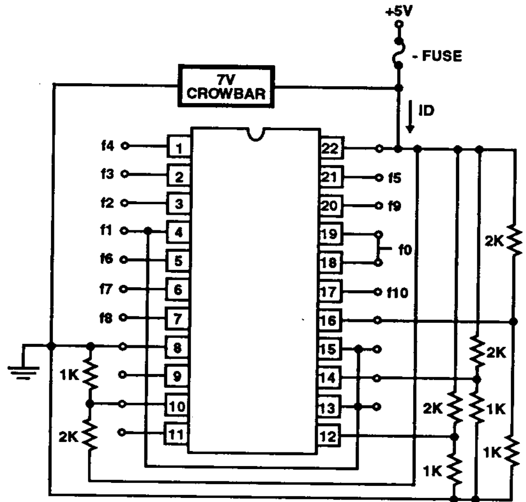
Burn-In Circuits



STATIC CONFIGURATION

NOTES:

VDD = 5.0V ± 10%
IDD + 1.5mA
R1 = 100K
R2 = 10k
Minimum Ambient Temperature = +125°C

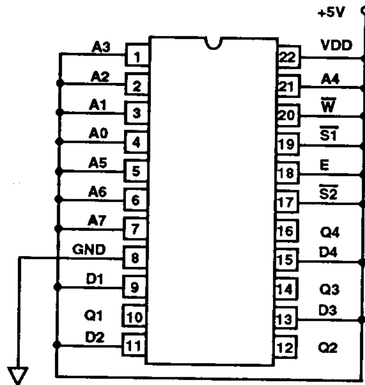


DYNAMIC CONFIGURATION

NOTES:

All resistors are ±20%, 1/4W
Use standard crowbar circuit with +7V zener diode
50% Duty Cycle square wave
IDMAX = 8mA/part
VIH = 4.0V, VIL = 0.8V
IL = ±1nA, CIN = 10pF
f0 = 500KHz; f1 = f0/2; f2 = f1/2; . . . f10 = f9/2

Irradiation Circuit



NOTES:

VDD = 5V
GND = 0V
All Inputs = 5V
All Q outputs float open

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Harris - Space Level (-Q) Product Flow (Note 1)

SEM - Traceable to Diffusion Method 2018
Wafer Lot Acceptance Method 5007
Internal Visual Inspection Method 2010, Condition A
Gamma Radiation Assurance Tests Method 1019
Nondestructive Bond Pull Method 2023
Customer Pre-Cap Visual Inspection (Note 2)
Temperature Cycling Method 1010, Condition C
Constant Acceleration Method 2001, Condition E Min, Y1
Particle Impact Noise Detection Method 2020, Condition A
Electrical Tests (Harris' Option)
Serialization
X-Ray Inspection Method 2012
Electrical Tests - Subgroup 1; Read and Record (T0)
Static Burn-In Method 1015, Condition B, 72 Hrs, +125°C Min.
Interim 1 Electrical Tests - Subgroup 1; Read and Record (T1)
Burn-In Delta Calculation (T0 -T1)
PDA Calculation 3% Subgroup 7
5% Subgroups 1, 7, Δ
Dynamic Burn-In Method 1015, Condition D, 240 Hrs, +125°C (Note 3)
Interim 2 Electrical Tests - Subgroup 1; Read and Record (T2)
Alternate Group A - Subgroups 1, 7, 9; Method 5005; Para 3.5.1.1
Burn-In Delta Calculation (T0 - T2)
PDA Calculation 3% Subgroup 7
5% Subgroups 1, 7, Δ
Electrical Tests - Subgroup 3; Read and Record
Alternate Group A - Subgroups 3, 8B, 11; Method 5005; Para 3.5.1.1
Marking
Electrical Tests - Subgroup 2; Read and Record
Alternate Group A - Subgroups 2, 8A, 10; Method 5005; Para 3.5.1.1
Gross Leak Tests Method 1014, 100%
Fine Leak Tests Method 1014, 100%
Customer Source Inspection (Note 2)
Group B Inspection Method 5005 (Note 2)
End-Point Electrical Parameters: B-5 - Subgroups 1, 2, 3, 7, 8A, 8B, 9, 10, 11; B-6 - Subgroups 1, 7, 9
Group D Inspection Method 5005 (Notes 2, 4)
End-Point Electrical Parameters: Subgroups 1, 7, 9
External Visual Inspection Method 2009
Data Package Generation (Note 5)

NOTES:
1. The notes of Method 5004, Table 1 shall apply; Unless Otherwise Specified.
2. These steps are optional, and should be listed on the individual purchase order(s), when required.
3. Harris reserves the right of performing burn-in time temperature regression as defined by Table 1 of Method 1015.
4. For Group D, Subgroup 3 inspection of package configurations which utilizes a gold plated lid in its construction; the inspection criteria for illegible markings criteria of Method 1010, paragraph 3.3 and of Method 1004, paragraph 3.8.a shall not apply.
5. Data package contains:
   Assembly Attributes (post seal)
   Test Attributes (includes Group A)
   Shippable Serial Number List
   Radiation Testing Certificate of Conformance
   Wafer Lot Acceptance Report (Including SEM Report)
   X-Ray Report and Film
   Test Variables Data

Harris -8 Product Flow

Internal Visual Inspection
Gamma Radiation Assurance Tests Method 1019
Customer Pre-Cap Visual Inspection (Note 1)
Temperature Cycling Method 1010, Condition C
Fine and Gross Leak Tests Method 1014
Constant Acceleration Method 2001 Y1 30KG
Initial Electrical Tests
Dynamic Burn-In Method 1015, Condition D, 160 Hrs, +125°C
+25°C Electrical Tests - Subgroups 1, 7, 9
PDA Calculation 5% Subgroups 1, 7
Electrical Tests +125°C, -55°C
Group A Inspection Method 5005. 5% PDA (Note 3)
Brand
Customer Source Inspection (Note 1)
Group C Inspection Method 5005 (Notes 1, 2)
Group D Inspection Method 5005 (Notes 1, 2)
External Visual Inspection Method 2009
Data Package Generation (Note 4)

NOTES:
1. These steps are optional, and must be negotiated as part of order.
2. Group B and D data package contains Attributes Data plus Variables Data.
3. Harris reserves the right to perform Alternate Group A. The 5% PDA is still applicable.
4. '-8' Data package contains:
   Assembly Attributes (post seal)
   Test Attributes (includes Group A)
   Radiation Testing Certificate of Conformance
   Certificate of Conformance (as found on shipper)

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Metallization Topology

DIE DIMENSIONS:
Die Size: 132 x 160 mils
Die Thickness: 14 ±1 mils

METALLIZATION:
Type: Si-Al, 14kÅ ± 2kÅ
Back: Gold

GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ± 1kÅ

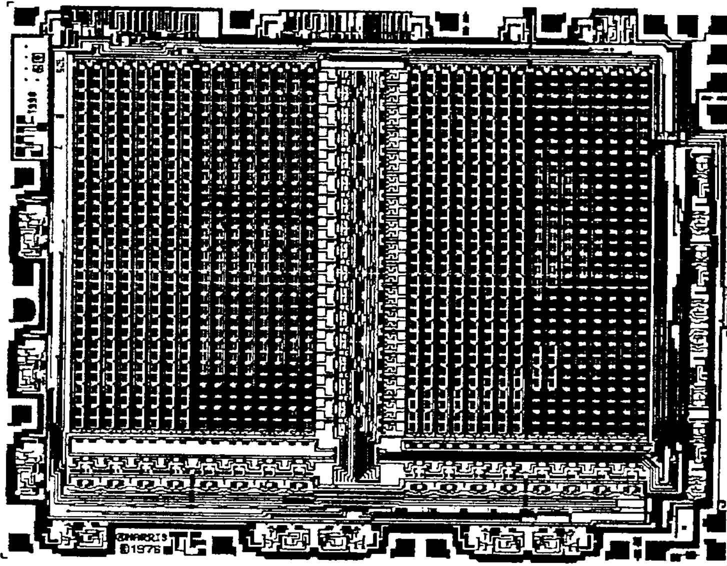
DIE ATTACH:
Material: Si-Au Eutectic Alloy
Temperature: Sidebrazed Ceramic DIP - 460°C±10°C (Max)
Braze Seal Flatpack- 460°C ± 10°C (Max)

WORST CASE CURRENT DENSITY: 5.8×10^4 A/cm^2

SUBSTRATE POTENTIAL: VDD

Metallization Mask Layout

HS-6551RH



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