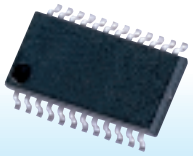
TPD7202F

● *Power MOSFET Gate Driver for H-Bridge*

TPD7202F is a power MOSFET Gate driver for H-bridge circuit using charge pump system. Because this IC contains a charge pump circuit for high-side drive, it allows you to configure H-bridge circuit.

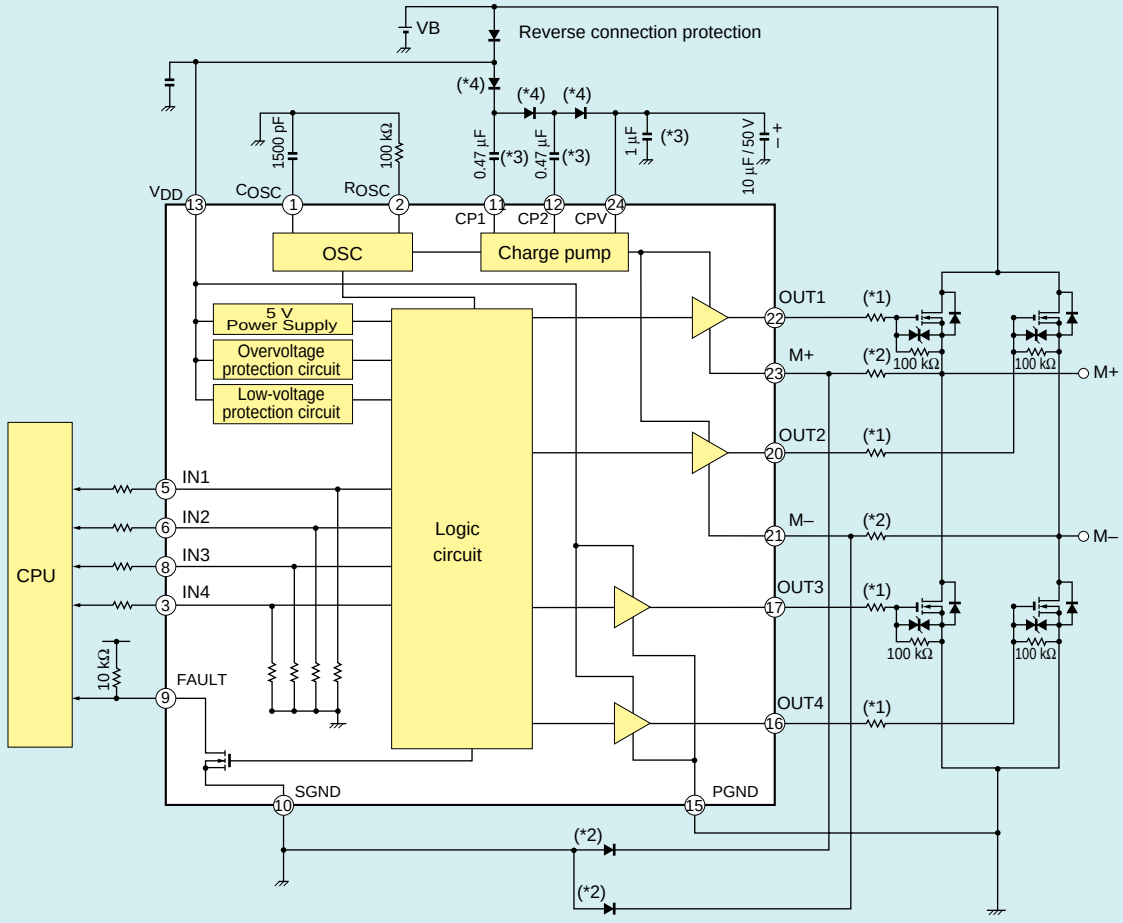
Features

- Power MOSFET Gate driver for H-bridge circuit
- Built-in power MOSFET protecrion and diagnosis functions:
  Overvoltage and low-voltage protedtion
- Built-in a charge pump circuit.
- Package: SSOP-24 (300 mil) with embossed-tape packing



SSOP-24PIN

Block Diagram



(*1): Optimum conditions depend on switching loss, EMI, etc. of external MOSFET.
(*2): SBD V_F = 0.5 V max (Recommended: CRS03)
This is need when the M+ or M- pin is biased to the negative side by more than 0.5 V.
(*3): This is a laminated ceramic capacitor.
(*4): High-speed diode t_{rr} = 100 ns max (Recommended: CRH01)

Maximum Rating (T_a = 25°C)

Characteristic	Symbol	Rating	Unit	Remarks
Power Supply Voltage	V_{DD}	– 0.5 to 30	V	
Output Current	I_{SOURCE}	1	A	Pulse width ≦ 10 μs
	I_{SINK}	1		
Input Voltage	V_{IN}	– 0.5 to 7	V	
FAULT Pin Voltage	V_{FAULT}	30	V	
M+, M– Pin Neagative Voltage	M+ (–) M– (–)	– 0.5	V	Negative voltage that can be applied to M+ and M– pin (reference to SGND pin)
PGND Pin Neagative Voltage	PGND (–)	– 0.5	V	Negative voltage that can be applied to PGND pin (reference to SGND pin)
FAULT Pin Current	I_{FAULT}	5	mA	
Power Dissipation	P_D	0.8	W	
		1.2 (Note)		
Operating Temperature	Topr	– 40 to 125	°C	
Storage Temperature	Tstg	–40 to 150	°C	

Note: When a device mounted on 60 mm x 60 mm x 1.6 mm glass epoxy PCB

Electrical Characteristics (T_j = –40 to 125°C)

Characteristic		Symbol	Condition	Min	Typ.	Max	Unit	Remarks
Operating Supply Voltage		V_{DD}	—	7	13.5	18	V	
Supply Current		$I_{DD\ (1)}$	V_{DD} = 13.5 V	—	—	10	mA	Oscilation circuit stops
		$I_{DD\ (2)}$	V_{DD} = 13.5 V, V_{IN1} to V_{IN4}= 0 V	—	—	100		When oscilation circuit is operating f = 20 kHz, mean current
Input Voltage		V_{IH}	V_{DD} = 7 V to 18 V, I_O = 0 A	3.5	—	—	V	IN1-IN4 high-level input voltage
		V_{IL}		—	—	1.5		IN1-IN4 low-level input voltage
Input Current		I_{IH}	V_{DD} = 7 V to 18 V, V_{IN} = 5 V, I_O = 0 A	—	—	1	mA	IN1-IN4 input current
		I_{IL}	V_{DD} = 7 V to 18 V, V_{IN} = 0 V, I_O = 0 A	–10	—	10	μA	
Output Voltage	High side	V_{OH}	V_{DD} = 13.5 V, V_{IN} = 5 V, I_O = 0 A	V_{CPV} –2	—	V_{CPV}	V	OUT1 pin voltage (reference to M+ pin) OUT2 pin voltage (reference to M– pin) V_{CPV} denotes CPV pin voltage
		V_{OL}	V_{DD} = 13.5 V, V_{IN} = 0 V, I_O = 0 A	—	—	0.1		
	Low side	V_{OH}	V_{DD} = 13.5 V, V_{IN} = 5 V, I_O = 0 A	11.5	—	13.5		OUT3 pin voltage (reference to PGND pin) OUT4 pin voltage (reference to PGND pin)
		V_{OL}	V_{DD} = 13.5 V, V_{IN} = 0 V, I_O = 0 A	—	—	0.1		
Charge Pump Voltage		V_{CPV}	V_{DD} = 13.5 V	23.5	—	34	V	CPV pin voltage (reference to SGND pin)
Active Clamp Voltage	High side	V_{CLAMP}	V_{IN} = 5 V, I_O = 10 mA	14	—	20	V	Clamp voltage between OUT1 and M+ pins Clamp voltage between OUT2 and M– pins
	Low side		V_{IN} = 5 V, I_O = 10 mA	—	18	—		OUT3 and OUT4 pins clamp voltage (reference to PGND pin)
Output Resistance		R_{SOURCE}	V_{DD} = 13.5 V, V_{IN} = 5 V, I_O = 0.5 A	—	7	10	Ω	OUT1-OUT4 output resistance pulse width ≦ 10 μs
		R_{SINK}	V_{DD} = 13.5 V, V_{IN} = 0 V, I_O = –0.5 A	—	4.5	10		
Low-Voltage Protection	Detection	$V_{SD\ (L)}$	—	5.5	6	6.5	V	Lowvoltage detection voltage and hysteresis (V_{DD} voltage detected)
	Hysteresis	$\Delta V_{SD\ (L)}$		—	0.5	—		
Overvoltage Protection	Detection	$V_{SD\ (H)}$	—	20	22	24	V	Overvoltage detection voltage and hysteresis (V_{DD} voltage detected)
	Hysteresis	$\Delta V_{SD\ (H)}$		—	2	—		
Switching Time	Turn-on delay time	$t_{d\ (ON)}$	V_{DD} = 7 V to 18 V, C_{OUT} = 0.047 μF, R_G = 47 Ω	—	—	4	μs	OUT1-OUT4 switching time
	Turn-on time	t_{ON}		—	—	6		
	Turn-off delay time	$t_{d\ (OFF)}$		—	—	4		
	Turn-off time	t_{OFF}		—	—	6		
Oscillation Frequency		f_{OSC}	V_{DD} = 7 V to 18 V, R_{OSC} = 100 kΩ, C_{OSC} = 1500 pF	—	20	—	kHz	f_{OSC} calculation formula $f_{OSC} \fallingdotseq 3 / \{C_{OSC} (R_{OSC} + 2\ k)\}$ (Hz)
FAULT Pin Voltage		V_{FAULT}	I_{FAULT} = 1 mA	—	—	0.8	V	FAULT pin low-level voltage (open-drain)
FAULT Output Delay Time		t_{ON}	R_{FAULT} = 5.1 kΩ, V_{FAULT} = 5 V (External power supply)	—	1	—	μs	Time from low voltage / overvoltage detection or restoration to FAULT output inversion
		t_{OFF}		—	1	—		