DATA SHEET

NEC

BIPOLAR ANALOG INTEGRATED CIRCUIT
μPC659A

8-BIT A/D CONVERTER FOR VIDEO PROCESSING WITH REFERENCE GENERATOR AND CLAMP CIRCUIT

The μPC659A is a 8-bit A/D converter for video signal processing, the power consumption of which is lower than the μPC659. The high speed and high quality bipolar processing technology has enabled fast conversion rate and high resolution to be achieved. Conversion rate is up to 20 Msps (sampling per second) and linearity error within ± 0.5 LSB while operating at low power consumption. Wide variety of application can be realized in digital application field such as digital TV system and high speed facsimile.

Also, this IC includes sample and hold circuit, clamp circuit and reference voltage generator, which enable simple external circuit to be constructed.

The μPC659A and the μPC659 are different in the number of clock pulses till transformed data is output after analog signal is captured. This should be taken into consideration when using the μPC659A instead of the μPC659. For details, refer to the timing chart of page 8.

FEATURES

- Resolution : 8-bit
- Conversion rate : 20 Msps
- Differential non-linearity : ± 0.5 LSB MAX.
- Power supply : + 5 V
- Analog input voltage : 1.0 V_{p-p}
- Power consumption : 210 mW TYP.
- Built-in circuit : Sample and hold circuit
  Clamp circuit (Clamp voltage and clamp pulse must be supplied)
  Reference voltage generator (V_{RB} = 2.3 V, V_{RT} = 3.3 V TYP.)

ORDERING INFORMATION

Part Number	Package	Quality Grade
μPC659AGS	24-pin plastic SOP (300 mil)	Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

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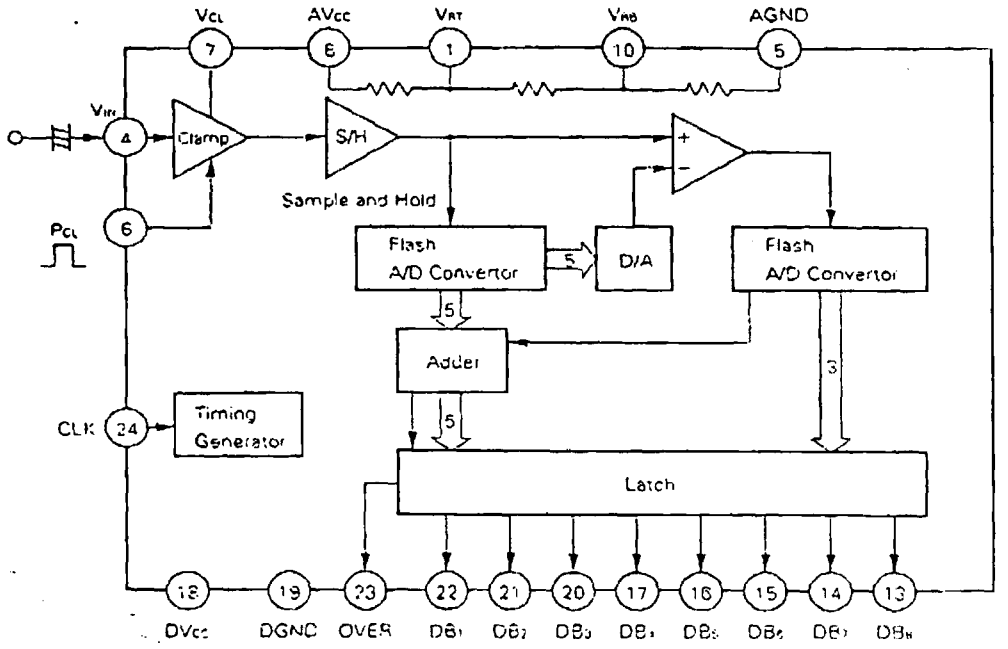
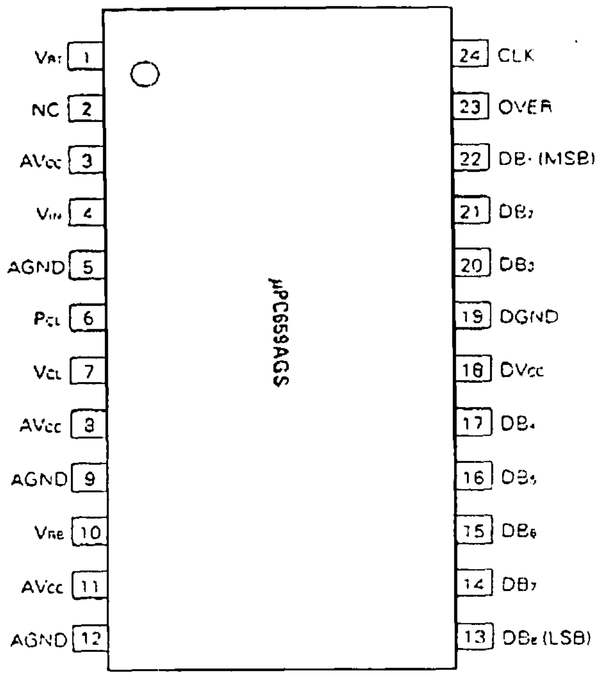
BLOCK DIAGRAM

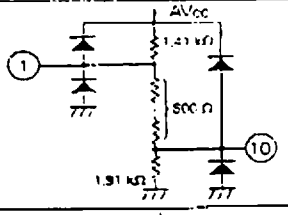
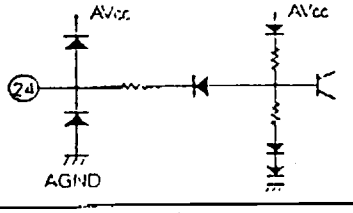
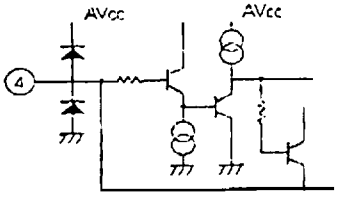
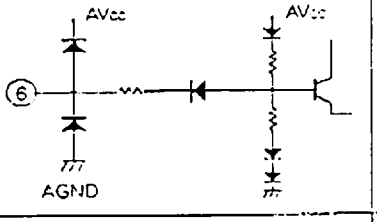
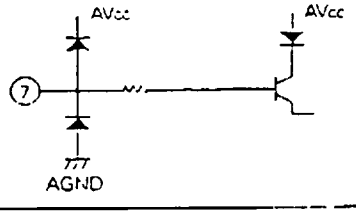
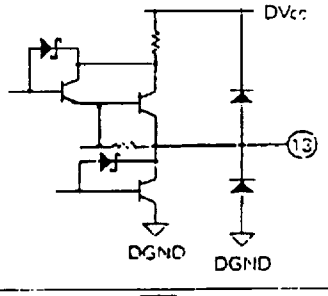


PIN CONFIGURATION (Top View)



No.	Symbol	Pin Name	No.	Symbol	Pin Name
1	V_{RT}	Ref. Voltage (Top)	13	DB_8	Digital Data Output (LSB)
2	NC	No Connection	14	DB_7	Digital Data Output (7th)
3	AV_{CC}	Power Supply for Analog Circuit	15	DB_6	Digital Data Output (6th)
4	V_{IN}	Analog Signal Input Terminal	16	DB_5	Digital Data Output (5th)
5	AGND	Ground for Analog Circuit	17	DB_4	Digital Data Output (4th)
6	P_{CL}	Clamp Pulse Input Terminal	18	DV_{CC}	Power Suply for Digital Circuit
7	V_{CL}	Clamp Voltage Input Terminal	19	DGND	Ground for Digital Circuit
8	AV_{CC}	Power Supply for Analog Circuit	20	DB_3	Digital Data Output (3rd)
9	AGND	Ground for Analog Circuit	21	DB_2	Digital Data Output (2nd)
10	V_{RB}	Ref. Voltage (Bottom)	22	DB_1	Digital Data Output (MSB)
11	AV_{CC}	Power Supply for Analog Circuit	23	OVER	Digital Over Range Output
12	AGND	Ground for Analog Circuit	24	CLK	Sampling Clock Input Terminal

EQUIVALENT CIRCUIT AROUND TERMINAL

Pin No.	Equivalent Circuit	Function
1, 10		1: Reference voltage (Top) V_{RT} 10: Reference voltage (Bottom) V_{RB}
5, 9, 12		Ground for Analog Circuit.
24		Sampling Clock input terminal. Analog data acquisition and digital data out are synchronized with the rising edge of this clock.
3, 9, 11		Power supply for analog circuit.
4		Analog signal input terminal. Input analog signal from this terminal. The signal is read at rising edge of the clock. The clamp function also will be worked on this terminal. So it's necessary to connect capacitance and low impedance signal source. The burst signal is protected at pedestal clamp because of soft clamp circuit.
6		Clamp pulse input terminal. Analog signal input from analog input terminal is clamped to the voltage: V_{CL} according to the high level term of this pulse. During high level signal is input, analog input pin voltage is nearly clamped to voltage V_{CL}.
7		Clamp voltage input terminal. Set voltage at clamping analog input signal Analog input signal is clamped nearly to this input voltage V_{CL} according to the clamp pulse P_{CL} high level period.
13 to 17 20 to 22 23		Digital data output terminal 13: Out of LSB data 14: Out of 7th data 15: Out of 6th data 16: Out of 5th data 17: Out of 4th data 20: Out of 3rd data 21: Out of 2nd data 22: Out of MSB data 23: Out of Over Flow (Active High)
18		Power supply for digital.
19		Ground for digital.

ABSOLUTE MAXIMUM RATINGS (T_a = + 25 °C)

Parameter	Symbol	Ratings	Unit
Supply voltage	AVcc, DVcc	– 0.3 to + 6.0	V
Digital input voltage	VIND	– 0.3 to DVcc + 0.3	V
Analog input voltage	VINA	– 0.3 to AVcc + 0.3	V
Reference input voltage	VRT, VRB	– 0.3 to AVcc + 0.3	V
Clamp voltage	VCL	– 0.3 to AVcc + 0.3	V
Clamp pulse input voltage	VPCL	– 0.3 to AVcc + 0.3	V
Operating temperature	Topt	– 20 to +70	°C
Storage temperature	Tstg	– 40 to +150	°C
Power dissipation	Pd	560	mW

RECOMMENDED OPERATING CONDITIONS (T_a = – 20 to + 70 °C)

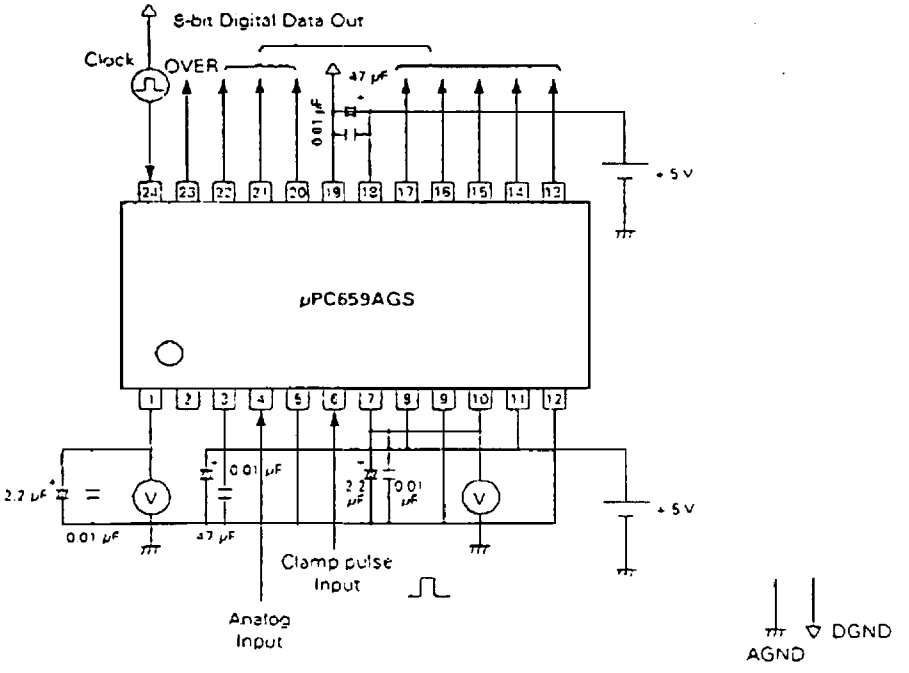
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply voltage	AVcc, DVcc	AGND=DGND = 0 V	4.7	5.0	5.3	V
Analog input voltage	VINA	Vcc = 5.0 V	VRB – 0.4		VRT + 0.4	V
Clamp input voltage	VCL	Vcc = 5.0 V	VRB – 0.4		VRT + 0.4	V
Sampling clock	fsamp				20	MHz
Sampling clock high level pulse width	tPWH		25			ns
Sampling clock low level pulse width	tPWL		25			ns
Clock input high level voltage	VCKH		2.0			V
Clock input low level voltage	VCKL				0.8	V
Clamp pulse width	tPWCL		1.0			μs
Clamp pulse input high level voltage	VPCLH		2.0			V
Clamp pulse input low level voltage	VPCLL				0.8	V
Clamp capacitance	CCL			10		μF
Maximum analog input frequency	fAIN			8		MHz

ELECTRICAL CHARACTERISTICS (T_a = − 20 to + 70 °C, AVcc = DVcc = 5.0 ± 0.3 V)

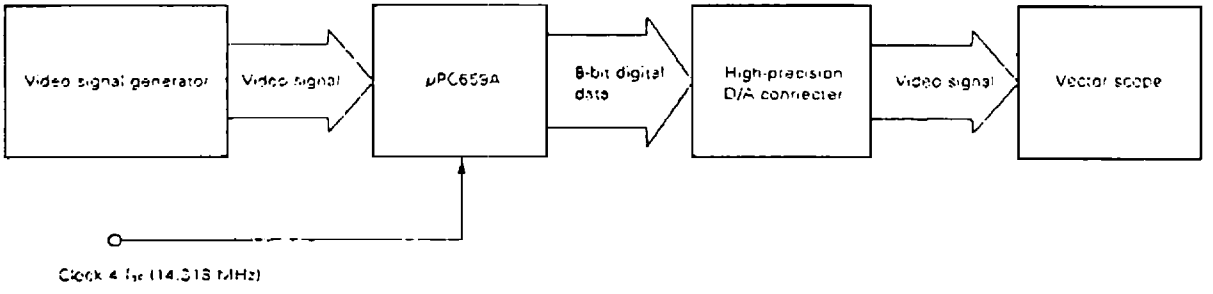
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply current	I_{CC}	V_{CC} = 5.0 V, T_a = + 25 °C	25	42	60	mA
Resolution	RES			8		bit
Non-linearity	NL	V_{CC} = 5.0 V, T_a = + 25 °C V_{IN} = 1.0 V_{P-P}			± 1.5	LSB
Differential non-linearity	DNL	V_{CC} = 5.0 V, T_a = + 25 °C V_{IN} = 1.0 V_{P-P}			± 0.5	LSB
Differential gain	DG	f_{samp} = 14.318 MHz NTSC ramp wave (40 IRE)		1.5	3	%
Differential phase	DP	f_{samp} = 14.318 MHz NTSC ramp wave (40 IRE)		0.8	3	deg
Digital data output delay time	t_D	Delay time from rising edge of sampling clock, DB1 to DB8, OVER		20	35	ns
Digital output low level voltage	V_{OL}	I_{OL} = 1.6 mA DB1 to DB8, OVER			0.4	V
Digital output high level voltage	V_{OH}	I_{OH} = − 400 μA DB1 to DB8, OVER	2.7			V
Digital input low level current	I_{INDL}	V_{IN} = 0.8 V			− 200	μA
Digital input high level current	I_{INDH}	V_{IN} = 2.0 V			10	μA
Analog input current	I_{INA}	Measure input current from analog input terminal		10	35	μA
Reference voltage (Bottom)	V_{RB}	V_{CC} = 5.0 V	2.1	2.3	2.5	V
Reference voltage (Top)	V_{RT}	V_{CC} = 5.0 V	3.1	3.3	3.5	V
Analog input equivalent capacitance	C_{IN}	V_{IN} = V_{RB}		3		pF
Clock input equivalent capacitance	C_{CLK}			2		pF
Reference voltage (Difference)	V_{REF}	V_{RT} − V_{RB}, V_{CC} = 5.0 V		1		V

Caution The values of I_{CC} and t_D are different between the μPC659 and the μPC659A

TEST CIRCUIT

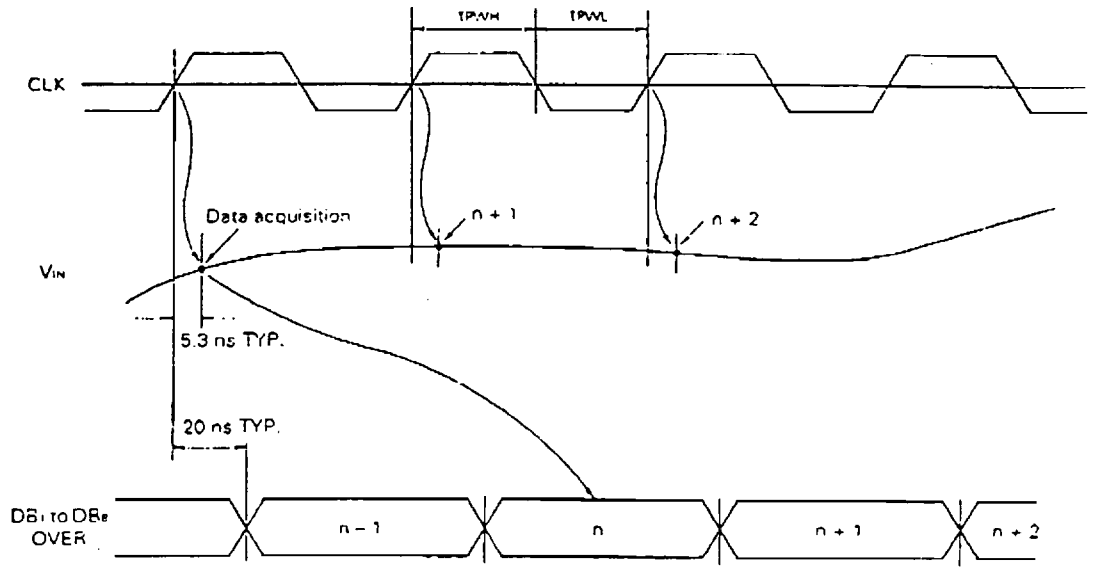


DG, DP TEST BLOCK



The video signal from the video signal generator is 40 IRE ramp signal.

TIMING CHART



Analog signal is captured at the rising edge, and converted data will be out at the rising edge after 1 clock pulse[Note].

Note For the μPC659, 2 clock pulses.

Caution The value of data output delay time (t_D) is different between the μPC659 and the μPC659A.

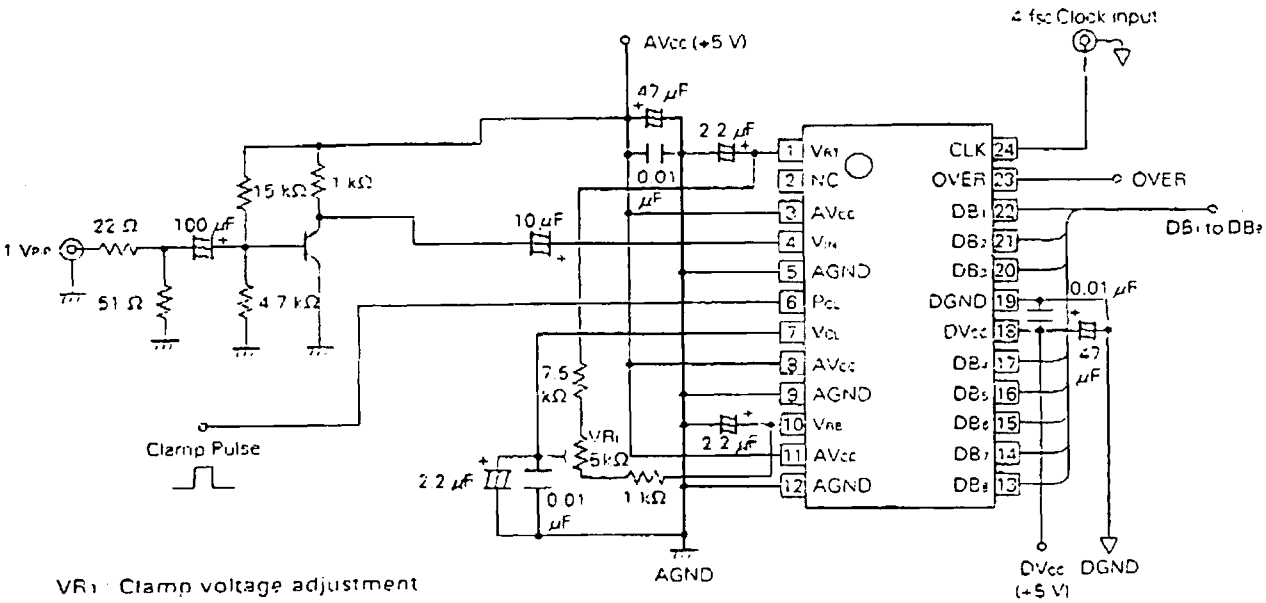
OUTPUT CODE FOR ANALOG INPUT

Analog input	Output digital code								
	OVER	DB1 (MSB)	DB2	DB3	DB4	DB5	DB6	DB7	DB8 (LSB)
V_{RB} to 1/2 LSB	0	0	0	0	0	0	0	0	0
1/2 LSB to (1 + 1/2) LSB	0	0	0	0	0	0	0	0	1
to	to	to	to	to	to	to	to	to	to
(254 + 1/2) LSB to (255 + 1/2) LSB	0	1	1	1	1	1	1	1	1
(255 + 1/2) LSB to V_{RT}	1	1	1	1	1	1	1	1	1
V_{RT} to AV_{CC}	1	1	1	1	1	1	1	1	1

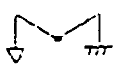
$$LSB \fallingdotseq \frac{V_{RT}-V_{RB}}{256} \fallingdotseq 3.906\ \text{mV TYP}$$

V_{RB} = 2.3 V TYP.
V_{RT} = 3.3 V TYP.

APPLICATION



VR1 : Clamp voltage adjustment

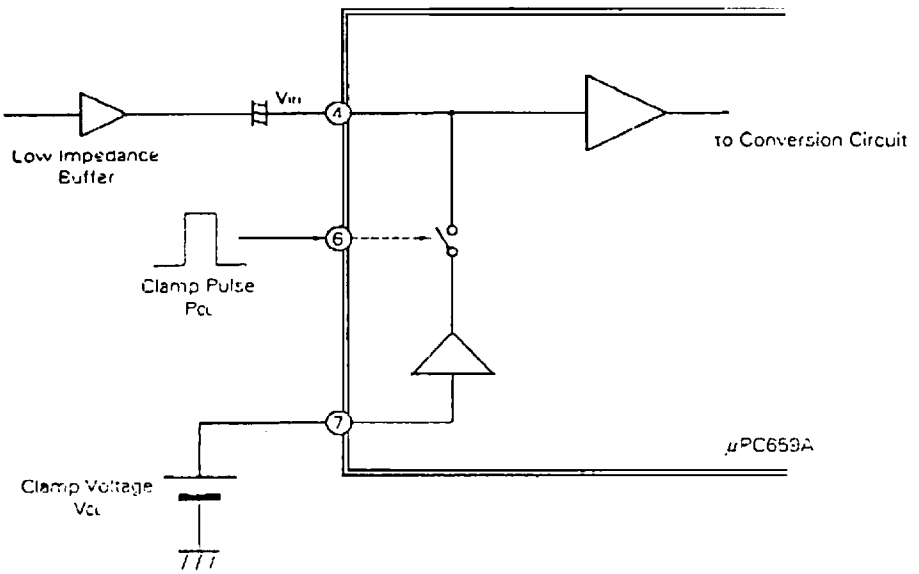


Must be thick line wiring for the power supply lines. And reduce the resistance and reactance ingredient.
AVcc and DVcc must be connected at one point.
AGND and DGND must be connected at one point.

The application circuits and circuit constant described in this document don't apply to mass production where variations in parts quality and/or temperature characteristics are considered.

ATTENTION FOR APPLICATION

- Analog input terminal
  Please connect low impedance signal source to analog input terminal, because of executing clamp operation.
  And must be AC coupled. Clamp circuit is appeared by following rough block diagram.
  Take polarity of clamping capacitor into account.



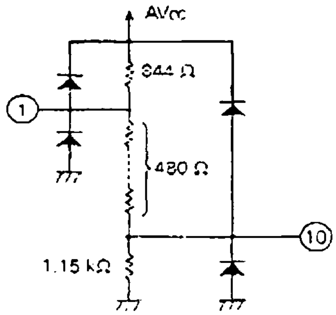
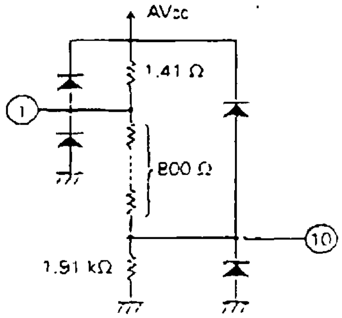
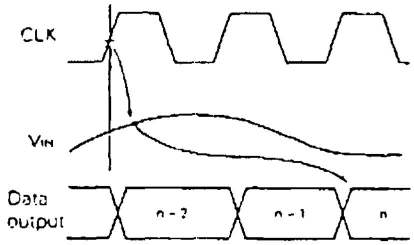
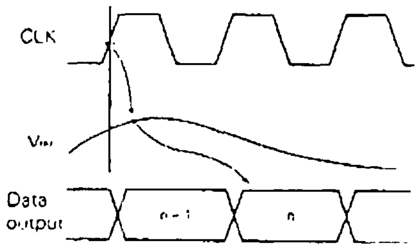
- If don't use the clamp circuit
  The clamp pulse terminal (PIN 6) and GND must be short-circuit. And insert by-pass capacitor of about 0.1 μF between the clamp voltage input terminal (PIN 7) and GND. Input analog signal to PIN 4.
- Clamp voltage
  There is a few difference clamp voltage between the supply clamp voltage V_{CL} (PIN 7) and really clamp voltage.
  Really clamp voltage = $V_{CL} + \alpha$
  Take account of the α (about ± 20 mV) at supply V_{CL} to PIN 7.
- Converted data output
  Analog signal is captured at the rising edge, and converted data will be out at the rising edge after 1 clock pulse [Note]
- When reference voltage is set from external, V_{R6} (PIN 10) = 2.3 V, V_{RT} (PIN 1) = 3.3 V.

Note For the μPC659, 2 clock pulses.

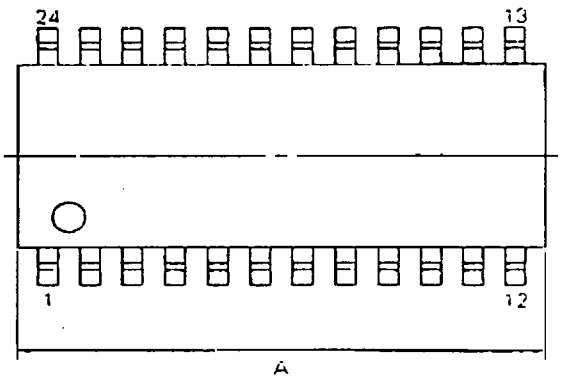
DIFFERENCE BETWEEN THE μPC659 AND THE μPC659A

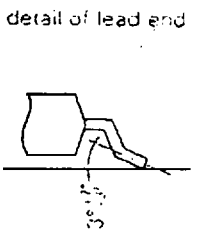
The following table shows the differences between the μPC659 and the μPC659A

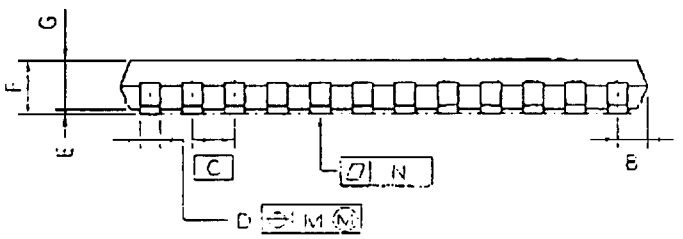
This should be taken into consideration when using the μPC659A instead of the μPC659.

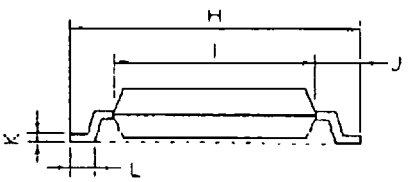
Parameter		μPC659	μPC659A
Supply current Icc (V_{CC} = 5.0 V, T_a = +25 °C)	MIN.	50 mA	25 mA
	TYP.	79 mA	42 mA
	MAX.	110 mA	60 mA
Digital data output delay time to	TYP.	12 ns	20 ns
	MAX.	20 ns	35 ns
Internal reference resistance PIN 1, PIN 10			
Timing chart			

24 PIN PLASTIC SOP (300 mil)









NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

P24GM-50-300B-2

ITEM	MILLIMETERS	INCHES
A	15.54 MAX.	0.612 MAX.
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.40^{+0.10}_{-0.05}$	$0.016^{+0.004}_{-0.002}$
E	0.1±0.1	0.004±0.004
F	1.8 MAX.	0.071 MAX.
G	1.55	0.061
H	7.7±0.3	0.303±0.012
I	5.6	0.220
J	1.1	0.043
K	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$
L	0.6±0.2	$0.024^{+0.008}_{-0.009}$
M	0.12	0.005
N	0.15	0.006

RECOMMENDED SOLDERING CONDITIONS

The following conditions (See table below) must be met when soldering this product.

For more details, refer to our document "SEMICONDUCTOR DEVICE TECHNOLOGY MANUAL" (IEI-1207)

Please consult with our sales offices in case other soldering process is used, or in case soldering is done under different conditions.

TYPE OF SURFACE MOUNT DEVICE

μPC659AGS: 24-pin plastic SOP (300 mil)

Soldering process	Soldering conditions	Symbol
Infrared Ray Reflow	Peak package's surface temperature : 230 °C or below, Reflow time : 30 seconds or below (210 °C or higher), Number of reflow process : 1	IR30-00-1
VPS	Peak package's temperature : 215 °C or below, Reflow time : 40 seconds or below (200 °C or higher), Number of reflow process : 1	VP15-00-1
Wave Soldering	Solder temperature : 260 °C or below, Flow time : 10 seconds or below, Temperature of pre-heat : 120 °C or below (Plastic surface temperature) Number of flow process : 1	WS60-00-1
Partial Heating Method	Terminal temperature : 300 °C or below, Time : 3 seconds or below (Per side of leads)	—

Caution Do not apply more than one soldering method at any one time, except for "Partial heating method".

[MEMO]