## 128Kx8 Static RAM CMOS, Module

The EDI8M8128C/LP/P* is a 1024K bit CMOS Static RAM based on four 32Kx8 Static RAMs in leadless chip carriers mounted on a multi-layered ceramic substrate.

An on-board decoder circuit interprets the higher order address to select one of the 32Kx8 Static RAMs.

All inputs and outputs are TTL compatible and operate from a single 5V supply. Fully asynchronous, the EDI8M8128C/LP/P requires no clocks or refreshing for operation.

The Military product is available in two low power versions, P and LP. The LP version offers a data retention function for battery backup applicatons.

EDI Military Modules are built with RAMs that are compliant to MIL-STD-883, Paragraph 1.2.1.

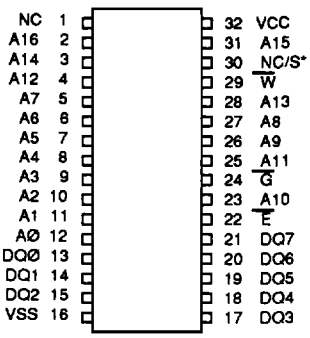
## Features

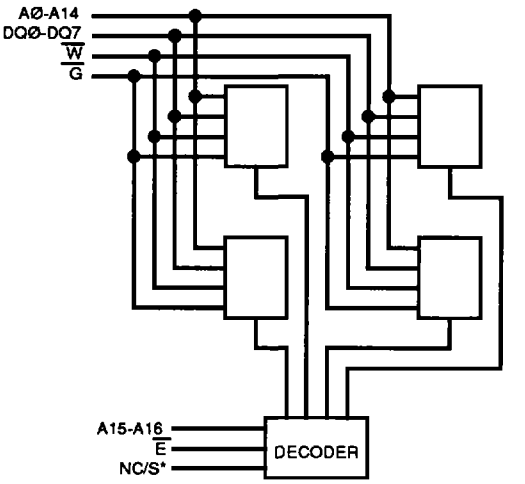
128Kx8 bit CMOS Static Random Access Memory
- Access Times 45 thru 150ns
- $\overline{E}$, S*, and $\overline{G}$ Functions for Bus Control
- Data Retention Function (LP Version Only)
- TTL Compatible Inputs and Outputs
- Fully Static, No Clocks

Jedec Approved Pinout
- 32 Pin Ceramic DIP Module, No. 51

Single +5V (±10%) Supply Operation

## Pin Configuration and Block Diagram




## Pin Names

| | |
|---|---|
| AØ-A16 | Address Inputs |
| $\overline{E}$ | Chip Enable |
| $\overline{S}$* | Chip Select |
| $\overline{W}$ | Write Enable |
| $\overline{G}$ | Output Enable |
| DQØ-DQ7 | Common Data Input/Output |
| VCC | Power (+5V±10%) |
| VSS | Ground |
| NC | No Connection |

**EDI8M8130C/LP/P is identical to the EDI8M8128C/LP/P, with an additional chip select line (S). This additional chip select line can be used to provide system memory security during power down in non-battery backed up systems and to simplify decoding schemes in memory banking where large multiple pages of memory are required.*

## Absolute Maximum Ratings*

Voltage on any pin relative to VSS ..... -0.5V to 7.0V
Operating Temperature TA (Ambient)
Commercial ..... 0°C to +70°C
Industrial ..... -40°c to +85°C
Military ..... -55°C to +125°C
Storage Temperature
Ceramic ..... -65°C to +150°C
Power Dissipation ..... 1 Watt
Output Current. ..... 20 mA

*Stress greater than those listed under "Absolute Maxi5mum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## Recommended DC Operating Conditions

| Parameter | Sym | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Supply Voltage | VCC | 4.5 | 5.0 | 5.5 | V |
| Supply Voltage | VSS | 0 | 0 | 0 | V |
| Input High Voltage | VIH | 2.2 | -- | 6.0 | V |
| Input Low Voltage | VIL | -0.3 | -- | 0.8 | V |

## AC Test Conditions

Input Pulse Levels ..... VSS to 3.0V
Input Rise and Fall Times ..... 5ns
Input and Output Timing Levels ..... 1.5V
Output Load 45-70ns ..... 1TTL, CL = 30pF
80-150ns ..... 1TTL, CL = 100pF
(note: For TEHQZ,TGHQZ and TWLQZ, CL = 5pF)

## DC Electrical Characteristics

| Parameter | Sym | Conditions | | Min | Typ* | Max 45-70 | Max 80-150 | Units |
|---|---|---|---|---|---|---|---|---|
| Operating Power Supply Current | ICC1 | $\overline{W}$, $\overline{E}$ = VIL, II/O = 0mA, Min Cycle | | -- | 70 | 210 | 95 | mA |
| Standby (TTL) Power Supply Current | ICC2 | $\overline{E}$ ≥ VIH, VIN ≤ VIL or ≥ VIH | | -- | 10 | 110 | 40 | mA |
| Full Standby Power Supply Current | ICC3 | $\overline{E}$ ≥ VCC-0.2V | C | -- | 1 | 20 | 3 | mA |
| | | VIN ≥ VCC-0.2V or VIN ≤ 0.2V | LP/P | -- | 50 | -- | 900 | µA |
| Input Leakage Current | ILI | VIN = 0V to VCC | | -- | -- | ±10 | ±10 | µA |
| Output Leakage Current | ILO | V I/O = 0V to VCC | | -- | -- | ±10 | ±10 | µA |
| Output High Voltage | VOH | IOH = -1.0mA | | 2.4 | -- | -- | -- | V |
| Output Low Voltage | VOL | IOL = 2.1mA | | -- | -- | 0.4 | 0.4 | V |

*Typical: TA = 25°C, VCC = 5.0V

## Truth Table

| $\overline{G}$ | $\overline{E}$ | $\overline{W}$ | Mode | Output | Power |
|---|---|---|---|---|---|
| X | H | X | Standby | High Z | ICC2, ICC3 |
| H | L | H | Output Deselect | High Z | ICC1 |
| L | L | H | Read | DOUT | ICC1 |
| X | L | L | Write | DIN | ICC1 |

## Capacitance

(f=1.0MHz, VIN=VCC or VSS)

| Parameter | Sym | Max | Unit |
|---|---|---|---|
| Input Capacitance (Except DQ Pins) | CI | 50 | pF |
| Capacitance Control (DQ Pins) | CD/Q | 43 | pF |
| Input Capacitance Control Lines ($\overline{E}$) | CC | 10 | pF |
| Input Capacitance $\overline{W}$ Line | CW | 50 | pF |

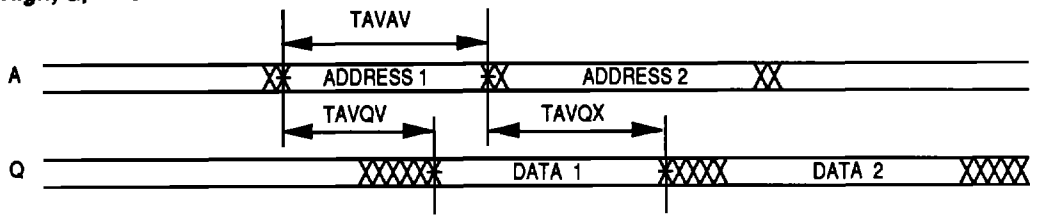
These parameters are sampled, not 100% tested.

## AC Characteristics
## Read Cycle

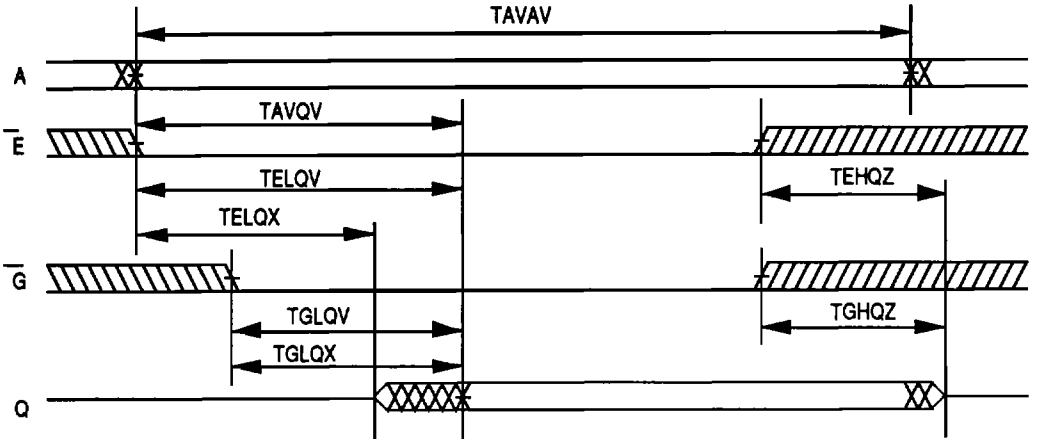
| Parameter | Symbol | 45ns | | 55ns | | 70ns | | 80ns | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| Read Cycle Time | TAVAV | 45 | | 55 | | 70 | | 80 | | ns |
| Address Access Time | TAVQV | | 45 | | 55 | | 70 | | 80 | ns |
| Chip Enable Access Time | TELQV | | 45 | | 55 | | 70 | | 80 | ns |
| Chip Enable to Output in Low Z (1) | TELQX | 5 | | 5 | | 5 | | 5 | | ns |
| Output Enable to Output Valid | TGLQV | | 20 | | 25 | | 35 | | 35 | ns |
| Output Enable to Output in Low Z (1) | TGLQX | 3 | | 3 | | 3 | | 0 | | ns |
| Chip Disable to Output in High Z (1) | TEHQZ | | 20 | | 20 | | 35 | | 35 | ns |
| Output Disable to Output in High Z(1) | TGHQZ | | 20 | | 20 | | 35 | | 35 | ns |
| Output Hold from Address Change | TAVQX | 3 | | 3 | | 3 | | 3 | | ns |

Note 1: Parameter guaranteed, but not tested.

### Read Cycle 1
### $\overline{W}$ High; $\overline{G}$, $\overline{E}$ Low




### Read Cycle 2
### $\overline{W}$ High



## AC Characteristics
## Read Cycle

| Parameter | Symbol | 90ns | | 100ns | | 120ns | | 150ns | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| Read Cycle Time | TAVAV | 90 | | 100 | | 120 | | 150 | | ns |
| Address Access Time | TAVQV | | 90 | | 100 | | 120 | | 150 | ns |
| Chip Enable Access Time | TELQV | | 90 | | 100 | | 120 | | 150 | ns |
| Chip Enable to Output in Low Z (1) | TELQX | 5 | | 5 | | 5 | | 5 | | ns |
| Output Enable to Output Valid | TGLQV | | 40 | | 50 | | 60 | | 70 | ns |
| Output Enable to Output in Low Z (1) | TGLQX | 0 | | 0 | | 0 | | 0 | | ns |
| Chip Disable to Output in High Z (1) | TEHQZ | | 35 | | 35 | | 40 | | 45 | ns |
| Output Disable to Output in High Z(1) | TGHQZ | | 35 | | 35 | | 40 | | 45 | ns |
| Output Hold from Address Change | TAVQX | 3 | | 3 | | 3 | | 3 | | ns |

Note 1: Parameter guaranteed, but not tested.

## *AC Characteristics*
## *Write Cycle*

| Parameter | Symbol | | 45ns | | 55ns | | 70ns | | 80ns | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| Write Cycle Time | TAVAV | | 45 | | 55 | | 70 | | 80 | | ns |
| Chip Enable to | TELWH | $\overline{W}$ | 40 | | 50 | | 60 | | 70 | | ns |
| End of Write | TWLEH | $\overline{E}$ | 40 | | 50 | | 60 | | 70 | | ns |
| Address Setup Time | TAVWL | $\overline{W}$ | 0 | | 0 | | 0 | | 0 | | ns |
| | TAVEL | $\overline{E}$ | 0 | | 0 | | 0 | | 0 | | ns |
| Address Valid to | TAVWH | $\overline{W}$ | 40 | | 50 | | 60 | | 55 | | ns |
| End of Write | TAVEH | $\overline{E}$ | 40 | | 50 | | 60 | | 55 | | ns |
| Write Pulse Width | TWLWH | $\overline{W}$ | 25 | | 25 | | 45 | | 70 | | ns |
| | TELEH | $\overline{E}$ | 25 | | 25 | | 45 | | 70 | | ns |
| Write Recovery Time | TWHAX | $\overline{W}$ | 0 | | 0 | | 0 | | 0 | | ns |
| | TEHAX | $\overline{E}$ | 0 | | 0 | | 0 | | 0 | | ns |
| Data Hold Time | TWHDX | $\overline{W}$ | 3 | | 3 | | 3 | | 3 | | ns |
| | TEHDX | $\overline{E}$ | 3 | | 3 | | 3 | | 3 | | ns |
| Write to Output in High Z (1) | TWLQZ | | 0 | 20 | 0 | 35 | 0 | 40 | 0 | 45 | ns |
| Data to Write Time | TDVWH | $\overline{W}$ | 20 | | 25 | | 30 | | 35 | | ns |
| | TDVEH | $\overline{E}$ | 20 | | 25 | | 30 | | 35 | | ns |
| Output Active from End of Write (1) | TWHQX | | 3 | | 3 | | 3 | | 3 | | ns |

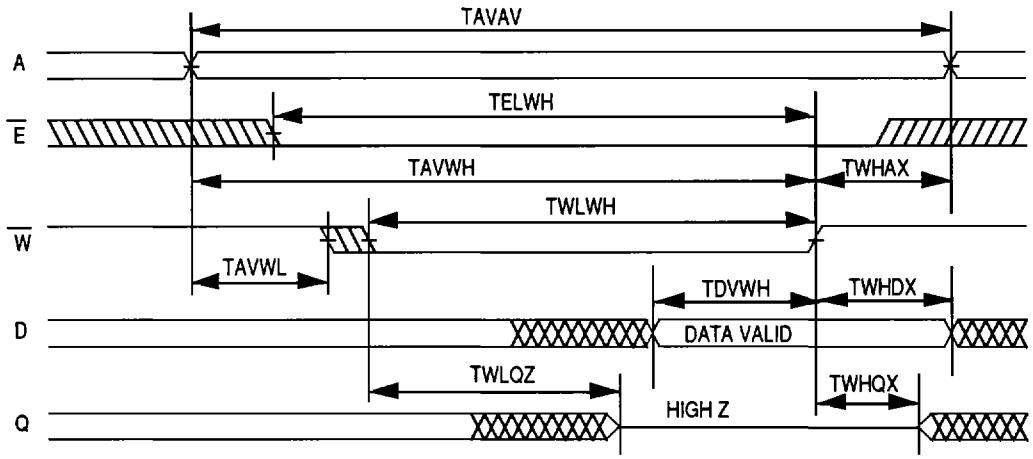
Note 1: Parameter guaranteed, but not tested.

## *AC Characteristics*
## *Write Cycle*

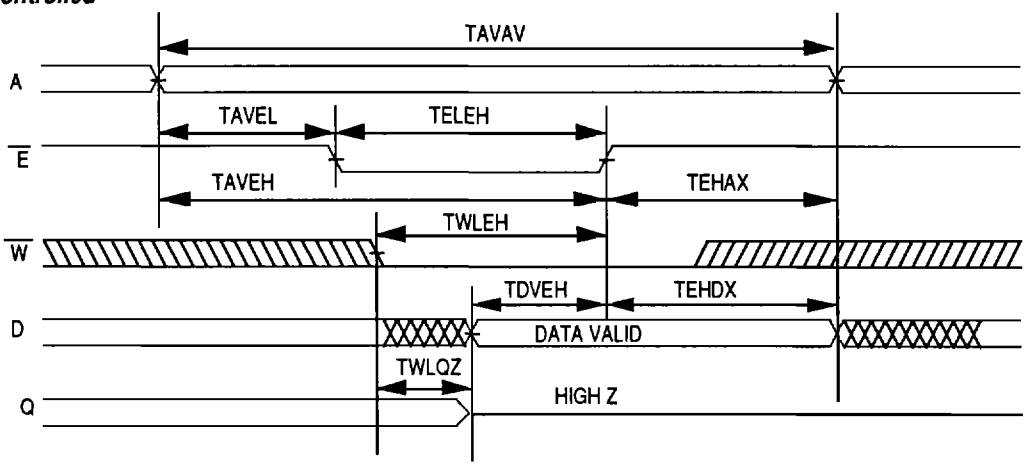
| Parameter | Symbol | | 90ns | | 100ns | | 120ns | | 150ns | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| Write Cycle Time | TAVAV | | 90 | | 100 | | 120 | | 150 | | ns |
| Chip Enable to | TELWH | $\overline{W}$ | 80 | | 80 | | 85 | | 90 | | ns |
| End of Write | TWLEH | $\overline{E}$ | 80 | | 80 | | 85 | | 90 | | ns |
| Address Setup Time | TAVWL | $\overline{W}$ | 0 | | 0 | | 0 | | 0 | | ns |
| | TAVEL | $\overline{E}$ | 0 | | 0 | | 0 | | 0 | | ns |
| Address Valid to | TAVWH | $\overline{W}$ | 70 | | 80 | | 85 | | 90 | | ns |
| End of Write | TAVEH | $\overline{E}$ | 70 | | 80 | | 85 | | 90 | | ns |
| Write Pulse Width | TWLWH | $\overline{W}$ | 55 | | 70 | | 70 | | 80 | | ns |
| | TELEH | $\overline{E}$ | 55 | | 70 | | 70 | | 80 | | ns |
| Write Recovery Time | TWHAX | $\overline{W}$ | 0 | | 0 | | 0 | | 0 | | ns |
| | TEHAX | E | 0 | | 0 | | 0 | | 0 | | ns |
| Data Hold Time | TWHDX | W | 3 | | 3 | | 3 | | 3 | | ns |
| | TEHDX | $\overline{E}$ | 3 | | 3 | | 3 | | 3 | | ns |
| Write to Output in High Z (1) | TWLQZ | | 0 | 45 | 0 | 50 | 0 | 50 | 0 | 50 | ns |
| Data to Write Time | TDVWH | $\overline{W}$ | 35 | | 35 | | 40 | | 50 | | ns |
| | TDVEH | $\overline{E}$ | 35 | | 35 | | 40 | | 50 | | ns |
| Output Active from End of Write (1) | TWHQX | | 3 | | 3 | | 3 | | 3 | | ns |

Note 1: Parameter guaranteed, but not tested.

***Write Cycle 1***
***$\overline{W}$ Controlled***




***Write Cycle 2***
***$\overline{E}$ Controlled***



## Data Retention Characteristics

**LP Version Only**

| Characteristic | Sym | Test Conditions | Min | Typ | Max | Max | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | 45-70 | 80-150 | |
| Data Retention Voltage | VDD | VDD = 2.0V | 2 | – | -- | -- | V |
| Data Retention Quiescent Current | ICCDR | $\overline{E}$≥ VDD -0.2V | -- | 100 | N/A | 500 | µA |
| Chip Disable to Data Retention Time | TCDR | VIN ≥VDD -0.2V | 0 | -- | -- | -- | ns |
| Operation Recovery Time | TR | or VIN ≤0.2V | 5 | -- | -- | -- | ms |

*Read Cycle Time

## Data Retention
## $\overline{E}$ Controlled