T8502 and T8503 Dual PCM Codecs with Filters

Features

- +5 V only
- Two independent channels
- Pin-selectable receive gain control
- Pin-selectable μ-law or A-law companding
- Automatic powerdown mode
- Low-power, latch-up-free CMOS technology
  — 40 mW/channel typical operating power dissipation
  — 12.5 mW/channel typical standby power dissipation
- Automatic master clock frequency selection
  — 2.048 MHz or 4.096 MHz
- Independent transmit and receive frame strobes
- 2.048 MHz or 4.096 MHz data rate
- On-chip sample and hold, autozero, and precision voltage reference
- Differential architecture for high noise immunity and power supply rejection
- Meets or exceeds ITU-T G.711—G.712 requirements and VF characteristics of D3/D4 (as per Bellcore PUB43801)
- Operating temperature range: –40 °C to +85 °C

Description

The T8502 and T8503 devices are single-chip, two-channel, μ-law/A-law PCM codecs with filters. These integrated circuits provide analog-to-digital and digital-to-analog conversion. They provide the transmit and receive filtering necessary to interface a voice telephone circuit to a time-division multiplexed system. These devices are packaged in both 20-pin SOJs and 20-pin SOGs.

The T8502 differs from the T8503 in its timing mode. The T8502 operates in the delayed timing mode (digital data is valid one clock cycle after frame sync goes high), and the T8503 operates in the nondelayed timing mode (digital data valid when frame sync goes high) (see Figures 5 and 6).

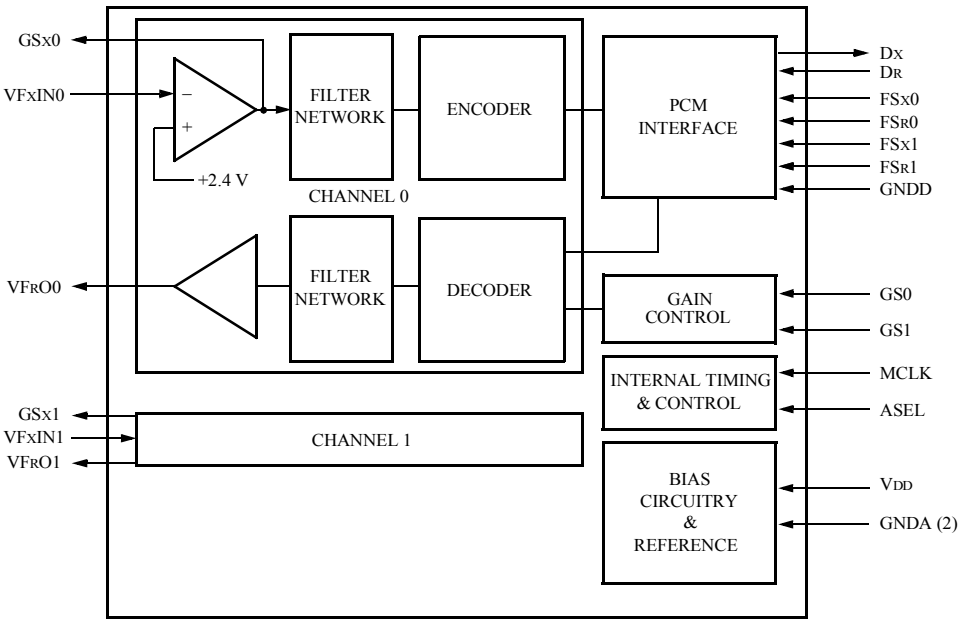

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Figure 1. Block Diagram

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Functional Description

Two channels of PCM data input and output are passed through only two ports, D_X and D_R, so some type of time-slot assignment is necessary. The scheme used here is to utilize a fixed-data rate mode of 32 or 64 time slots corresponding to master clock frequencies of either 2.048 MHz or 4.096 MHz, respectively. Each device has four frame sync (FS_X and FS_R) inputs, one pair for each channel. During a single 125 µs frame, each frame sync input is supplied a single pulse. The timing of the respective frame sync pulse indicates the beginning of the time slot during which the data for that channel is clocked in or out of the device. FS_X and FS_R must be high for a minimum of one master clock cycle. They can be operated independently, or they can be tied together for coincident transmit and receive data transfer. During a frame, channel 0 and 1 transmit frame sync pulses must be separated from each other by one or more time slots. Likewise, channel 0 and 1 receive frame sync pulses must be separated from each other by one or more time slots. Both transmit and receive frame strobes must be derived from master clock, but they do not need to be byte aligned.

A channel is placed in standby mode by removing both FS_X and FS_R for 500 µs. Note, if any one of those pulses (per channel) is removed, operation is indeterminate. Standby mode reduces overall device power consumption by turning off nonessential circuitry. Critical circuits that ensure a fast, quiet powerup are kept active. Master clock need not be active when both channels are in standby mode.

The frequency of the master clock must be either 2.048 MHz or 4.096 MHz. Internal circuitry determines the master clock frequency during the powerup reset interval.

The analog input section in Figure 2 includes an on-chip op amp that is used in conjunction with external, user-supplied resistors to vary encoder passband gain. The feedback resistance (RF) should range from 10 k¾ to 200 k¾, and capacitance from GS_X to ground should be kept to less than 50 pF. The input signal at VF_XIN should be ac coupled. For best performance, the maximum gain of this op amp should be limited to 20 dB or less. Gain in the receive path is selectable via the GS pins as either 0 dB or –3.5 dB.

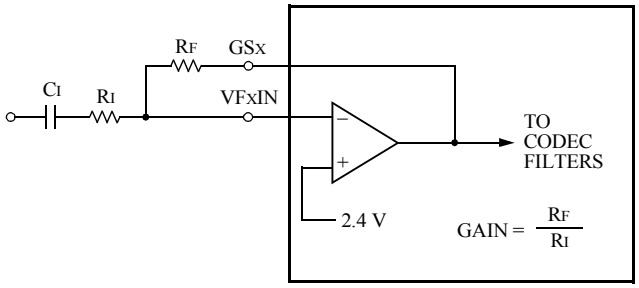

Figure 2. Typical Analog Input Section

Pin Information

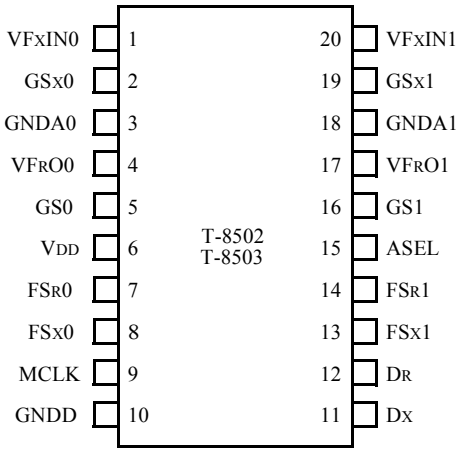

Figure 3. Pin Diagram

Pin Information (continued)

Table 1. Pin Descriptions

Symbol	Pin	Type*	Name/Function
VFXIN1 VFXIN0	20 1	I	**Voice Frequency Transmitter Input.** Analog inverting input to the uncommitted operational amplifier at the transmit filter input. Connect the signal to be digitized to this pin through a resistor RI (see Figure 2).
GSX1 GSX0	19 2	O	**Gain Set for Transmitter.** Output of the transmit uncommitted operational amplifier. The pin is the input to the transmit differential filters. Connect the pin to its corresponding VFXIN through a resistor RF (see Figure 2).
VFRO1 VFRO0	17 4	O	**Voice Frequency Receiver Output.** This pin can drive 2000 ¾ (or greater) loads.
VDD	6	—	**+5 V Power Supply**. This pin should be bypassed to ground with at least 0.1 µF of capacitance as close to the device as possible.
GNDA1 GNDA0	18 3	—	**Analog Grounds**. All ground pins must be connected on the circuit board.
DR	12	I	**Receive PCM Data Input**. The data on this pin is shifted into the device on the falling edges of MCLK. Data is only entered for valid time slots as defined by the FSR inputs.
DX	11	O	**Transmit PCM Data Output**. This pin remains in the high-impedance state except during active transmit time slots. An active transmit time slot is defined as one in which a pulse is present on one of the FSX inputs. Data is shifted out on the rising edge of MCLK.
MCLK	9	I	**Master Clock Input**. The frequency must be 2.048 MHz or 4.096 MHz. This clock serves as the bit clock for all PCM data transfer.
GNDD	10	—	**Digital Ground**. Ground connection for the digital circuitry. All ground pins must be connected on the circuit board.
FSX1 FSX0	13 8	Id	**Transmit Frame Sync**. This signal is an edge trigger and must be high for a minimum of one MCLK cycle. This signal must be derived from MCLK. The division ratio is 1:256 or 1:512 (FSX:MCLK). Each FSX input must have a pulse present at the start of the desired active output time slot. Pulses on FSX inputs must be separated by one or more integer multiples of time slots. If the device is to be used as an A/D converter only, FSX must be tied to FSR. An internal pull-down device is included on each FSX.
FSR1 FSR0	14 7	Id	**Receive Frame Sync**. This signal is an edge trigger and must be high for a minimum of one MCLK cycle. This signal must be derived from MCLK. The division ratio is 1:256 or 1:512 (FSR:MCLK). Each FSR input must have a pulse present at the start of the desired active input time slot. Pulses on FSR inputs must be separated by one or more integer multiples of time slots. If the device is to be used as a D/A converter only, FSR must be tied to FSX. An internal pull-down device is included on each FSR.
GS1 GS0	16 5	Iu	**Gain Selection**. A high or floating state sets the receive path gain at 0 dB; a logic low sets the gain to –3.5 dB. A pull-up device is included.
ASEL	15	Id	**A-Law/µ-Law Select**. A logic low selects µ-law coding. A logic high selects A-law coding. A pull-down device is included.

* Id indicates a pull-down device is included on this lead. Iu indicates a pull-up device is included on this lead.

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of this data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min	Max	Unit
Storage Temperature Range	T_{stg}	–55	150	°C
Power Supply Voltage	V_{DD}	—	6.5	V
Voltage on Any Pin with Respect to Ground	—	–0.5	0.5 + V_{DD}	V
Maximum Power Dissipation (package limit)	P_D	—	600	mW

Handling Precautions

Although protection circuitry has been designed into this device, proper precautions should be taken to avoid exposure to electrostatic discharge (ESD) during handling and mounting. Legerity employs a human-body model (HBM) and a charged-device model (CDM) for ESD-susceptibility testing and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used to define the model. No industry-wide standard has been adopted for CDM. However, a standard HBM (resistance = 1500 ¾, capacitance = 100 pF) is widely used and, therefore, can be used for comparison purposes. The HBM ESD threshold presented here was obtained by using these circuit parameters:

HBM ESD Threshold Voltage	
Device	**Rating**
T8502	>2000
T8503	>2000

Electrical Characteristics

Specifications apply for T_A = –40 °C to +85 °C, V_{DD} = 5 V ± 5%, MCLK = either 2.048 MHz or 4.096 MHz, and GND = 0 V, unless otherwise noted.

dc Characteristics

Table 2. Digital Interface

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Low Voltage	V_{IL}	All digital inputs	—	—	0.8	V
Input High Voltage	V_{IH}	All digital inputs	2.0	—	—	V
Output Low Voltage	V_{OL}	D_X, I_L = 3.2 mA	—	—	0.4	V
Output High Voltage	V_{OH}	D_X, I_L = –3.2 mA	2.4	—	—	V
		D_X, I_L = –320 µA	3.5	—	—	V
Input Current, Pins 9, 12	I_I	GNDD < V_{IN} < V_{DD}	–10	—	10	µA
Input Current, Pins 7, 8, 13, 14, 15	I_I	GNDD < V_{IN} < V_{DD}	2	—	150	µA
Input Current, Pins 5, 16	I_I	GNDD < V_{IN} < V_{DD}	–120	—	–2	µA
Output Current in High-impedance State	I_{OZ}	D_X	–30	<±2	30	µA
Input Capacitance	C_I	—	—	—	5	pF

Electrical Characteristics (continued)

dc Characteristics (continued)

Table 3. Power Dissipation

Power measurements are made at MCLK = 4.096 MHz with outputs unloaded and ASEL and GS[1:0] not connected. Clock and frame sync levels are +5 V and 0 V.

Channels Operational	Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
0	Standby Current	I_{DDS}	MCLK present; $FS_X[1:0] = FS_R[1:0] = 0$ V	—	5	8	mA
1	Partial Standby Current	I_{DDP}	MCLK present; FS pulses present for one channel, $FS_X = FS_R = 0$ V for other channel	—	10	16	mA
2	Powerup Current	I_{DD1}	MCLK, FS pulses present	—	16	23	mA

Transmission Characteristics

Table 4. Analog Interface

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Resistance, VFxIN	R_{VFXI}	0.25 V < VFxI < 4.75 V	1.0	60	—	M¾
Input Leakage Current, VFxIN	I_{BVFXI}	0.25 V < VFxI < 4.75 V	—	0.04	2.4	µA
dc Open-loop Voltage Gain, GSx	A_{VOL}	—	5000	—	—	—
Open-loop Unity Gain Bandwidth, GSx	fo	—	1	3	—	MHz
Load Capacitance, GSx	CL_{X1}	—	—	—	50	pF
Load Resistance, GSx	RL_{X1}	—	10	—	—	k¾
Input Voltage, VFxIN	V_{IX}	Relative to ground	2.25	2.35	2.5	V
Load Resistance, VFrO	RL_{VFRO}	—	2000	—	—	¾
Load Capacitance, VFrO	CL_{VFRO}	—	—	—	100	pF
Output Resistance, VFrO	RO_{VFRO}	0 dBm0, 1020 Hz PCM code applied to D_R	—	—	20	¾
		Standby mode $FS_X = FS_R = 0$ V for channel under test	3000	—	10000	¾
Output Voltage, VFrO	V_{OR}	Alternating ± zero µ-law PCM code applied to D_R	2.25	2.38	2.5	V
Output Voltage, VFrO, Standby	VO_{RPD}	Standby mode $FS_X = FS_R = 0$ V for channel under test, no load	2.0	2.35	2.65	V
Output Voltage Swing, VFrO	V_{SWR}	RL = 2000 ¾	3.2	—	—	Vp-p

Transmission Characteristics (continued)

ac Transmission Characteristics

Unless otherwise noted, the analog input is a 0 dBm0, 1020 Hz sine wave; the input amplifier is set for unity gain. The digital input is a PCM bit stream equivalent to that obtained by passing a 0 dBm0, 1020 Hz sine wave through an ideal encoder. The output level is sin(x)/x-corrected.

Table 5. Absolute Gain

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Encoder Milliwatt Response (transmit gain tolerance)	EmW	Signal input of 0.775 Vrms, μ-law or A-law	0 °C to 85 °C	–0.20	—	0.20	dBm0
			–40 °C to +85 °C	–0.25	—	0.25	dBm0
Decoder Milliwatt Response (receive gain tolerance)	DmW	Measured relative to 0.775 Vrms μ-law or A-law, PCM input of 0 dBm0 1020 Hz, RL = 10 k¾	0 °C to 85 °C	–0.20	—	0.20	dBm0
			–40 °C to +85 °C	–0.25	—	0.25	dBm0
Relative Decoder Gain Variation Referenced to DmW	RGR	Decoder gain at –3.5 dB (GS = 0)	–40 °C to +85 °C	–0.15	—	0.15	dB

Table 6. Gain Tracking

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Transmit Gain Tracking Error Sinusoidal Input μ-Law/A-Law	GTX	+3 dBm0 to –37 dBm0	–0.25	—	0.25	dB
		–37 dBm0 to –50 dBm0	–0.50	—	0.50	dB
Receive Gain Tracking Error Sinusoidal Input μ-Law/A-Law	GTR	+3 dBm0 to –37 dBm0	–0.25	—	0.25	dB
		–37 dBm0 to –50 dBm0	–0.50	—	0.50	dB

Table 7. Distortion

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Transmit Signal to Distortion	SDX	μ-law 3 dBm0 ≤ VFXI ≤ –30 dBm0	36	—	—	dB
		A-law 3 dBm0 ≤ VFXI ≤ –30 dBm0	35	—	—	dB
		μ-law –30 dBm0 ≤ VFXI ≤ –40 dBm0	30	—	—	dB
		A-law –30 dBm0 ≤ VFXI v –40 dBm0	29	—	—	dB
		μ-law –40 dBm0 ≤ VFXI ≤ –45 dBm0	25	—	—	dB
		A-law –40 dBm0 ≤ VFXI ≤ –45 dBm0	25	—	—	dB
Receive Signal to Distortion	SDR	μ-law 3 dBm0 ≤ VFRO ≤ –30 dBm0	36	—	—	dB
		A-law 3 dBm0 ≤ VFRO ≤ –30 dBm0	35	—	—	dB
		μ-law –30 dBm0 ≤ VFRO ≤ –40 dBm0	30	—	—	dB
		A-law –30 dBm0 ≤ VFRO ≤ –40 dBm0	29	—	—	dB
		μ-law –40 dBm0 ≤ VFRO ≤ –45 dBm0	25	—	—	dB
		A-law –40 dBm0 ≤ VFRO ≤ –45 dBm0	25	—	—	dB
Single Frequency Distortion, Transmit	SFDX	200 Hz—3400 Hz, 0 dBm0 input, output any other single frequency ≤ 3400 Hz	—	—	–38	dBm0
Single Frequency Distortion, Receive	SFDR	200 Hz—3400 Hz, 0 dBm0 input, output any other single frequency ≤ 3400 Hz	—	—	–40	dBm0
Intermodulation Distortion	IMD	Transmit or receive, two frequencies in the range (300 Hz—3400 Hz) at –6 dBm0	—	—	–42	dBm0

Transmission Characteristics (continued)

ac Transmission Characteristics (continued)

Table 8. Envelope Delay Distortion

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Tx Delay, Absolute	D_{XA}	f = 1600 Hz	—	280	300	µs
Tx Delay, Relative to 1600 Hz	D_{XR}	f = 500 Hz—600 Hz	—	—	220	µs
		f = 600 Hz—800 Hz	—	—	145	µs
		f = 800 Hz—1000 Hz	—	—	75	µs
		f = 1000 Hz—1600 Hz	—	—	40	µs
		f = 1600 Hz—2600 Hz	—	—	75	µs
		f = 2600 Hz—2800 Hz	—	—	105	µs
		f = 2800 Hz—3000 Hz	—	—	155	µs
Rx Delay, Absolute	D_{RA}	f = 1600 Hz	—	190	200	µs
Rx Delay, Relative to 1600 Hz	D_{RR}	f = 500 Hz—1000 Hz	–40	—	—	µs
		f = 1000 Hz—1600 Hz	–30	—	—	µs
		f = 1600 Hz—2600 Hz	—	—	90	µs
		f = 2600 Hz—2800 Hz	—	—	125	µs
		f = 2800 Hz—3000 Hz	—	—	175	µs
Round-trip Delay, Absolute	D_{RTA}	Any time slot/channel to any time slot/channel f = 1600 Hz	—	470	600	µs

Overload Compression

Figure 4 shows the region of operation for encoder signal levels above the reference input power (0 dBm0).

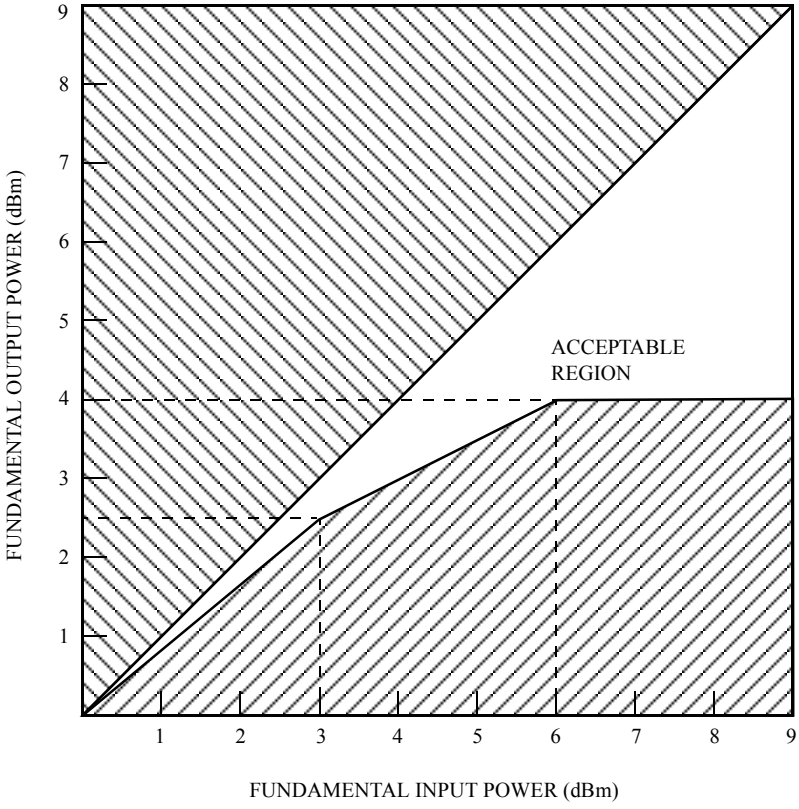

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Figure 4. Overload Compression

Transmission Characteristics (continued)

ac Transmission Characteristics (continued)

Table 9. Noise

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Transmit Noise, μ-Law	N_{XC}	—	—	—	18	dBrnC0
		Input amplifier gain = 20 dB	—	—	19	dBrnC0
Transmit Noise, A-Law	N_{XP}	—	—	—	–68	dBm0p
Receive Noise, μ-Law	N_{RC}	PCM code is alternating positive and negative zero	—	—	13	dBrnC0
Receive Noise, A-Law	N_{RP}	PCM code is A-law positive one	—	—	–75	dBm0p
Noise, Single Frequency, f = 0 kHz—100 kHz	N_{RS}	VF_XIN = 0 Vrms, measurement at VF_RO, D_R = D_X	—	—	–53	dBm0
Power Supply Rejection Transmit	PSR_X	V_{DD} = 5.0 Vdc + 100 mVrms: f = 0 kHz—4 kHz f = 4 kHz—50 kHz	 36 30	 — —	 — —	 dB dB
Power Supply Rejection Receive	PSR_X	PCM code is positive one LSB V_{DD} = 5.0 Vdc + 100 mVrms: f = 0 kHz—4 kHz f = 4 kHz—25 kHz f = 25 kHz—50 kHz	 36 40 30	 — — —	 — — —	 dB dB dB
Spurious Out-of-band Signals at VF_RO Relative to Input	SOS	0 dBm0, 300 Hz—3400 Hz input PCM code applied: 4600 Hz—7600 Hz 7600 Hz—8400 Hz 8400 Hz—50 kHz	 — — —	 — — —	 –30 –40 –30	 dB dB dB

Table 10. Receive Gain Relative to Gain at 1.02 kHz

Frequency (Hz)	Min	Typ	Max	Unit
Below 3000	–0.150	±0.04	0.150	dB
3140	–0.570	±0.04	0.150	dB
3380	–0.735	–0.58	0.010	dB
3860	—	–10.7	–9.4	dB
4600 and above	—	—	–28	dB

Table 11. Transmit Gain Relative to Gain at 1.02 kHz

Frequency (Hz)	Min	Typ	Max	Unit
16.67	—	–35	–30	dB
40	—	–34	–26	dB
50	—	–36	–30	dB
60	—	–50	–30	dB
200	–1.8	–0.5	0	dB
300 to 3000	–0.150	±0.04	0.150	dB
3140	–0.570	±0.04	0.150	dB
3380	–0.735	–0.58	0.010	dB
3860	—	–10.7	–9.4	dB
4600 and above	—	—	–32	dB

Transmission Characteristics (continued)

ac Transmission Characteristics (continued)

Table 12. Interchannel Crosstalk (Between Channels) R_F = ≤ 200 k¾ (See Note.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Transmit to Receive Crosstalk 0 dBm0 Transmit Levels	CT_{XX-RY}	f = 300 Hz—3400 Hz idle PCM code for channel under test; 0 dBm0 into other channel VF_XIN	—	–100	–77	dB
Receive to Transmit Crosstalk 0 dBm0 Receive Levels	CT_{RX-XY}	f = 300 Hz—3400 Hz VF_XIN = 0 Vrms for channel under test; 0 dBm0 code level on other channel D_R	—	–92	–77	dB
Transmit to Transmit Crosstalk 0 dBm0 Transmit Levels	CT_{XX-XY}	f = 300 Hz—3400 Hz VF_XIN = 0 Vrms for channel under test; 0 dBm0 into other channel VF_XIN	—	–90	–77	dB
Receive to Receive Crosstalk 0 dBm0 Receive Levels	CT_{RX-RY}	f = 300 Hz—3400 Hz idle PCM code for channel under test; 0 dBm0 code level on other channel D_R	—	–102	–77	dB

Table 13. Intrachannel Crosstalk (Within Channels) R_F = ≤ 200 k¾ (See Note.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Transmit to Receive Crosstalk 0 dBm0 Transmit Levels	CT_{XX-RX}	f = 300 Hz—3400 Hz idle PCM code for channel under test; 0 dBm0 into VF_XIN	—	–80	–70	dB
Receive to Transmit Crosstalk 0 dBm0 Receive Levels	CT_{RX-XX}	f = 300 Hz—3400 Hz VF_XIN = 0 Vrms for channel under test; 0 dBm0 code level on D_R	—	–88	–70	dB

Note: For Tables 12 and 13, crosstalk into the transmit channels (VF_XIN) can be significantly affected by parasitic capacitive feeds from GS_X and VF_RO outputs. PWB layouts should be arranged to keep these parasitics low. The resistor value of R_F (from GS_X to VF_XIN) should also be kept as low as possible (while maintaining the load on GS_X above 10 k¾, per Table 4) to minimize crosstalk.

Timing Characteristics

Table 14. Clock Section (See Figures 5 and 6.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
tMCHMCL1	Clock Pulse Width	—	97	—	—	ns
tMCH1MCH2 tMCL2MCL1	Clock Rise and Fall Time	—	0	—	15	ns

Table 15. T8502 Transmit Section (See Figure 5.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
tMCHDV	Data Enabled on TS Entry	$0 < C_{LOAD} < 100$ pF	0	—	60	ns
tMCHDV1	Data Delay from MC	$0 < C_{LOAD} < 100$ pF	0	—	60	ns
tMCLDZ*	Data Float on TS Exit	$C_{LOAD} = 0$	10	—	100	ns
tFSHMCL	Frame-sync Hold Time	—	50	—	—	ns
tMCLFSH	Frame-sync High Setup	—	50	—	—	ns
tFSLMCL	Frame-sync Low Setup	—	50	—	—	ns
tFSHFSL	Frame-sync Pulse Width	—	0.1	—	125 – tMCHMCH	µs

* Timing parameter tMCLDZ is referenced to a high-impedance state.

Table 16. T8503 Transmit Section (See Figure 6.)

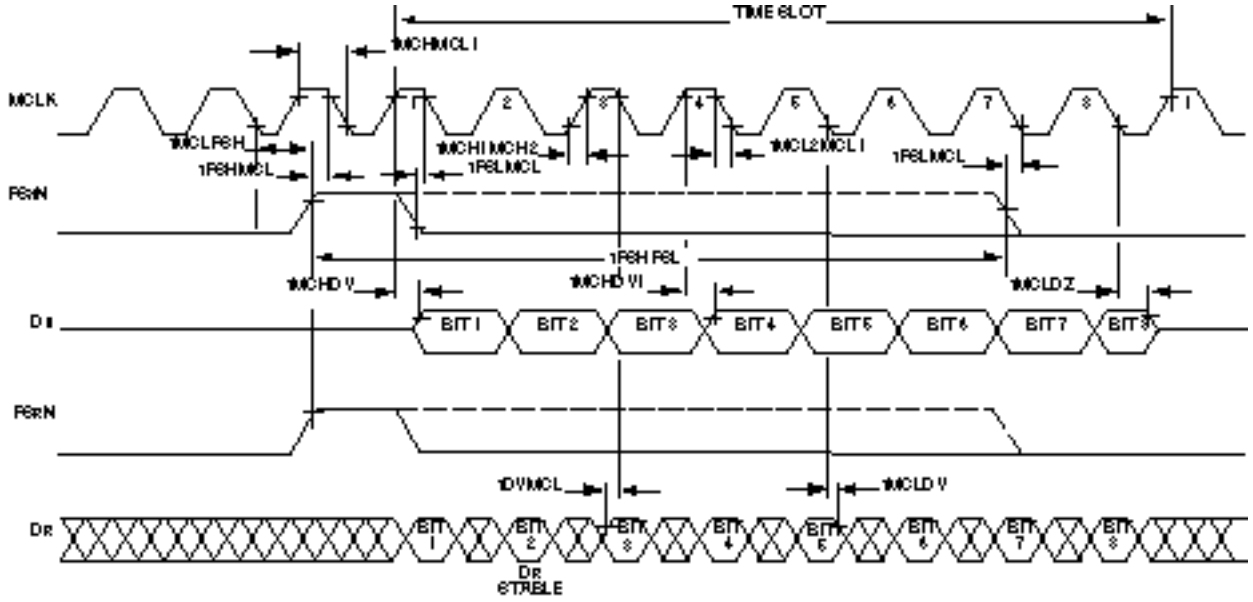
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
tFSHDV	Data Enabled on TS Entry	$0 < C_{LOAD} < 100$ pF	0	—	80	ns
tMCHDV1	Data Delay from FSx	$0 < C_{LOAD} < 100$ pF	0	—	60	ns
tMCHDZ*	Data Float on TS Exit	$C_{LOAD} = 0$	0	—	30	ns
tFSHMCL	Frame-sync Hold Time	—	50	—	—	ns
tMCLFSH	Frame-sync High Setup	—	50	—	—	ns
tFSLMCL	Frame-sync Low Setup	—	50	—	—	ns
tFSHFSL	Frame-sync Pulse Width	—	0.1	—	125 – tMCHMCH	µs

* Timing parameter tMCHDZ is referenced to a high-impedance state.

Table 17. T8502 and T8503 Receive Section (See Figures 5 and 6.)

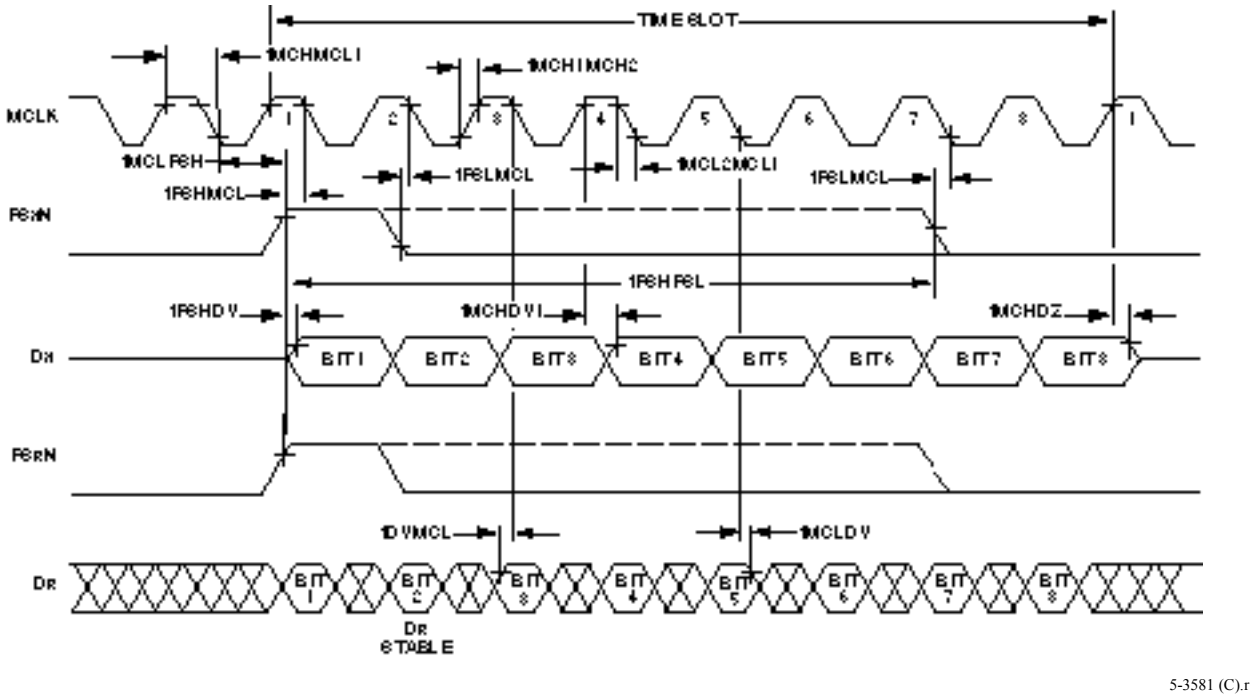
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
tDVMCL	Receive Data Setup	—	30	—	—	ns
tMCLDV	Receive Data Hold	—	15	—	—	ns

Timing Characteristics (continued)



Note: FSX and FSR do not need to be coincident.

Figure 5. T8502 Transmit and Receive Timing



Note: FSX and FSR do not need to be coincident.

Figure 6. T8503 Transmit and Receive Timing

Applications

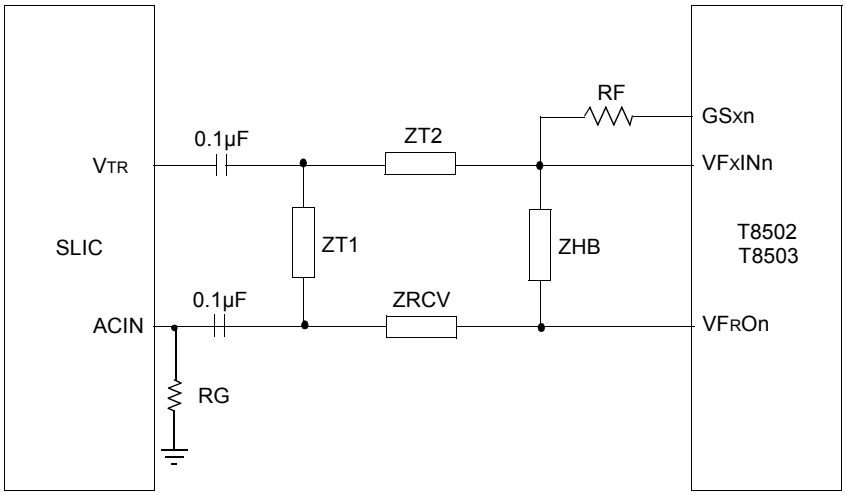


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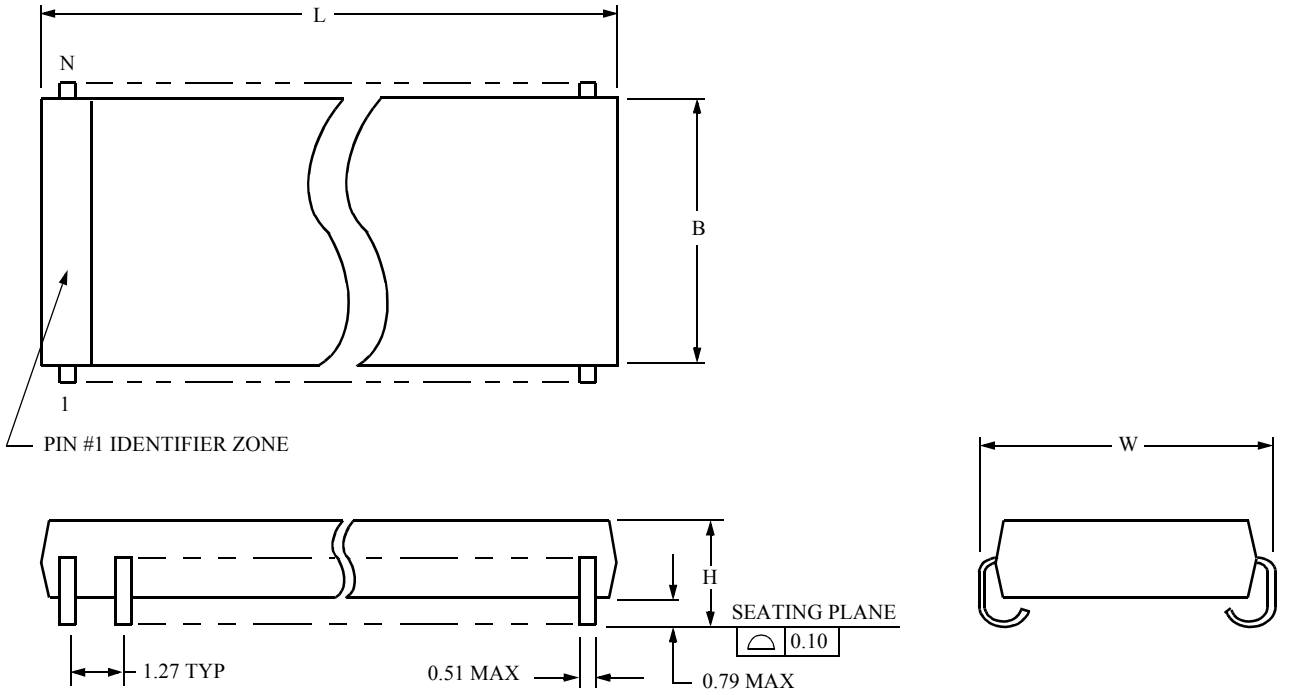
Figure 7. Typical T8502 and T8503/SLIC Interconnection

Outline Diagrams

20-Pin SOJ

Dimensions are in millimeters.

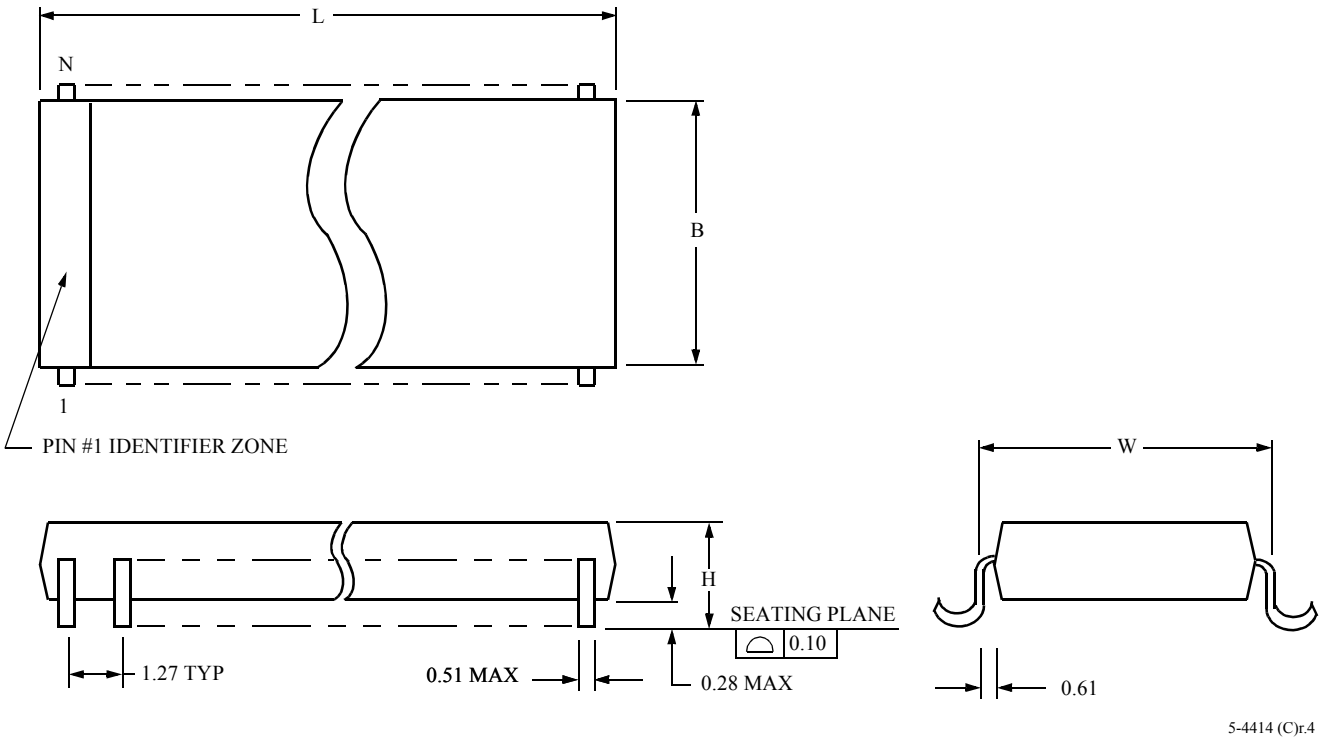


Number of Pins (N)	Maximum Length (L)	Maximum Width Without Leads (B)	Maximum Width Including Leads (W)	Maximum Height Above Board (H)
20	12.95	7.62	8.81	3.18

Outline Diagrams (continued)

20-Pin SOG

Dimensions are in millimeters.



Number of Pins (N)	Maximum Length (L)	Maximum Width Without Leads (B)	Maximum Width Including Leads (W)	Maximum Height Above Board (H)
20	13.00	7.62	10.64	2.67

Ordering Information

Device Part No.	Package	Temperature	Comcode
T-8502 - - EL2-D	20-Pin SOJ	–40 °C to +85 °C	108295908
T-8502 - - EL2-DT	20-Pin SOJ Tape & Reel	–40 °C to +85 °C	108295916
T-8502 - - GL2-D	20-Pin SOG	–40 °C to +85 °C	108295924
T-8502 - - GL2-DT	20-Pin SOG Tape & Reel	–40 °C to +85 °C	108295932
T-8503 - - EL2-D	20-Pin SOJ	–40 °C to +85 °C	108295940
T-8503 - - EL2-DT	20-Pin SOJ Tape & Reel	–40 °C to +85 °C	108295957
T-8503 - - GL2-D	20-Pin SOG	–40 °C to +85 °C	108295965
T-8503 - - GL2-DT	20-Pin SOG Tape & Reel	–40 °C to +85 °C	108295973

Note: All parts are shipped in dry bag.

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