NEC

MOS INTEGRATED CIRCUIT

μPD16405

120-OUTPUT TFT-LCD SOURCE DRIVER

DESCRIPTION

The μPD16405 is a source driver for a TFT liquid-crystal panel. The internal configuration comprises a multiplexer circuit which is compatible with various kinds of color filters, a shift register which generates the sampling timing, and a sample-and-hold circuit which samples the analog voltage. There are two sample-and-hold circuits which perform sampling and holding alternately. Thus, it is ideal for a line-sequential scanning type color liquid-crystal TV. Low power consumption can be achieved by stopping driver operation during vertical intervals.

Either the μPD16422 or μPD16446 (slim type) can be used as the gate driver.

FEATURES

- Two on-chip sample-and-hold circuits
- Wide dynamic range (10.5 V MIN., at V_{DD2} = 15 V)
- Small output deviation between pins (deviation between chip pins: ±50 mV MAX.)
- Stripe, mosaic, delta array color filter compatibility using the on-chip multiplexer
- On-chip power save circuit
- Switchable between right and left shift using the R/L pin
- High-density mounting capability (TCP)

ORDERING INFORMATION

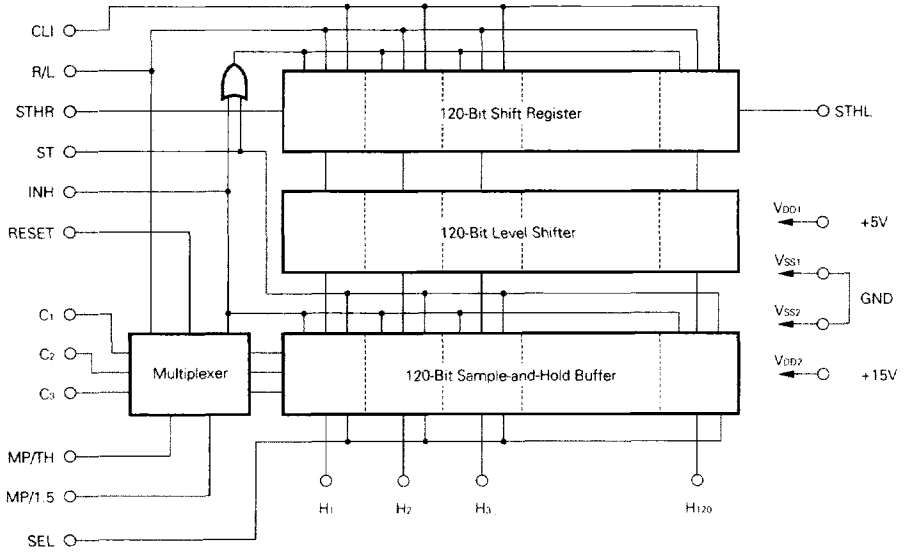
Part Number	Package	Quality Grade
μPD16405N-×××	TCP (TAB package)	Standard

TCP packages must be custom ordered and so consult with your NEC sales representative.

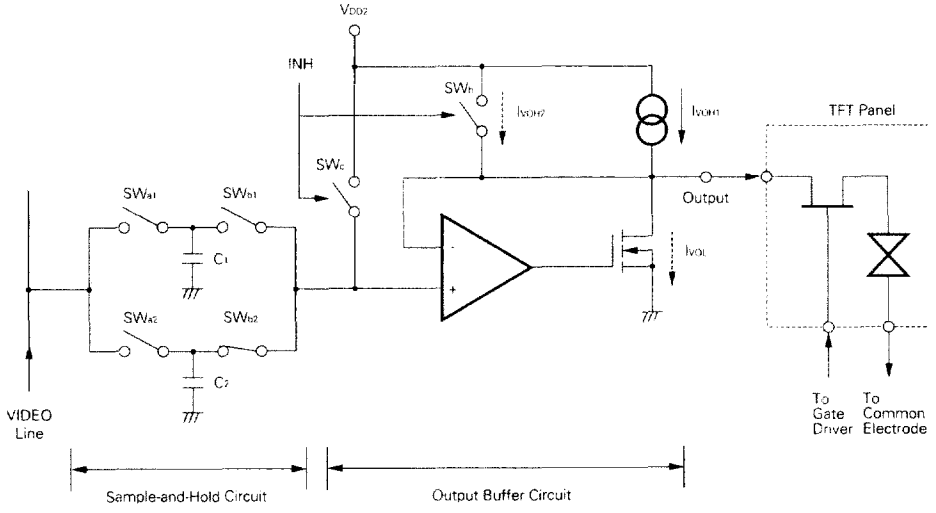
Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

Document No. IC-3296
(O. D. No. IC-8461)
Date Published December 1993 P
Printed in Japan

BLOCK DIAGRAM



SAMPLE-AND-HOLD CIRCUIT AND OUTPUT CIRCUIT



PIN DESCRIPTION (1/2)

PAD No.	Symbol	Pin Name	Function Description
6 5 4	C_1 C_2 C_3	Video signal input	Video signal (analog) input. The R, G, and B video signals are input. The input video signals pass through the multiplexer and and after they are sampled and held, they are output from the video signal outputs H_1 to H_{120}.
21 to 140	H_1 to H_{120}	Video signal output	Video signal output pins. The sampled-and-held signals are output during the horizontal period.
20 1	STHR STHL	Cascade pulse input	Sample-and-hold timing start pulse input pins. For a right shift, STHR is the input pin and STHL is the output pin, and for a left shift, STHL is the input pin and the STHR is the output pin. After INH rises, the start pulse should be input after 4 clocks.
19	SEL	Output retention current selection input	Video signal high-level output current (output retention current) is switched. SEL = H ; I_{VOH} = -30 μA TYP. SEL = L ; I_{VOH} = -8 μA TYP.
16	CLI	Shift clock input	At the rising edge, the start pulse is read, and at each edge, the video signal is sampled in the sample-and-hold circuit.
15	INH	Inhibit input	When this pin is high level, the video signal output is driven high and the pixels in the panel are pre-charged. At the falling edge it switches the multiplexer and the two sample-and-hold circuits.
13	RESET	Reset input	When this pin is high level, the selection counter of the multiplexer circuit and two sample-and-hold circuits are reset. After a reset, the multiplexer is OFF, therefore the video signal should be input after INH pulse is input one time. If the video signal is input without inputting the INH pulse, sampling is not performed.
14	ST	Power save input	When this pin is driven high, all of the video signal output is driven high, and the bias current of the analog circuit is reduced. By driving it high during the vertical interval, it is possible to reduce the consumption current.
10	MP/TH	Multiplexer circuit switching input (1)	Using combinations of MP/TH and MP/1.5, the multiplexer is compatible with three different kinds of color filter arrays. Mode / MP/TH / MP/1.5 Mosaic array / H / L Delta array / H / H Stripe array / L / L Do not select the combination MP/TH = L and MP/1.5 = H.
11	MP/1.5	Multiplexer circuit switching input (2)	
12	R/L	Shift direction switching input	R/L = H: Right shift: STHR → H_1 → H_{120} → STHL R/L = L: Left shift: STHL → H_{120} → H_1 → STHR

PIN DESCRIPTION (2/2)

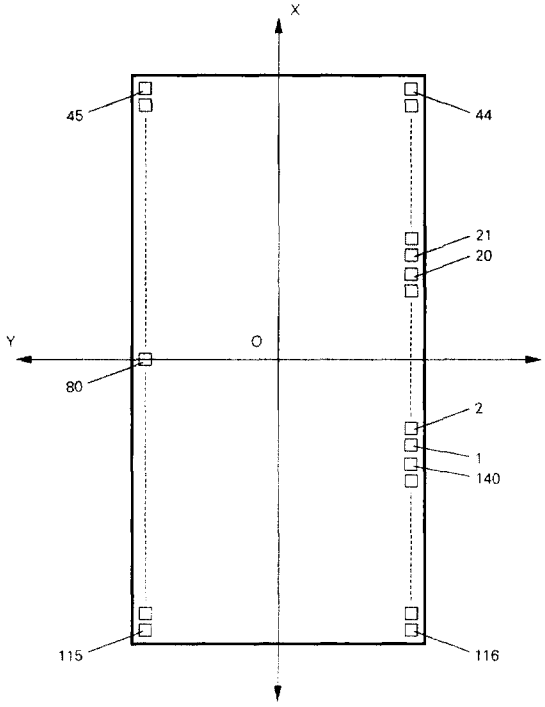
PAD No.	Symbol	Pin Name	Function Description
9	V_{DD1}	Logic system power supply	5 V ±10 %
3, 7	V_{DD2}	Driver system power supply	12 V to 18 V
2, 8, 18	V_{SS}	Ground	Should be connected to the system ground.

Cautions

1. **To prevent latch up breakdown, the power should be turned ON in the order, V_{DD1}, logic input, V_{DD2}, video signal input. It should be turned OFF in the opposite order. This relationship should be followed during transition periods as well.**
2. **The delay time between the clock and the internal sampling pulse SHPn is approximately 15 to 30 ns (typical distribution at V_{DD1} = 5 V, and 25 °C). Therefore, the video input signal should be delayed the amount of the delay time after the clock.**
3. **Be sure not to change the video input signal during a sampling period. The video input frequency of this product is designed to be 3.3 MHz maximum, and so if a faster video signal is input, errors in the display may occur.**

PAD LOCATION

Chip Size: 11.40 × 3.03 mm²



PAD COORDINATES (UNIT: μm) (1/2)

PAD No.	Symbol	X-Coordinate	Y-Coordinate	PAD No.	Symbol	X-Coordinate	Y-Coordinate
1	STHL	−1345.75	−1375.62	43	H_{23}	+5108.12	−1375.62
2	V_{SS2}	−1174.75	−1375.62	44	H_{24}	+5258.12	−1375.62
3	V_{DD2}	−1003.75	−1375.62	45	H_{25}	+5258.12	+1375.62
4	C_3	−795.50	−1375.62	46	H_{26}	+5108.12	+1375.62
5	C_2	−645.50	−1375.62	47	H_{27}	+4958.12	+1375.62
6	C_1	−495.50	−1375.62	48	H_{28}	+4808.12	+1375.62
7	V_{DD2}	−345.50	−1375.62	49	H_{29}	+4658.12	+1375.62
8	V_{SS1}	−188.87	−1375.62	50	H_{30}	+4508.12	+1375.62
9	V_{DD1}	−38.87	−1375.62	51	H_{31}	+4358.12	+1375.62
10	MP/TH	+111.12	−1375.62	52	H_{32}	+4208.12	+1375.62
11	MP/1.5	+261.12	−1375.62	53	H_{33}	+4058.12	+1375.62
12	R/L	+411.12	−1375.62	54	H_{34}	+3908.12	+1375.62
13	RESET	+561.12	−1375.62	55	H_{35}	+3758.12	+1375.62
14	ST	+711.12	−1375.62	56	H_{36}	+3608.12	+1375.62
15	INH	+861.12	−1375.62	57	H_{37}	+3458.12	+1375.62
16	CLI	+1011.12	−1375.62	58	H_{38}	+3308.12	+1375.62
17	V_{DD2}	+1161.12	−1375.62	59	H_{39}	+3158.12	+1375.62
18	V_{SS2}	+1311.12	−1375.62	60	H_{40}	+3008.12	+1375.62
19	SEL	+1461.12	−1375.62	61	H_{41}	+2858.12	+1375.62
20	STHR	+1611.12	−1375.62	62	H_{42}	+2708.12	+1375.62
21	H_1	+1808.12	−1375.62	63	H_{43}	+2558.12	+1375.62
22	H_2	+1958.12	−1375.62	64	H_{44}	+2408.12	+1375.62
23	H_3	+2108.12	−1375.62	65	H_{45}	+2258.12	+1375.62
24	H_4	+2258.12	−1375.62	66	H_{46}	+2108.12	+1375.62
25	H_5	+2408.12	−1375.62	67	H_{47}	+1958.12	+1375.62
26	H_6	+2558.12	−1375.62	68	H_{48}	+1808.12	+1375.62
27	H_7	+2708.12	−1375.62	69	H_{49}	+1658.12	+1375.62
28	H_8	+2858.12	−1375.62	70	H_{50}	+1508.12	+1375.62
29	H_9	+3008.12	−1375.62	71	H_{51}	+1358.12	+1375.62
30	H_{10}	+3158.12	−1375.62	72	H_{52}	+1208.12	+1375.62
31	H_{11}	+3308.12	−1375.62	73	H_{53}	+1058.12	+1375.62
32	H_{12}	+3458.12	−1375.62	74	H_{54}	+908.12	+1375.62
33	H_{13}	+3608.12	−1375.62	75	H_{55}	+758.12	+1375.62
34	H_{14}	+3758.12	−1375.62	76	H_{56}	+608.12	+1375.62
35	H_{15}	+3908.12	−1375.62	77	H_{57}	+458.12	+1375.62
36	H_{16}	+4058.12	−1375.62	78	H_{58}	+308.12	+1375.62
37	H_{17}	+4208.12	−1375.62	79	H_{59}	+158.12	+1375.62
38	H_{18}	+4358.12	−1375.62	80	H_{60}	+8.12	+1375.62
39	H_{19}	+4508.12	−1375.62	81	H_{61}	−141.87	+1375.62
40	H_{20}	+4658.12	−1375.62	82	H_{62}	−291.87	+1375.62
41	H_{21}	+4808.12	−1375.62	83	H_{63}	−441.87	+1375.62
42	H_{22}	+4958.12	−1375.62	84	H_{64}	−591.87	+1375.62

PAD COORDINATES (UNIT: μm) (2/2)

PAD No.	Symbol	X-Coordinate	Y-Coordinate	PAD No.	Symbol	X-Coordinate	Y-Coordinate
85	H_{65}	-741.87	+1375.62	113	H_{93}	-4941.87	+1375.62
86	H_{66}	-891.87	+1375.62	114	H_{94}	-5091.87	+1375.62
87	H_{67}	-1041.87	+1375.62	115	H_{95}	-5241.87	+1375.62
88	H_{68}	-1191.87	+1375.62	116	H_{96}	-5241.87	-1375.62
89	H_{69}	-1341.87	+1375.62	117	H_{97}	-5091.87	-1375.62
90	H_{70}	-1491.87	+1375.62	118	H_{98}	-4941.87	-1375.62
91	H_{71}	-1641.87	+1375.62	119	H_{99}	-4791.87	-1375.62
92	H_{72}	-1791.87	+1375.62	120	H_{100}	-4641.87	-1375.62
93	H_{73}	-1941.87	+1375.62	121	H_{101}	-4491.87	-1375.62
94	H_{74}	-2091.87	+1375.62	122	H_{102}	-4341.87	-1375.62
95	H_{75}	-2241.87	+1375.62	123	H_{103}	-4194.87	-1375.62
96	H_{76}	-2391.87	+1375.62	124	H_{104}	-4041.87	-1375.62
97	H_{77}	-2541.87	+1375.62	125	H_{105}	-3891.87	-1375.62
98	H_{78}	-2691.87	+1375.62	126	H_{106}	-3741.87	-1375.62
99	H_{79}	-2841.87	+1375.62	127	H_{107}	-3591.87	-1375.62
100	H_{80}	-2991.87	+1375.62	128	H_{108}	-3441.87	-1375.62
101	H_{81}	-3141.87	+1375.62	129	H_{109}	-3291.87	-1375.62
102	H_{82}	-3291.87	+1375.62	130	H_{110}	-3141.87	-1375.62
103	H_{83}	-3441.87	+1375.62	131	H_{111}	-2991.87	-1375.62
104	H_{84}	-3591.87	+1375.62	132	H_{112}	-2841.87	-1375.62
105	H_{85}	-3741.87	+1375.62	133	H_{113}	-2691.87	-1375.62
106	H_{86}	-3891.87	+1375.62	134	H_{114}	-2541.87	-1375.62
107	H_{87}	-4041.87	+1375.62	135	H_{115}	-2391.87	-1375.62
108	H_{88}	-4191.87	+1375.62	136	H_{116}	-2241.87	-1375.62
109	H_{89}	-4341.87	+1375.62	137	H_{117}	-2091.87	-1375.62
110	H_{90}	-4491.87	+1375.62	138	H_{118}	-1941.87	-1375.62
111	H_{91}	-4641.87	+1375.62	139	H_{119}	-1791.87	-1375.62
112	H_{92}	-4791.87	+1375.62	140	H_{120}	-1641.87	-1375.62

DESCRIPTION OF FUNCTIONS

1. MULTIPLEXER CIRCUIT

The R, G, and B video signals that are input to pins C_1, C_2, and C_3 according to the pixel array of the liquid-crystal display are switched and output to pins H_1 to H_{120}. It is possible to select either a strip array, mosaic array, or delta array according to the combination of pins MP/TH and MP/1.5

1.1 STRIPE ARRAY MODE (MP/TH = L, MP/1.5 = L)

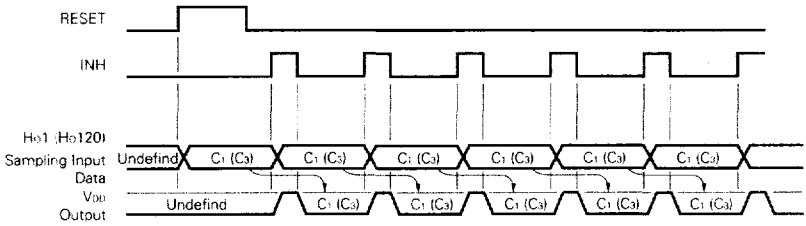
Stripe array can be handled. In this mode, the multiplexer circuit is set to through.

Operation Table

Line No. (No. of INH)	RESET	INH	H_1 (H_{120})	H_2 (H_{119})	H_3 (H_{118})	H_4 (H_{117})	H_{119} (H_2)	H_{120} (H_1)
0	H	L	Sampling C_1 (C_3)	Sampling C_2 (C_2)	Sampling C_3 (C_1)	Sampling C_1 (C_3)	Sampling C_2 (C_3)	Sampling C_3 (C_1)
1	L	↑	Output C_1 (C_3)	Output C_2 (C_2)	Output C_3 (C_1)	Output C_1 (C_3)	Output C_2 (C_3)	Output C_3 (C_1)
2	L	↑	Output C_1 (C_3)	Output C_2 (C_2)	Output C_3 (C_1)	Output C_1 (C_3)	Output C_2 (C_3)	Output C_3 (C_1)
⋮	⋮	⋮	⋮		⋮	⋮	⋮	⋮

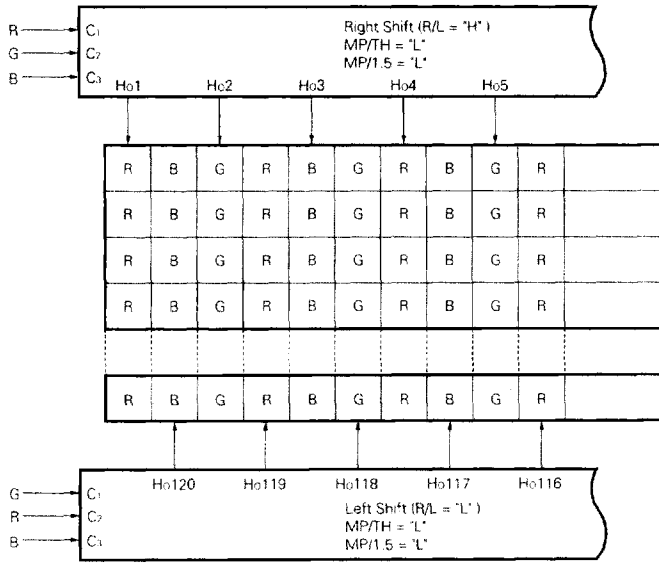
Values inside the brackets ( ) are for left shift.

Timing Chart for Stripe Array



The timing is the same for pins other than H_{01} (H_{0120}) For information about the data, refer to the output status (operation table).

Example of Pixel Layout Multiplexer Operation for Stripe Array



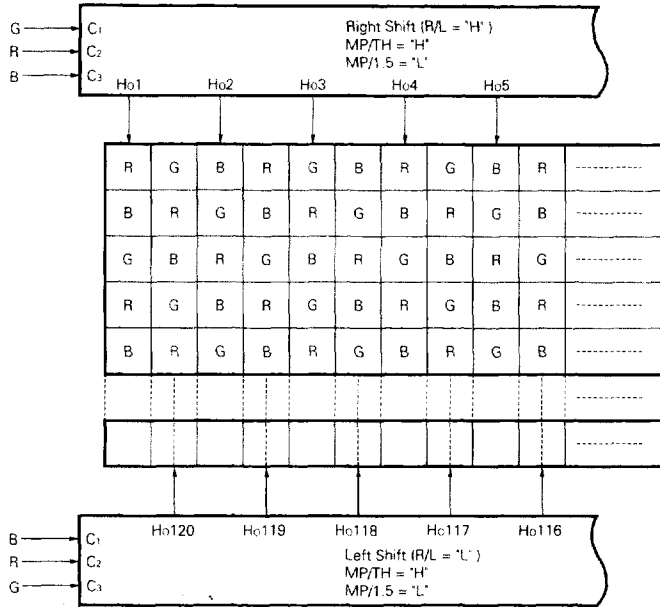
1.2 MOSAIC ARRAY MODE (MP/TH = H, MP/1.5 = L)

Mosaic array (1 pixel shift) can be handled.

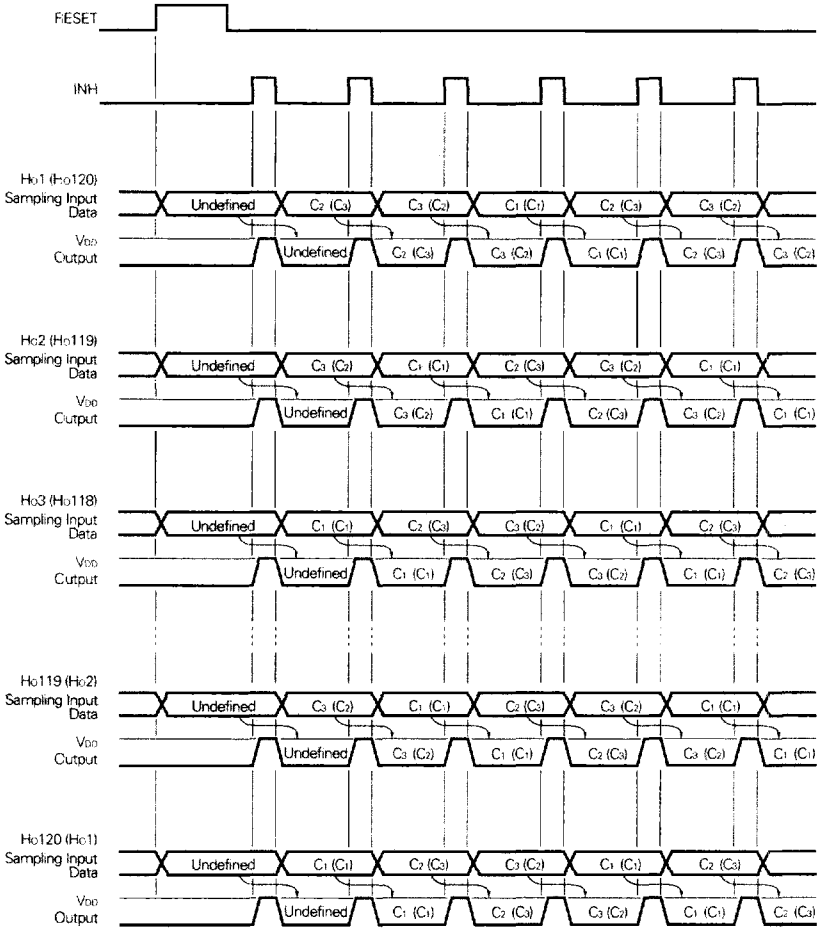
Operation Table

Line No. (No. of INH)	RESET	INH	H_1 (H_{120})	H_2 (H_{119})	H_3 (H_{118})	H_4 (H_{117})	H_{119} (H_2)	H_{120} (H_1)
0	H	L	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
1	L	↑	Sampling C_2 (C_3)	Sampling C_3 (C_2)	Sampling C_1 (C_1)	Sampling C_2 (C_3)	Sampling C_3 (C_2)	Sampling C_1 (C_1)
2	L	↑	Output C_2 (C_3)	Output C_3 (C_2)	Output C_1 (C_1)	Output C_2 (C_3)	Output C_3 (C_2)	Output C_1 (C_1)
3	L	↑	Output C_3 (C_2)	Output C_1 (C_1)	Output C_2 (C_3)	Output C_3 (C_2)	Output C_1 (C_2)	Output C_2 (C_3)
4	L	↑	Output C_1 (C_1)	Output C_2 (C_3)	Output C_3 (C_2)	Output C_1 (C_1)	Output C_2 (C_2)	Output C_3 (C_2)
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮

Values in brackets () are for a left shift.


G
R
B
C1
C2
C3
Right Shift (R/L = "H")
MP/TH = "H"
MP/1.5 = "L"
Ho1
Ho2
Ho3
Ho4
Ho5
R G B R G B R G B R
B R G B R G B R G B
G B R G B R G B R G
R G B R G B R G B R
B R G B R G B R G B
Ho120
Ho119
Ho118
Ho117
Ho116
B
R
G
C1
C2
C3
Left Shift (R/L = "L")
MP/TH = "H"
MP/1.5 = "L"

Timing Chart for Mosaic Array



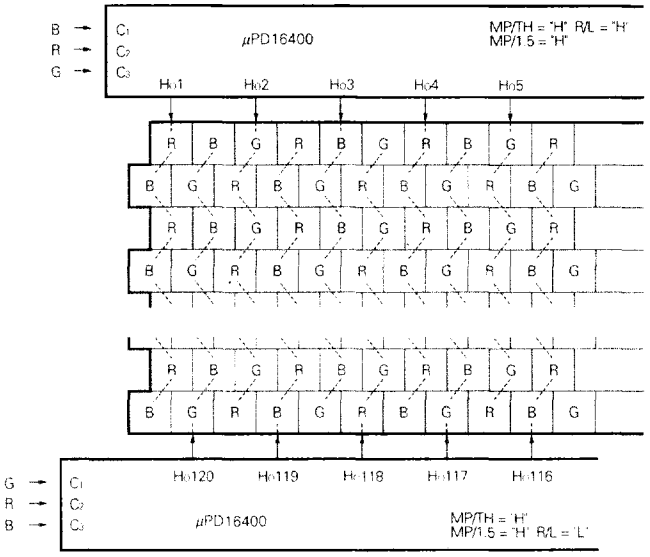
1.3 DELTA ARRAY MODE (MP/TH = H, MP/1.5 = H)

Delta array (half pixel shift) can be handled.

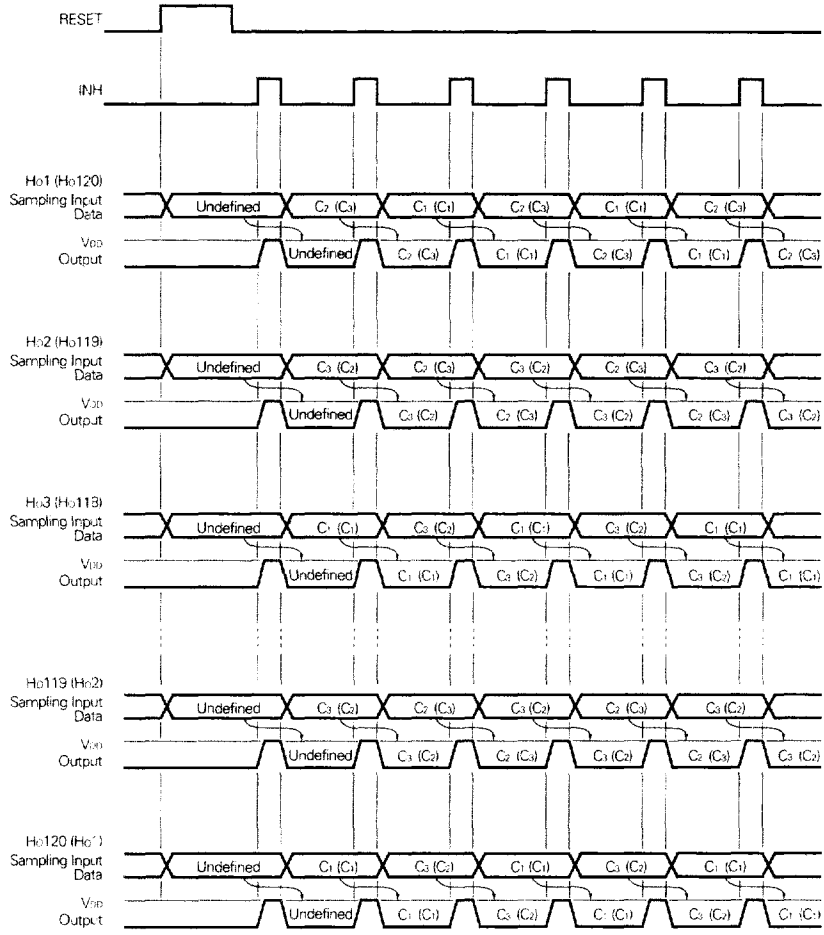
Operation Table

Line No. (No. of INH)	RESET	INH	H_1 (H_{120})	H_2 (H_{119})	H_3 (H_{118})	H_4 (H_{117})	H_{119} (H_2)	H_{120} (H_1)
0	H	L	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
1	L	↑	Sampling C_2 (C_3)	Sampling C_3 (C_2)	Sampling C_1 (C_1)	Sampling C_2 (C_3)	Sampling C_3 (C_2)	Sampling C_1 (C_1)
2	L	↑	Output C_2 (C_3)	Output C_3 (C_2)	Output C_1 (C_1)	Output C_2 (C_3)	Output C_3 (C_2)	Output C_1 (C_1)
3	L	↑	Output C_1 (C_1)	Output C_2 (C_3)	Output C_3 (C_2)	Output C_1 (C_1)	Output C_2 (C_3)	Output C_3 (C_2)
4	L	↑	Output C_2 (C_3)	Output C_3 (C_2)	Output C_1 (C_1)	Output C_2 (C_3)	Output C_3 (C_2)	Output C_1 (C_1)
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮

Values in brackets () are for a left shift.


B
R
G
C1
C2
C3
μPD16400
MP/TH = "H" R/L = "H"
MP/1.5 = "H"
H0.1
H0.2
H0.3
H0.4
H0.5
R B G R B G R B G R
B G R B G R B G R B G
H0.120
H0.119
H0.118
H0.117
H0.116
MP/TH = "H"
MP/1.5 = "H" R/L = "L"

Timing Chart for Delta Array

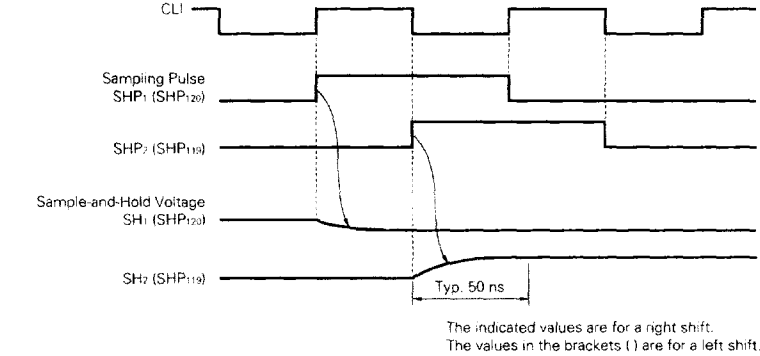


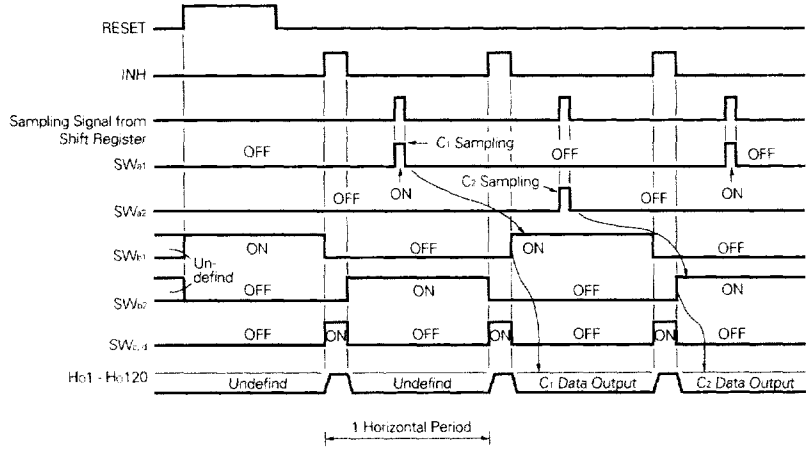
2. SAMPLE-AND-HOLD CIRCUIT

The sample-and-hold circuit samples one of C_1, C_2 and C_3 video signals selected by the multiplexer circuit (see the section on the multiplexer circuit) into C_1 and C_2 by SW_{a1} and SW_{a2}, respectively, that are controlled by the binary signal that is reset by the sampling signal from the shift register and the RESET signal, and changes at the INH signal rising edge. The video signals sampled into C_1 and C_2 are switched by SW_{b1} and SW_{b2} alternately at the INH signal rising edge and then sent to the next output circuit.

At the output circuit, while the INH signal is "H", the output is discharged by SWc and SWd, and when the INH signal becomes "L", SW_c and SW_d are turned OFF and the video signals from the sampling circuit are output by charging TFT with I_{VOH}. In other words, after a load is charged once by $I_{VOH1} + I_{VOH2}$, the load is discharged by I_{VOL}, and so the idling current of the output buffer during the output period can be taken to be I_{VOH1}, and power is saved.

2.1 SAMPLE-AND-HOLD TIMING





Remarks The sample-and-hold switching (SWa and SWb) signals for C_1 and C_2 are reset by the RESET signal and controlled by a flip-flop which changes between 0 and 1 at the INH rising edge.

ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C, Vss = 0 V)

PARAMETER	SYMBOL	RATING	UNIT	TEST CONDITIONS
Logic supply voltage	V_{DD1}	−0.5 to +7.0	V	
Driver supply voltage	V_{DD2}	−0.5 to +23	V	
Logic input voltage	V_I	−0.5 to V_{DD1} +0.5	V	
Video input voltage	V_{VI}	−0.5 to V_{DD2} +0.5	V	C_1, C_2, C_3
Input current	I_I	±20	mA	
Driver output current	I_O	±5	mA	
Operating temperature	T_{opt}	−20 to +70	°C	
Storage temperature	T_{stg}	−65 to +125 °C	°C	

RECOMMENDED OPERATING CONDITIONS (Vss = 0 V)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Logic supply voltage	V_{DD1}	4.5	5.0	5.5	V	
Driver supply voltage	V_{DD2}	12	15	18	V	

ELECTRICAL SPECIFICATIONS (T_a = −20 to +70 °C, V_{DD1} = 4.5 to 5.5 V, V_{DD2} = 15 V)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Maximum video signal output voltage	V_{VOH}	V_{DD2} −2.0	V_{DD2} −0.8		V	
Minimum video signal output voltage	V_{VOL}		1.45	2.5	V	
Logic output voltage high	V_{LOH}	0.8•V_{DD1}			V	STHL, STHR pins, I_{OH} = − 1 mA
Logic output voltage low	V_{LOL}			0.2•V_{DD1}	V	STHL, STHR pins, I_{OL} = 1 mA
Input voltage high	V_{IH}	0.7•V_{DD1}		V_{DD1}	V	
Input voltage low	V_{IL}	0		0.3•V_{DD1}	V	
Video signal output current high 1	I_{VOH1}	−13	−8	−2	μA	INH = L, SEL = L V_{of} = 6 V, V_O = 8 V
Video signal output current high 2	I_{VOH2}		−30		μA	INH = L, SEL = H V_{of} = 6 V, V_O = 8 V
Video signal output current high 3	I_{VOH3}			−0.3	mA	INH = H, V_{of} = 10 V
Video signal output current low	I_{VOL}	1.0			mA	INH = L, V_{of} = 11 V, V_O = 8 V
Minimum video signal input voltage	V_{VIL}			1.5	V	T_a = 25 °C
Reference voltage 1	V_{REF1}		3.09		V	V_{VI} = 2.5 V, T_a = 25 °C
Reference voltage 2	V_{REF2}		7.80		V	V_{VI} = 7.5 V, T_a = 25 °C
Reference voltage 3	V_{REF3}		12.6		V	V_{VI} = 12.5 V, T_a = 25 °C
Output voltage deviation 1	ΔV_{VO1}			±50	mV	V_{VI} = 2.5 V, T_a = 25 °C
Output voltage deviation 2	ΔV_{VO2}			±50	mV	V_{VI} = 7.5 V, T_a = 25 °C
Output voltage deviation 3	ΔV_{VO3}			±50	mV	V_{VI} = 12.5 V, T_a = 25 °C
Logic input leakage current	I_{LL}			±1	μA	
Video input leakage current	I_{VL}			±10	μA	
Logic dynamic consumption current	I_{DD11}		0.7	2.5	mA	f_{CLK} = 4 MHz V_{VI} = 7.5 V, no load
Driver dynamic consumption current	I_{DD21}		4.0	5.0	mA	f_{CLK} = 4 MHz V_{VI} = 7.5 V, no load

V_{of}: Output applied voltage, V_O: Output voltage for no load

The reference voltage is the average value of the output voltage of all of the pins in the chip, and the output voltage deviation is the deviation in output voltage between pins in the chip. The output voltage deviation is not the value guaranteed for between chips or lots.

SWITCHING CHARACTERISTICS (Ta = −20 to +70 °C, V_{DD1} = 4.5 to 5.5 V, V_{DD2} = 15 V, C_L = 20 pF, tr = tf = 5 ns)

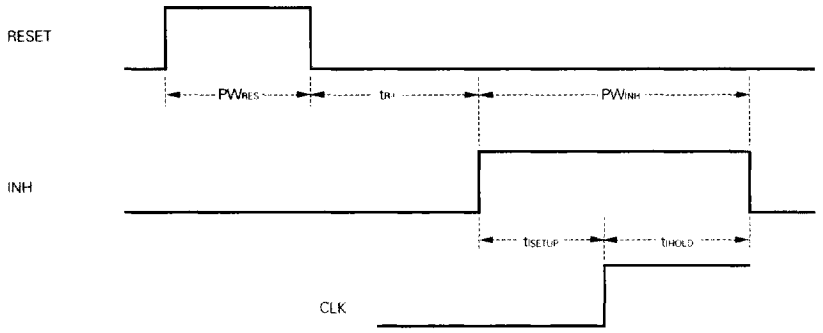
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Start pulse transmission delay time	t_{PHL}	15		160	ns	
	t_{PLH}	15		160	ns	
Maximum clock frequency	f_{max}	5			MHz	
Logic input capacitance	C_{I1}			15	pF	Except STHL and STHR, at 25 °C
STHL, STHR input capacitance	C_{I2}			20	pF	STHL, STHR, 25 °C
Video input capacitance	C_{I3}			30	pF	C_1 to C_3, V_{VI} = 7.5V, 25 °C

TIMING REQUIREMENTS (Ta = −20 to +70 °C, V_{DD1} = 4.5 to 5.5 V, V_{DD2} = 15 V, tr = tf = 5 ns)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Clock pulse width	PW_{CL1}	100			ns	Duty = 50 %
ST pulse width	PW_{ST}	100			ns	
Reset pulse width	PW_{RES}	100			ns	
Reset to INH time	t_{R-I}	100			ns	
Start pulse setup time	t_{SETUP}	40			ns	
Start pulse hold time	t_{HOLD}	15			ns	
INH setup time	t_{ISETUP}	300			ns	
INH hold time	t_{IHOLD}	300			ns	

The rise and fall time of the digital input signals should all be tr = tf = 5 ns or less (10 % to 90 % rating).

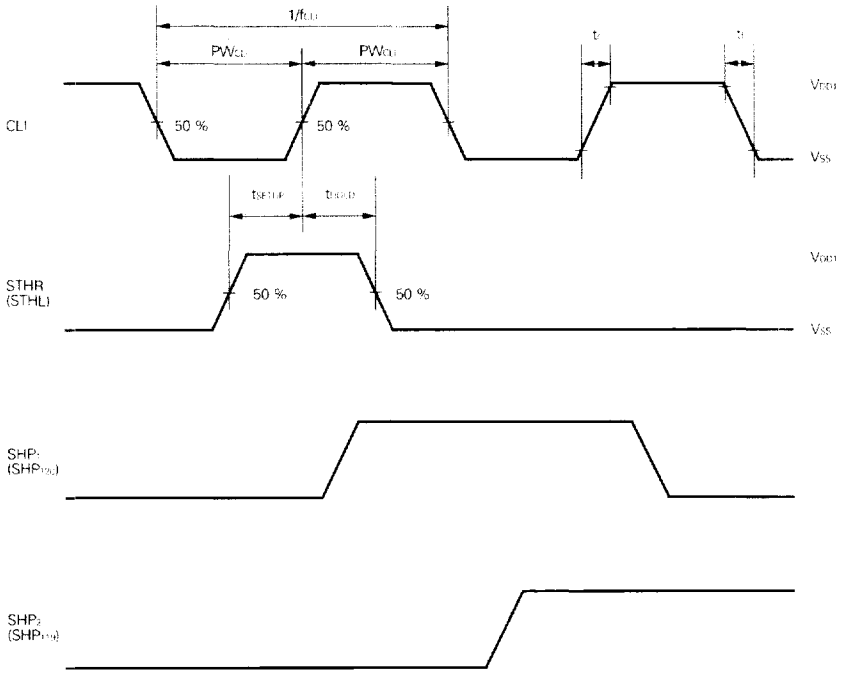
RESET TO INH TIME STIPULATION



The minimum INH pulse width should be 3 clocks or more.

SWITCHING CHARACTERISTIC WAVEFORMS

Start Pulse Input Timing



Start Pulse Output Timing