μPD9604AD/05AD
CMOS PCM
CODEC-Filter Combination

Description

The μPD9604AD and μPD9605AD are PCM codec-filter combo chips, μ-law and A-law compatible, respectively. These monolithic CMOS LSIs include digital gain setting, transmit/receive filters, and phase-locked loops (PLL) that derive internal signal processing clocks from the transmit and receive frame sync clock inputs.

Features

- Digital gain setting for transmit and receive sections
- Transmit input operational amplifier
- Transmit active lowpass filter and switched-capacitor bandpass filter
- Analog loopback test
- Autozero circuit
- Receive unbalanced 600-Ω output power amplifier
- Receive switched-capacitor lowpass filter
- Digital serial I/O interface circuit
- μ-law (9604AD) and A-law (9605AD) companding
- Precision reference voltage circuit
- Synchronous or asynchronous operation
- Data rate, 64 kb/s to 2.048 Mb/s
- Low power dissipation
  — 50 mW normal mode
  — 5 mW power-down or standby mode
- 16-pin ceramic DIP

Ordering Information

Part Number	Companding	Package
μPD9604AD	μ-law	16-pin ceramic DIP (300 mil)
μPD9605AD	A-law	

Block Diagram