Standard Products

UT7R995 & UT7R995C RadClock™

RadHard 2.5V/3.3V 200MHz High-Speed Multi-phase PLL Clock Buffer

Advanced Data Sheet
November 29, 2005

FEATURES:

- ❑ +3.3V Core Power Supply
- ❑ +2.5V or +3.3V Clock Output Power Supply
  - Independent Clock Output Bank Power Supplies
- ❑ Output frequency range: 6 MHz to 200 MHz
- ❑ Output-output skew < 100 ps
- ❑ Cycle-cycle jitter < 100 ps
- ❑ ± 2% maximum output duty cycle
- ❑ Eight LVTTL outputs with selectable drive strength
- ❑ Selectable positive- or negative-edge synchronization
- ❑ Selectable phase-locked loop (PLL) frequency range and lock indicator
- ❑ Phase adjustments in 625 to 1300 ps steps up to ± 7.8 ns
- ❑ (1-6,8,10,12) x multiply and (1/2,1/4) x divide ratios
- ❑ Compatible with Spread-Spectrum reference clocks
- ❑ Power-down mode
- ❑ Selectable reference input divider
- ❑ Radiation performance
  - Total-dose tolerance: 300 krad (Si) and 1 Mrad (Si)
  - SEL Immune to a LET of 109 MeV-cm^2/mg
  - SEU Immune to a LET of 109 MeV-cm^2/mg
  - SET: Contact factory for details
- ❑ Military temperature range: -55°C to +125°C
- ❑ Packaging options:
  - 48-Lead Ceramic Flatpack
- ❑ Standard Microcircuit Drawing: 5962-05214
  - QML-Q and QML-V compliant part

INTRODUCTION:

The UT7R995/UT7R995C is a low-voltage, low-power, eight-output, 6-to-200 MHz clock driver. It features output phase programmability which is necessary to optimize the timing of high-performance microprocessor and communication systems.

The user programs both the frequency and the phase of the output banks through nF[1:0] and DS[1:0] pins. The adjustable phase feature allows the user to skew the outputs to lead or lag the reference clock. Connect any one of the outputs to the feedback input to achieve different reference frequency multiplication and division ratios.

The devices also feature split output bank power supplies that enable banks 1 & 2, bank 3, and bank 4 to operate at a different power supply levels. The ternary PE/HD pin controls the synchronization of output signals to either the rising or the falling edge of the reference clock and selects the drive strength of the output buffers. The UT7R995 and UT7R995C both interface to a digital clock while the UT7R995C will also interface to a quartz crystal.

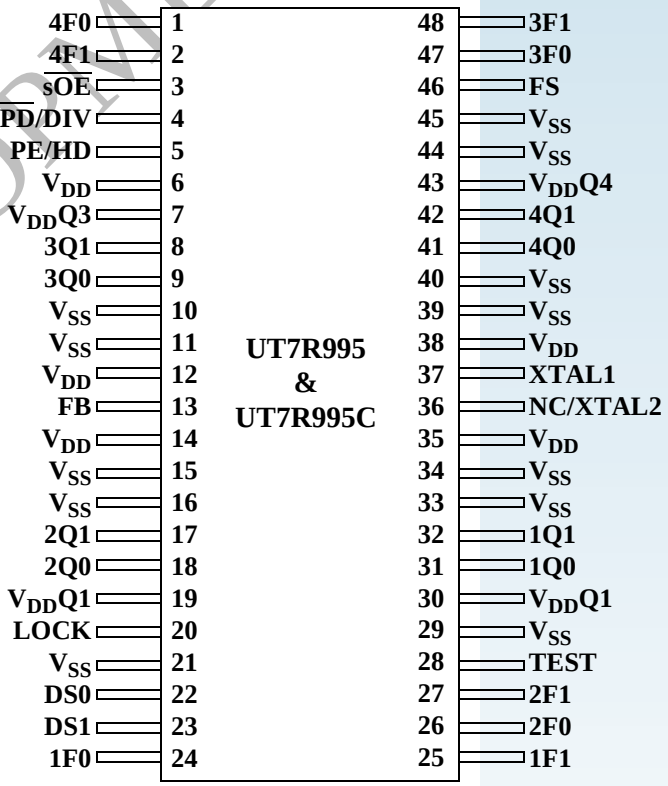


Figure 1. 48-Lead Ceramic Flatpack Pin Description

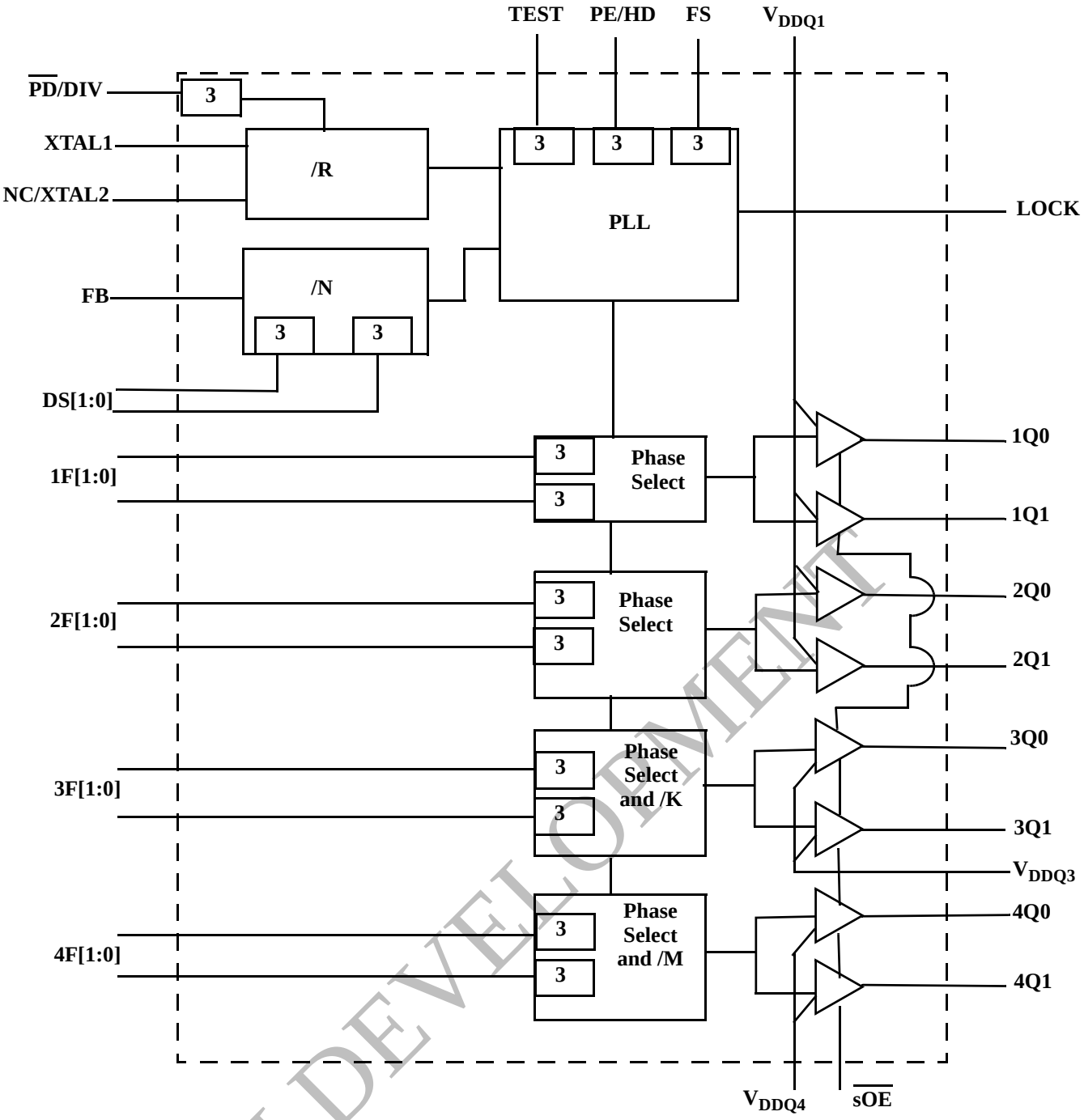


Figure 2. UT7R995 & UT7R995C Block Diagram

1.0 DEVICE CONFIGURATION:

The outputs of the UT7R995/C can be configured to run at frequencies ranging from 6 MHz to 200 MHz. Each output bank has the ability to run at separate frequencies and with various phase skews. Furthermore, numerous clock division and multiplication options exist.

The following discussion and list of tables will summarize the available configuration options for the UT7R995/C. Tables 1 through 11, are relevant to the following configuration discussions.

1.1 Divider Configuration Settings:

The feedback input divider is controlled by the 3-level DS[1:0] pins as indicated in Table 1 and the reference input divider is controlled by the 3-level $\overline{PD}$/DIV pin as indicated in Table 2. Although the Reference divider will continue to operate when the UT7R995/C is in the standard TEST mode of operation, the Feedback Divider will not be available.

Table 1: Feedback Divider Settings (*N-factor*)

DS[1:0]	Feedback Input Divider - *(N)*	Permitted Output Divider (K or M) Connected to FB
LL	2	1 or 2
LM	3	1
LH	4	1, 2, or 4
ML	5	1 or 2
MM	1	1, 2, or 4
MH	6	1 or 2
HL	8	1 or 2
HM	10	1
HH	12	1

Table 2: Reference Divider Settings (*R-factor*)

$\overline{PD}$/DIV	Operating Mode	Reference Input Divider - *(R)*
LOW [1]	Powered Down	Not Applicable
MID	Normal Operation	**2**
HIGH	Normal Operation	**1**

Notes:
1. When $\overline{PD}$/DIV = LOW, the device enters power-down mode.

In addition to the reference and feedback dividers, the UT7R995/C includes output dividers on Bank 3 and Bank 4, which are controlled by 3F[1:0] and 4F[1:0] as indicated in Tables 3 and 4, respectively.

Table 3: Output Divider Settings - Bank 3 (*K-factor*)

3F(1:0)	Bank 3 Output Divider - *(K)*
LL	2
HH	4
Other [1]	1

Notes:
1. These states are used to program the phase of the respective banks. Please see Equation 1 along with Tables 8 and 10.

Table 4: Output Divider Settings - Bank 4 (*M-factor*)

4F[1:0]	Bank 4 Output Divider *(M)*
LL	2
Other [1]	1

Notes:
1. These states are used to program the phase of the respective banks. Please see Equation 1 along with Tables 8 and 10.

Each of the four divider options and their respective settings are summarized in Table 5. By applying the divider options in Table 5 to the calculations shown in Table 6, the user determines the proper clock frequency for every output bank.

Table 5: Frequency Divider Summary

Division Factors	Available Divider Settings
N	1, 2, 3, 4, 5, 6, 8, 10, 12
R	1, 2
K	1, 2, 4
M	1, 2

Table 6: Calculating Output Frequency Settings

Configuration	Output Frequency		
Clock Output Connected to FB	**1Q[1:0] [1] and 2Q[1:0] [1]**	**3Q[1:0]**	**4Q[1:0]**
1Qn or 2Qn	(N/R) * f_{XTAL}	(N/R) * (1/K) * f_{XTAL}	(N/R) * (1/M) * f_{XTAL}
3Qn	(N/R) * K * f_{XTAL}	(N/R) * f_{XTAL}	(N/R) * (K/M) * f_{XTAL}
4Qn	(N/R) * M * f_{XTAL}	(N/R) * (M/K) * f_{XTAL}	(N/R) * f_{XTAL}

Notes:

1. These outputs are undivided copies of the VCO clock. Therefore, the formulas in this column can be used to calculate the nominal VCO operating frequency (f_{NOM}) at a given reference frequency (f_{XTAL}) and the divider and feedback configuration. The user must select a configuration and a reference frequency that will generate a VCO frequency that is within the range specified by FS pin. Please see Table 7.

1.2 Frequency Range and Skew Selection:

The PLL in the UT7R995/C operates within three nominal frequency ranges. Depending upon the desired PLL operating frequency, the user must define the state of the ternary FS control pin. Table 7 defines the required FS selections based upon the nominal PLL operating frequency ranges. Because the clock outputs on Bank 1 and Bank 2 do not include a divider option, they will always reflect the current frequency of the PLL. Reference the first column of equations in Table 6 to calculate the value of f_{NOM} for any given feedback clock.

Table 7: Frequency Range Select

FS	Nominal PLL Frequency Range (f_{NOM})
L	24 to 50 MHz
M	48 to 100MHz
H	96 to 200 MHz

Selectable output skew is in discrete increments of time unit (t_U). The value of t_U is determined by the FS setting and the PLL's operating frequency (f_{NOM}). Use the following equation to calculate the time unit (t_U):

Equation 1. $$t_u = \frac{1}{(f_{NOM} * MF)}$$

The f_{NOM} term, which is calculated with the help of Table 6, must be compatible with the nominal frequency range selected by the FS signal as defined in Table 7. The multiplication factor (MF), also determined by FS, is shown in Table 8. The UT7R995/C output skew steps have a typical accuracy, based upon the calculated time unit, of +/- 100ps per skew step.

After calculating the time unit (t_U) based on the nominal PLL frequency (f_{NOM}) and multiplication factor (MF), the circuit designer plans routing requirements of each clock output and its respective destination receiver. With an understanding of signal propagation delays through a conductive medium (see Table 9), the designer specifies trace lengths which ensure a signal propagation delay that is equal to one of the t_U multiples show in Table 10. For each output bank, the t_U skew factors are selected with the tri-level, bank-specific, nF[1:0] pins.

Table 8: MF Calculation

FS	MF	f_{NOM} examples that result in a t_U of 1.0ns
L	32	31.25 MHz
M	16	62.5 MHz
H	8	125 MHz

Table 9: Signal Propagation Delays in Various Media

Medium	Propagation Delay (ps/inch)	Dielectric Constant
Air (Radio Waves)	85	1.0
Coax. Cable (75% Velocity)	113	1.8
Coax. Cable (66% Velocity)	129	2.3
FR4 PCB, Outer Trace	140 - 180	2.8 - 4.5
FR4 PCB, Inner Trace	180	4.5
Alumina PCB, Inner Trace	240 - 270	8 - 10

Table 10: Output Skew Settings

nF[1:0]	Skew 1Q[1:0], 2Q[1:0]	Skew 3Q[1:0]	Skew 4Q[1:0]
LL [1, 2]	$-4t_U$	Divide by 2	Divide by 2
LM	$-3t_U$	$-6t_U$	$-6t_U$
LH	$-2t_U$	$-4t_U$	$-4t_U$
ML	$-1t_U$	$-2t_U$	$-2t_U$
MM	Zero Skew	Zero Skew	Zero Skew
MH	$+1t_U$	$+2t_U$	$+2t_U$
HL	$+2t_U$	$+4t_U$	$+4t_U$
HM	$+3t_U$	$+6t_U$	$+6t_U$
HH [2]	$+4t_U$	Divide by 4	Inverted [3]

Notes:
1. nF[1:0] = LL disables bank specific outputs if TEST=MID and $\overline{sOE}$ = HIGH.
2. When TEST=MID or HIGH, the Divide-by-2, Divide-by-4, and Inversion-options function as defined in Table 9.
3. When 4Q[1:0] are set to run inverted (4F[1:0] = HH), $\overline{sOE}$ disables these outputs HIGH when PE/HD = HIGH or MID, $\overline{sOE}$ disables them LOW when PE/HD = LOW.

A graphical summary of Table 10 is shown in Figure 3. The drawing assumes that the FB input is driven by a clock output programmed with zero skew. Depending upon the state of the nF[1:0] pins the respective clocks will be skewed, divided, or inverted relative to the fedback output as shown in Figure 3.

1.3 Output Drive, Synchronization, and Power Supplies:

The UT7R995/C employs flexible output buffers providing the user with selectable drive strengths, independent power supplies, and synchronization to either edge of the reference input. Using the 3-level PE/HD pin, the user selects the reference edge synchronization and the output drive strength for all clock outputs. The options for edge synchronization and output drive strength selected by the PE/HD pin are listed in Table 11.

Table 11: PE/HD Settings

PE/HD	Synchronization	Output Drive Strength [1]
L	Negative	Low Drive
M	Positive	High Drive
H	Positive	Low Drive

Notes:
1. Please refer to "DC Parameters" section for I_{OH}/I_{OL} specifications.

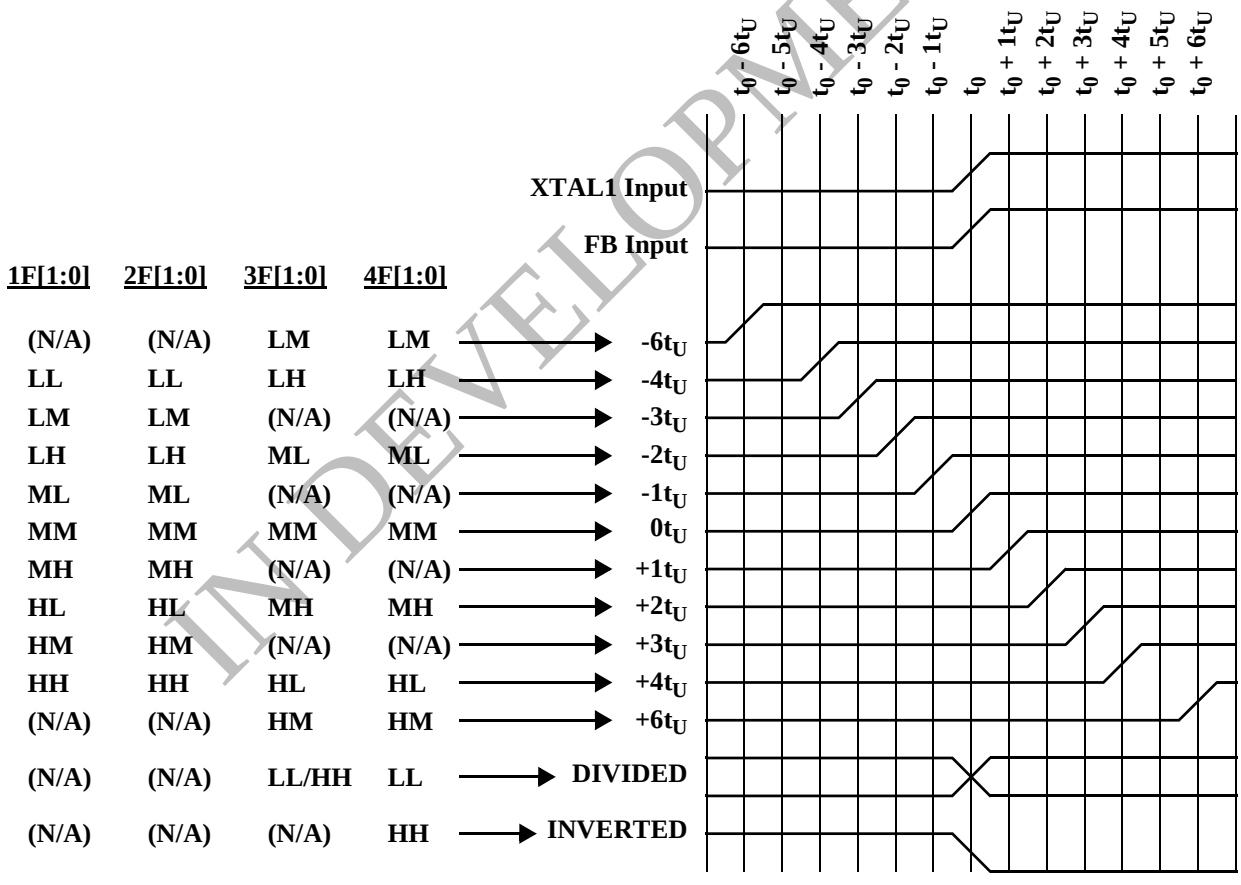


Figure 3. Typical Outputs with FB Connected to a Zero-Skewed Output

When the outputs are configured for low drive operation, they will provide a minimum 12mA of drive current regardless of the selected output power supply. If the outputs are configured for high drive operation, they will provide a minimum 24mA of drive current under a 3.3V power supply and 20mA when powered from a 2.5V supply.

The UT7R995/C features split power supply buses for Banks 1 and 2, Bank 3, and Bank 4. These independent power supplies enable the user to obtain both 3.3V and 2.5V output signals from one UT7R995/C device. The core power supply (V_{DD}) must run from a 3.3V power supply. Table 12 summarizes the various power supply options available with the UT7R995/C.

Table 12: Power Supply Constraints [1]

V_{DD}	$V_{DD}Q1$	$V_{DD}Q3$	$V_{DD}Q4$
3.3V	3.3V or 2.5V	3.3V or 2.5V	3.3V or 2.5V

Notes:
1. $V_{DD}Q1/3/4$ must not be set at a level higher than that of V_{DD}.

1.4 Reference Clock Interfaces

When an external, LVCMOS/LVTTL, digital clock is used to drive the UT7R995 and UT7R995C, the reference clock signal should drive the XTAL1 input of the RadClock, while the XTAL2 output should be left unconnected (see Figure 4). **Note**, for the UT7R995 only, the XTAL2 pin is defined as a no-connect.

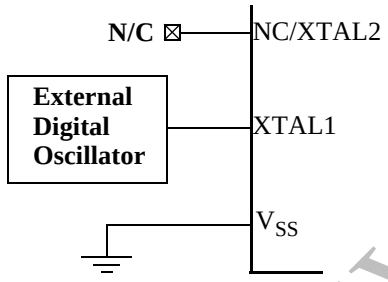
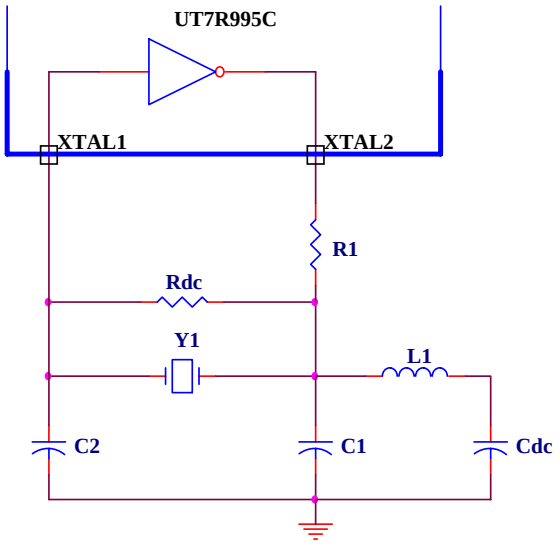


Figure 4. External Digital Clock Oscillator Interface

In addition to a digital clock reference, the UT7R995C can interface to a quartz crystal. When interfacing to a quartz crystal, XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier within the RadClock. This inverting amplifier provides the initial 180° phase shift of the reference clock whose frequency, and subsequent 180° phase shift, is set by the quartz crystal and its surrounding RLC network. Figure 5 shows a typical pierce-oscillator with tank-circuit that will support reliable startup of fundamental and odd-harmonic, AT-cut, quartz crystals.



Fundamental Frequency Pierce Crystal Oscillator

Rdc = ~10MΩ; L1 = Not Used; Cdc = Not Used

C2 is used to tune the circuit for stable oscillation. Typical values for C2 range from 30pF to 50pF.

R1 and C1 are selected to create a time constant that facilitates the fundamental frequency (f_F) of the quartz crystal as defined in equation 2.

Equation 2. $$f_F = \frac{1}{(2\pi * R1 * C1)}$$

As an example, selecting a value of 100Ω for R1 and 80pF for C1 would facilitate the reliable operation of a 20MHz, AT-cut, quartz crystal.

Higher Frequency Pierce Crystal Oscillator

Rdc = ~10MΩ; Cdc = ~1.5nF; C2 = Tuning capacitor similar to prior example

R1 and C1 are selected to create a time constant that facilitates the overtone frequency (f_{OT}) of the quartz crystal as shown in equation 3.

Equation 3. $$f_{OT} = \frac{1}{(2\pi * R1 * C1)}$$

Additionally, L1 is selected such that its relationship with C2 facilitates a frequency falling between the fundamental frequency (f_F) and the specified overtone frequency (f_{OT}) of the quartz crystal as shown in equation 4.

Equation 4. $$f_M = \frac{1}{\left(2\pi * \sqrt{L1 * C1}\right)}$$

As an example, selecting the following component values will result in a 50MHz Pierce Crystal Oscillator based upon an 3rd overtone, AT-cut, quartz crystal having a fundamental frequency of 16.6666MHz.

Rdc = 10MW; Cdc = 1.5nF; C2 = 30pF;
R1 = 50W; C1 = 55pF; L1 = 300nH
f_F = 16.6666MHz; f_{OT} = 50MHz

Figure 5. Pierce Crystal Oscillator with Tank Circuit

2.0 RADIATION HARDNESS

Table 13: Radiation Hardness Design Specifications

Parameter	Limit	Units
Total Ionizing Dose (TID)	>1E6	rads(Si)
Single Event Latchup (SEL) [1, 2]	>109	MeV-cm^2/mg
SEU Saturated Cross-Section (σ_{sat})	1.0E-8	cm^2/device
Onset Single Event Upset (SEU) LET Threshold [3]	109	MeV-cm^2/mg
Neutron Fluence	1.0E14	n/cm^2
Dose Rate Upset	TBD	rads(Si)/sec
Dose Rate Survivability	TBD	rads(Si)/sec

Notes:

1. The UT7R995/C are latchup immune to particle LETs >109 MeV-cm^2/mg.
2. Worst case temperature and voltage of T_C = +125^{o}C, V_{DD} = 3.6V, V_{DD}Q1/Q3/Q4 = 3.6V for SEL.
3. Worst case temperature and voltage of T_C = +25^{o}C, V_{DD} = 3.0V, V_{DD}Q1/Q3/Q4 = 3.0V for SEU.
4. Adams 90% worst case particle environment, Geosynchronous orbit, 100mils of Aluminum shielding.

Table 14: Weibull and Device Parameters (256 Registers[1])

Parameter	Limit	Units
Shape Parameter	TBD	--
Width Parameter	TBD	--
Structural Cross-Section (σ)	1.0E-8	cm^2/device
Onset SEU LET[2]	109	MeV-cm^2/mg
Depletion Depth	TBD	µm
Funnel Depth	TBD	µm

Notes:

1. This SEU data is based on a test chip containing an array of 256 registers that are identical to the 30 registers used within the UT7R995/C.
2. All SEU data specified in this datasheet is based on the storage elements used in the UT7R995/C. Please contact the factory for details regarding SET performance of the UT7R995/C.

3.0 PIN DESCRIPTION

Flatpack Pin No.	Name	I/O	Type	Description
37	XTAL1	I	LVTTL	**Primary reference clock input.** When interfacing a single-ended reference clock to the UT7R995 or UT7R995C, this input must be driven by an LVTTL/LVCMOS clock source. If a quartz crystal is used as the reference clock source (UT7R995C only), the second pin on the crystal must be connected to XTAL2. If a singled ended reference clock is supplied to this pin, then XTAL2 should be left unconnected.
36	N/C	--	--	**No Connect.** UT7R995 Only.
	XTAL2	O	N/A	**Feedback output from the on-board crystal oscillator.** When a crystal is used to supply the reference clock for the UT7R995C, this pin must be connected to the second terminal of the quartz crystal. If a single-ended reference clock is supplied to XTAL1, then this output should be left unconnected.
13	FB	I	LVTTL	**Feedback input for the PLL.** When FB is not driven by an active clock output the PLL will run to its maximum frequency, unless the device is placed in power-down.
28	TEST [1]	I	3-Level	**Built-in test control signal.** When Test is set to the **MID** or **HIGH** level, it disables the PLL and the XTAL1 reference frequency is driven to all outputs (except for the conditions described in note 2). Set Test **LOW** for normal operation.

Flatpack Pin No.	Name	I/O	Type	Description
3	$\overline{\text{sOE}}$	I	LVTTL	**Synchronous Output Enable.** The $\overline{\text{sOE}}$ input is used to synchronously enable/disable the output clocks. Each clock output that is controlled by the $\overline{\text{sOE}}$ pin is synchronously enabled/disabled by the individual output clock. When **HIGH**, $\overline{\text{sOE}}$ disables all clocks except 2Q0 and 2Q1. When disabled, 1Q0, 1Q1, 3Q0, and 3Q1 will always enter a **LOW** state when PE/HD is **MID** or **HIGH**, and they will disable into a **HIGH** state when PE/HD is **LOW**. The disabled state of 4Q0 and 4Q1 is dependent upon the state of PE/HD and 4F[1:0]. The following table illustrates the disabled state of bank 4 outputs as they are controlled by the state of PE/HD and 4F[1:0]. **PE/HD** — **4F[1:0]*** — **4Q0** — **4Q1** **LOW** — **HH** — **LOW** — **LOW** **MID** — **HH** — **HIGH** — **HIGH** **HIGH** — **HH** — **HIGH** — **HIGH** *All other combinations of 4F[1:0] will result in 4Q0 and 4Q1 disabling into a **LOW** state when PE/HD is **MID** or **HIGH**, and they will disable into a **HIGH** state when PE/HD is **LOW**. When TEST is held at the **MID** level and $\overline{\text{sOE}}$ is **HIGH**, the nF[1:0] pins act as individual output enable/disable controls for each output bank, excluding bank 2. Setting both nF[1:0] signals **LOW** disables the corresponding output bank. Set $\overline{\text{sOE}}$ **LOW** to place the UT7R995/C RadClock™ outputs into their normal operating modes.
1, 2, 24, 25, 26, 27, 47, 48	nF[1:0]	I	3-Level	**Output divider and phase skew selection for each output bank.** Please see Tables 3, 4, 5, 6, and 9 for a complete explanation of the nF[1:0] control functions and their effects on output frequency and skew.
46	FS	I	3-Level	**VCO operating frequency range selection.** Please see Tables 7 and 8.
8, 9, 17, 18, 31, 32, 41, 42	nQ[1:0]	O	LVTTL	**Four clock banks of two outputs each.** Please see Table 6 for frequency settings and Table 9 for skew settings.
22, 23	DS[1:0]	I	3-Level	**Feedback input divider selection.** Please see Table 1 for a summary of the feedback input divider settings.
5	PE/HD	I	3-Level	**Positive/negative edge control and high/low output drive strength selection.** The PE portion of this pin controls which edge of the reference input synchronizes the clock outputs. The HD portion of this pin controls the drive strength of the output clock buffers. The following table summarizes the effects of the PE/HD pin during normal operation. **PE/HD** — **Synchronization** — **Output Drive Strength** **LOW** — **Negative Edge** — **Low Drive** **MID** — **Positive Edge** — **High Drive** **HIGH** — **Positive Edge** — **Low Drive** Low drive strength outputs provide 12mA of drive strength while the high drive condition results in 24mA of current drive. Output banks operating from a 2.5V power supply guarantee a high drive of 20mA.

Flatpack Pin No.	Name	I/O	Type	Description
4	$\overline{PD}$/DIV	I	3-Level	**Power down and reference divider control.** This dual function pin controls the power down operation and selects the input reference divider. The following table summarizes the operating states controlled by the $\overline{PD}$/DIV pin. **$\overline{PD}$/DIV** — **Operating Mode** — **Input Reference Divider** **LOW** — **Powered Down** — **N/A** **MID** — **Normal Operation** — **÷ 2** **HIGH** — **Normal Operation** — **÷ 1**
20	LOCK	O	LVTTL	**PLL lock indication signal.** A **HIGH** state indicates that the PLL is in a locked condition. A **LOW** state indicates that the PLL is not locked and the outputs may not be synchronized to the input. As the following table indicates, the level of phase alignment between XTAL1 and FB that will cause the LOCK pin to change states is dependent upon the frequency range selected by the FS input. **FS** — **LOCK Resolution** **L** — **1.6ns typical** **M** — **1.6ns typical** **H** — **800ps typical** ** Note: When the RadClock is in a power-down mode or the reference clock is removed, the LOCK pin will transition to its HIGH state.
43	$V_{DD}Q4$ [2]	PWR	Power	**Power supply for Bank 4 output buffers.** Please see Table 12 for supply level constraints.
7	$V_{DD}Q3$ [2]	PWR	Power	**Power supply for Bank 3output buffers.** Please see Table 12 for supply level constraints.
19, 30	$V_{DD}Q1$ [2]	PWR	Power	**Power supply for Bank 1 and Bank 2 output buffers.** Please see Table 12 for supply level constraints.
6, 12, 14, 35, 38	V_{DD} [2]	PWR	Power	**Power supply for internal circuitry.** Please see Table 12 for supply level constraints.
10, 11, 15, 16, 21, 29, 33, 34, 39, 40, 44, 45	V_{SS}	PWR	Power	**Ground**

Notes:

1. When TEST = MID and s$\overline{OE}$ = HIGH, the PLL remains active with nF[1:0] = LL functioning as an output disable control for individual output banks. Skew selections remain in effect unless nF[1:0] = LL.
2. A bypass capacitor (0.1µF) should be placed as close as possible to each positive power pin (<0.2"). An additional 1µF capacitor should be located within 0.2" of the output bank power supplies ($V_{DD}Q1$, $V_{DD}Q3$, and $V_{DD}Q4$). If these bypass capacitors are not close to the pins, their high frequency filtering characteristics will be cancelled by the parasitic inductance of the traces. Additionally, it is recommend that wide traces (0.025" or wider) be used when connecting the decoupling capacitors to their respective power pins on the RadClock.

4.0 ABSOLUTE MAXIMUM RATINGS:[1]

(Referenced to V_{SS})

Symbol	Description	Limits	Units
V_{DD}	Core Power Supply Voltage	-0.3 to 4.0	V
$V_{DD}Q1$, $V_{DD}Q3$, and $V_{DD}Q4$	Output Bank Power Supply Voltage	-0.3 to 4.0	V
V_{IN}	Voltage Any Input Pin	-0.3 to V_{DD} + 0.3	V
V_{OUT}	Voltage Any Clock Bank Output	-0.3 to $V_{DD}Qn$ + 0.3	V
V_O	Voltage on XTAL2 and LOCK Outputs	-0.3 to V_{DD} + 0.3	V
I_I	DC Input Current	$\pm$10	mA
P_D	Maximum Power Dissipation	1	W
T_{STG}	Storage Temperature	-65 to +150	°C
T_J	Maximum Junction Temperature [2]	+150	°C
Θ_{JC}	Thermal Resistance, Junction to Case	15	°C/W
ESD_{HBM}	ESD Protection (Human Body Model) - Class II	>3000	V

Notes:
1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and performance.
2. Maximum junction temperature may be increased to +175°C during burn-in and steady-static life.

5.0 RECOMMENDED OPERATING CONDITIONS:

Symbol	Description	Limits	Units
V_{DD}	Core Operating Voltage	3.0 to 3.6	V
$V_{DD}Q1$, $V_{DD}Q3$, and $V_{DD}Q4$	Output Bank Operating Voltage	2.25 to 3.6	V
V_{IN}	Voltage Any Configuration and Control Input	0 to V_{DD}	V
V_{OUT}	Voltage Any Bank Output	0 to $V_{DD}Qn$	V
T_C	Case Operating Temperature	-55 to +125	°C

6.0 DC INPUT ELECTRICAL CHARACTERISTICS (Pre- and Post-Radiation)*

(V_{DD} = +3.3V ± 0.3V; T_C = -55°C to +125°C)

Symbol	Description	Conditions	Min.	Max.	Units
V_{IH} [1]	High-level input voltage (XTAL1, FB and $\overline{sOE}$ inputs)		2.0	--	V
V_{IL} [1]	Low-level input voltage (XTAL1, FB and $\overline{sOE}$ inputs)		--	0.8	V
V_{IHH} [1,2]	High-level input voltage		V_{DD} - 0.6	--	V
V_{IMM} [1,2]	Mid-level input voltage		V_{DD}÷2 - 0.3	V_{DD}÷2 + 0.3	V
V_{ILL} [1,2]	Low-level input voltage		--	0.6	V
I_{IL}	Input leakage current (XTAL1, FB and $\overline{sOE}$ inputs)	V_{IN} = V_{DD} or $V_{SS;}$ V_{DD} = Max	-5	5	µA
I_{3L} [2]	3-Level input DC current	HIGH, V_{IN} = V_{DD}	--	200	µA
		MID, V_{IN} = V_{DD}/2	-50	50	µA
		LOW, V_{IN} = V_{SS}	-200	--	µA
I_{DDQ}	Quiescent supply current	V_{DD} = +3.0V; V_{DD}Qn = +3.0V; TEST & $\overline{sOE}$ = HIGH; XTAL1, FB, FS, & PE/HD = LOW; All other inputs are floated; Outputs are not loaded	--	4	mA
I_{DDPD}	Power-down current	V_{DD} = +3.0V; V_{DD}Qn = +3.0V; TEST & $\overline{sOE}$ = HIGH; XTAL1, $\overline{PD}$/DIV, FB, FS, & PE/HD = LOW; All other inputs are floated; Outputs are not loaded	--	100	µA
C_{IN-2L} [3]	Input pin capacitance 2-level inputs	*f* = 1MHz @ 0V; V_{DD} = Max	8.5		pF
C_{IN-3L} [3]	Input pin capacitance 3-level inputs	*f* = 1MHz @ 0V; V_{DD} = Max	15		pF

Notes:

* Post-radiation performance guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to a TID level of 1.0E6 rad(Si).

1. Functional tests are conducted in accordance with MIL-STD-883 with the following input test conditions: V_{IH} = $V_{IH(min)}$ +20%, -0%; V_{IL} = $V_{IL(max)}$ +0%, -50%, as specified herein for LVTTL and LVCMOS inputs. For 3-level inputs, V_{IH} = $V_{IHH(min)}$ +50%, -0%; V_{IL} = $V_{ILL(max)}$ +0%, -50%; V_{IM} = $V_{IMM(nom)}$ +0.1V, -0.1V. Devices may be tested using any input voltage within the above specified range, but are guaranteed to $V_{IH(min)}$, $V_{IL(max)}$, $V_{IHH(min)}$, $V_{ILL(max)}$, and $V_{IMM(nom)}$.
2. These inputs are normally wired to V_{DD}, V_{SS}, or left unconnected. Internal termination resistors bias unconnected inputs to V_{DD}/2 ± 0.3V. The 3-level inputs include: TEST, $\overline{PD}$/DIV, PE/HD, FS, nF[1:0], DS[1:0].
3. Capacitance is measured for initial qualification and when design changes may affect the input/output capacitance. Capacitance is measured between the designated terminal and V_{SS} at frequency of 1MHz and a signal amplitude of 50mV rms maximum.

7.0 DC OUTPUT ELECTRICAL CHARACTERISTICS (Pre- and Post-Radiation)*

(V_{DD}Qn = +2.5V ± 10%; V_{DD} = +3.3V ± 0.3V; T_C = -55°C to +125°C) (Note 1)

Symbol	Description	Conditions	Min.	Max.	Units
V_{OL}	Output low voltage	I_{OL} = 12mA (PE/HD = LOW or HIGH); (Pins: nQ[1:0])	--	0.4	V
		I_{OL} = 20mA (PE/HD = MID); (Pins: nQ[1:0])	--	0.4	V
		I_{OL} = 2mA (Pins: LOCK)	--	0.4	V
V_{OH}	High-level output voltage	I_{OH} = 8mA (PE/HD = LOW or HIGH); (Pins: nQ[1:0]); V_{DD}Qn = +2.25V)	2.0	--	
		I_{OH} = -12mA (PE/HD = LOW or HIGH); (Pins: nQ[1:0])	2.0	--	V
		I_{OH} = -16mA (PE/HD = MID); (Pins: nQ[1:0]; V_{DD}Qn = +2.25V)	2.0	--	V
		I_{OH} = -20mA (PE/HD = MID); (Pins: nQ[1:0]; V_{DD}Qn = +2.375V)	2.0	--	V
		I_{OH} = -2mA (Pins: LOCK)	2.4	--	V
I_{OS}Qn [2]	Short-circuit output current	V_O = V_{DD}Qn or V_{SS}; V_{DD}Qn = +2.75V; PE/HD = MID	-500	500	mA
		V_O = V_{DD}Qn or V_{SS}; V_{DD}Qn = +2.75V; PE/HD = LOW or HIGH	-300	300	mA
I_{DDOP} [3]	Dynamic supply current	@200MHz (FS = HIGH); V_{DD} = Max; V_{DD}Qn = +2.75V; C_L = 40pF/output	--	250	mA
		@100MHz (FS = MID); V_{DD} = Max; V_{DD}Qn = +2.75V; C_L = 40pF/output	--	150	mA
		@50MHz (FS = LOW); V_{DD} = Max; V_{DD}Qn = +2.75V; C_L = 40pF/output	--	100	mA
C_{OUT} [4]	Output pin capacitance	*f* = 1MHz @ 0V; V_{DD} = Max; V_{DD}Qn = +2.75V	15		pF

(V_{DD}Qn = +3.3V ± 0.3V; V_{DD} = +3.3V ± 0.3V; T_C = -55°C to +125°C)

Symbol	Description	Conditions	Min.	Max.	Units
V_{OL}	Output low voltage	I_{OL} = 12mA (PE/HD = LOW or HIGH); (Pins: nQ[1:0])	--	0.4	V
		I_{OL} = 24mA (PE/HD = MID); (Pins: nQ[1:0])	--	0.4	V
		I_{OL} = 2mA (Pins: LOCK)	--	0.4	V
V_{OH}	High-level output voltage	I_{OH} = -12mA (PE/HD = LOW or HIGH); (Pins: nQ[1:0])	2.4	--	V
		I_{OH} = -24mA (PE/HD = MID); (Pins: nQ[1:0])	2.4	--	V
		I_{OH} = -2mA (Pins: LOCK)	2.4	--	V
I_{OS}Qn [2]	Short-circuit output current	V_O = V_{DD}Qn or V_{SS}; V_{DD}Qn = +3.6V; PE/HD = MID	-600	600	mA
		V_O = V_{DD}Qn or V_{SS}; V_{DD}Qn = +3.6V; PE/HD = LOW or HIGH	-300	300	mA
I_{DDOP} [3]	Dynamic supply current	@200MHz (FS = HIGH); V_{DD} = Max; V_{DD}Qn = +3.6V; C_L = 40pF/output	--	400	mA
		@100MHz (FS = MID); V_{DD} = Max; V_{DD}Qn = +3.6V; C_L = 40pF/output	--	230	mA
		@50MHz (FS = LOW); V_{DD} = Max; V_{DD}Qn = +3.6V; C_L = 40pF/output	--	150	mA
C_{OUT} [4]	Output pin capacitance	*f* = 1MHz @ 0V; V_{DD} = Max; V_{DD}Qn = +3.6V	15		pF

Notes: * Post-radiation performance guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to a TID level of 1.0E6 rad(Si).

1. Unless otherwise noted, these tests are performed with V_{DD} and V_{DD}Qn at their minimum levels.
2. Supplied as a design limit. Neither guaranteed nor tested.
3. When measuring the dynamic supply current, all outputs are loaded in accordance with the equivalent test load defined in figure 10.
4. Capacitance is measured for initial qualification and when design changes may affect the input/output capacitance. Capacitance is measured between the designated terminal and V_{SS} at frequency of 1MHz and a signal amplitude of 50mV rms maximum.

8.0 AC INPUT ELECTRICAL CHARACTERISTICS (Pre- and Post-Radiation)*

(V_{DD} = +3.3V ± 0.3V; T_C = -55°C to +125°C) (V_{DD}Qn = +3.3V nominal unless otherwise noted) (Note 1)

Symbol	Description	Condition	Min.	Max.	Unit
t_R, t_F [2, 3]	Input rise/fall time	VIH(min)-VIL(max)	--	20	ns/V
t_{PWC}	Input clock pulse	HIGH or LOW	2	--	ns
t_{XTAL}	Input clock period	$1 \div F_{XTAL}$	5	500	ns
t_{DCIN}	Input clock duty cycle	HIGH or LOW	10	90	%
f_{XTAL} [4]	Reference input frequency	FS = LOW; $\overline{PD}$/DIV = HIGH	2	50	MHz
		FS = LOW; $\overline{PD}$/DIV = MID	4	100	MHz
		FS = MID; $\overline{PD}$/DIV = HIGH	4	100	MHz
		FS = MID; $\overline{PD}$/DIV = MID	8	200	MHz
		FS = HIGH; $\overline{PD}$/DIV = HIGH	8	200	MHz
		FS = HIGH; $\overline{PD}$/DIV = MID	16	200	MHz

Notes:
* Post-radiation performance guaranteed at 25°C per MIL-STD-883 Method 1019.
1. Reference Figure 11 for clock output loading circuit that is equivalent to the load circuit used for all AC testing.
2. Supplied only as a design guideline, neither tested nor guaranteed.
3. When driving the UT7R995C with a crystal, the XTAL1 pin does not define maximum input rise/fall time.
4. Although the input reference frequencies are defined as-low-as 2MHz, the N and R dividers must be selected to ensure the PLL operates from 24MHz-50MHz when FS = LOW, 48MHz-100MHz when FS = MID, and 96MHz-200MHz when FS = HIGH.

9.0 AC OUTPUT ELECTRICAL CHARACTERISTICS (Pre- and Post-Radiation)*

(V_{DD} = +3.3V ± 0.3V; T_C = -55°C to +125°C) (Note 1)

Symbol	Description	Condition	Min.	Max.	Unit
f_{OR}	Output frequency range	V_{DD}Qn = +3.3V	6	200	MHz
VCO_{LR}	VCO lock range	V_{DD}Qn = +3.3V	24	200	MHz
VCO_{LBW} [2]	VCO loop bandwidth	V_{DD} = V_{DD}Qn = +3.3V; T_C = Room Temperature	0.25	3.5	MHz
t_{SKEWPR} [3]	Matched-pair skew	Skew between the earliest and the latest output transitions within the same bank.	--	100	ps
t_{SKEW0} [3]	Output-output skew	Skew between the earliest and the latest output transitions among all outputs at $0t_U$.	--	200	ps
t_{SKEW1} [3]		Skew between the earliest and the latest output transitions among all outputs for which the same phase delay has been selected.	--	200	ps
t_{SKEW2} [3]		Skew between the nominal output rising edge to the inverted output falling edge	--	500	ps
t_{SKEW3} [3]		Skew between non-inverted outputs running at different frequencies.	--	500	ps
t_{SKEW4} [3]		Skew between nominal to inverted outputs running at different frequencies.	--	500	ps
t_{SKEW5} [3]		Skew between nominal outputs at different power supply levels.	--	650	ps
t_{PART} [8]	Part-part skew	Skew between the outputs of any two devices under identical settings and conditions (V_{DD}Qn, V_{DD}, temp, air flow, frequency, etc).	--	750	ps

Symbol	Description	Condition		Min.	Max.	Unit
t_{PD0} [4, 8]	XTAL1 to FB propagation delay	V_{DD} = V_{DD}Qn = +3.3V; T_C = Room Temperature		-250	+250	ps
t_{ODCV}	Output duty cycle	fout < 100 MHz, measured at V_{DD}÷2		48	52	%
		fout > 100 MHz, measured at V_{DD}÷2		45	55	%
t_{PWH}	Output high time deviation from 50%	Measured at 2.0V; V_{DD}Qn = +3.3V		--	1.5	ns
t_{PWL}	Output low time deviation from 50%	Measured at 0.8V; V_{DD}Qn = +3.3V		--	2.0	ns
t_{ORISE} & t_{OFALL}	Output rise/fall time	Measured as transition time between V_{OH} = +1.7V and V_{OL} = +0.7V for V_{DD}Qn = +2.5V; C_L = 40pF	PE/HD = HIGH	0.5	1.5	ns
			PE/HD = MID	0.25	1.25	ns
		Measured as transition time between V_{OH} = +2.0V and V_{OL} = +0.8V for V_{DD}Qn = +3.3V; C_L = 40pF	PE/HD = HIGH	0.20	1.25	ns
			PE/HD = MID	0.10	1.0	ns
t_{LOCK} [5]	PLL lock time			--	1	ms
$t_{LOCKRES}$ [2, 6]	LOCK Pin Resolution	FS = LOW		1.6ns ± 200ps typ.		ns
		FS = MID		1.6ns ± 200ps typ.		ns
		FS = HIGH		800ps ± 100ps typ.		ps
t_{CCJ} [7]	Cycle-cycle jitter	Divide by 1 output frequency, FS = LOW, FB = divide by 12		--	100	ps
		Divide by 1 output frequency FS = MID or HIGH, FB = divide by 12		--	150	ps

Notes:
1. Reference Figure 11 for clock output loading circuit that is equivalent to the load circuit used for all AC testing.
2. Supplied as a design guideline. Neither guaranteed nor tested.
3. Test load = 40pF, terminated to V_{DD}÷2. All outputs are equally loaded. See figure 11.
4. t_{PD} is measured at 1.5V for V_{DD} = 3.3V with XTAL1 rise/fall times of 1ns between 0.8V-2.0V.
5. t_{LOCK} is the time that is required before outputs synchronize to XTAL1 as determined by the phase alignment between the XTAL1 and FB inputs. This specification is valid with stable power supplies which are within normal operating limits.
6. Lock detector circuit will monitor the phase alignment between the XTAL1 and FB inputs. When the phase separation between these two inputs is greater than the amount listed, then the LOCK pin will drop low signaling that the PLL is out of lock.
7. This parameter is guaranteed by measuring cycle-cycle jitter on 2^{16}, back-to-back clock cycles.
8. Guaranteed by characterization, but not tested.

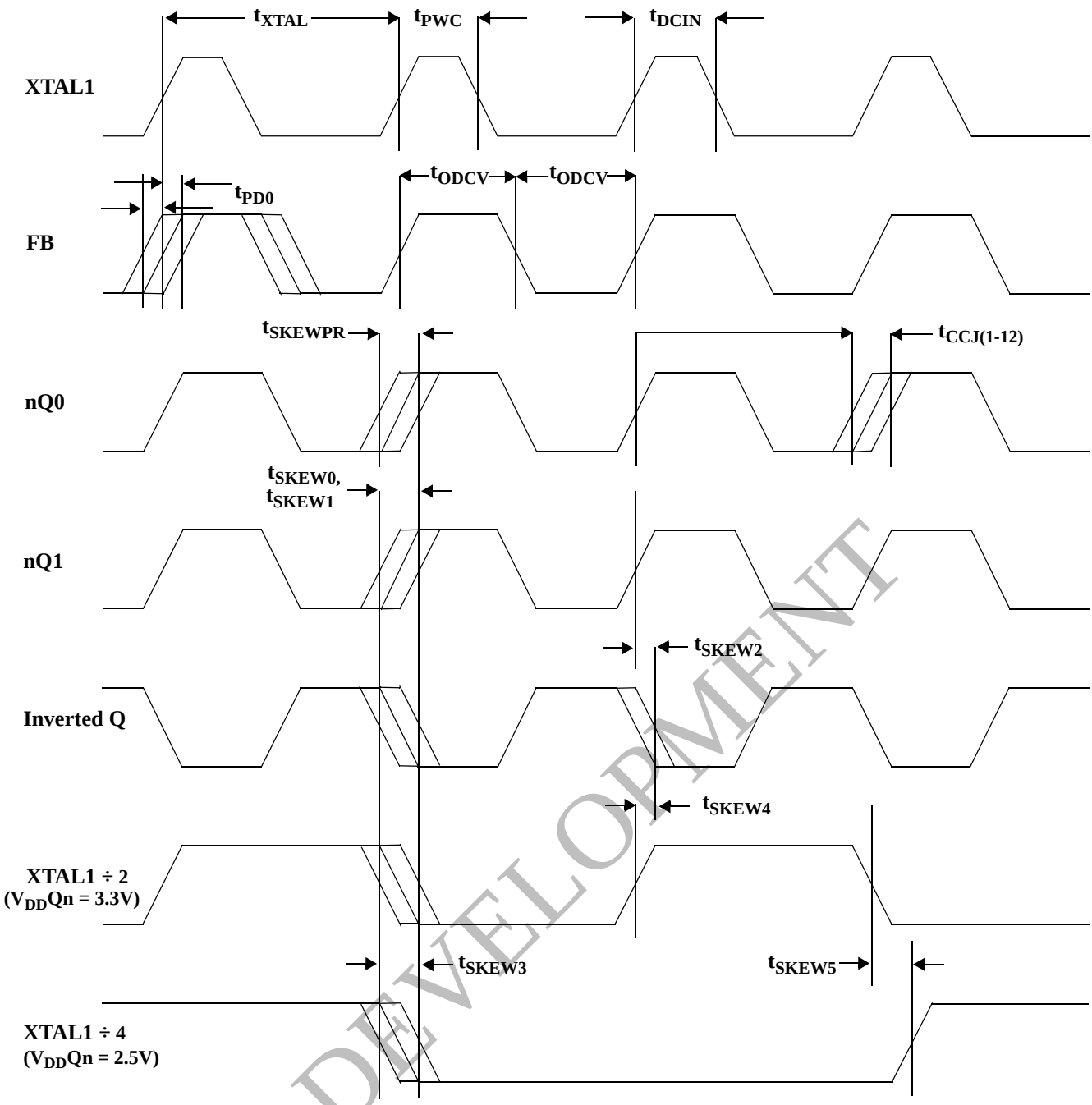


Figure 6. AC Timing Diagram

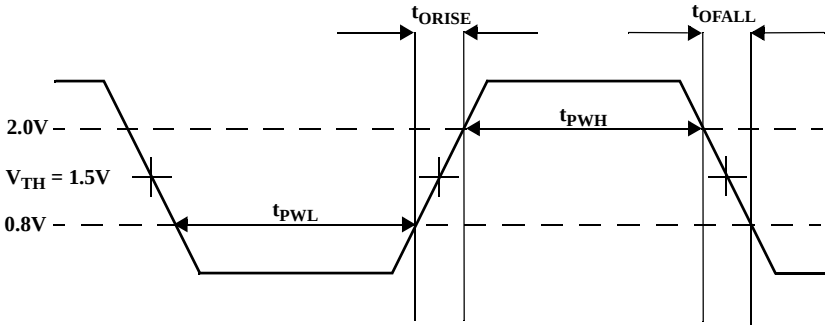


Figure 7. +3.3V LVTTL Output Waveform

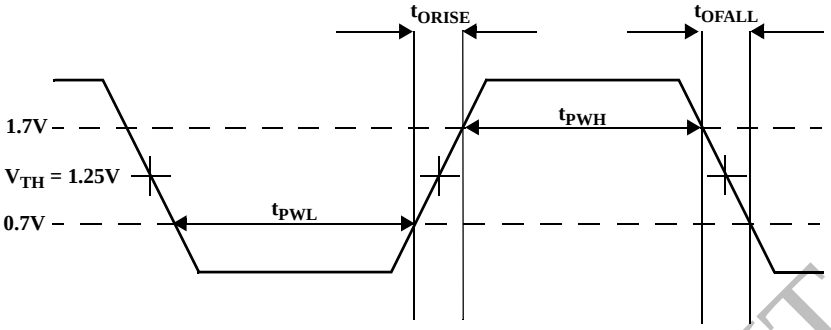


Figure 8. +2.5V LVTTL Output Waveform

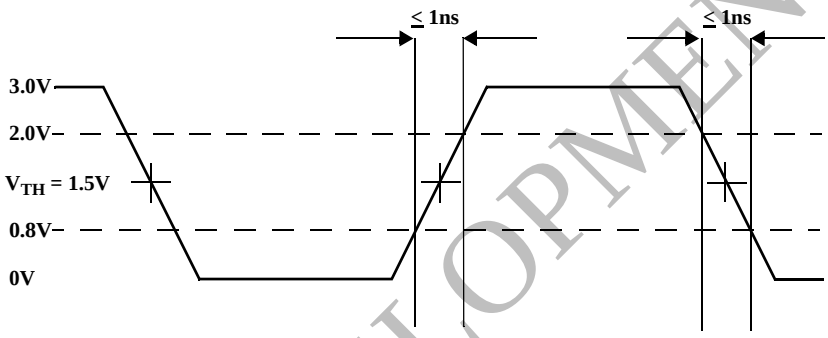


Figure 9. +3.3V LVTTL Input Test Waveform

Figure 10.
Output Test Load Circuit for LOCK and Dynamic Power Supply Current Measurements

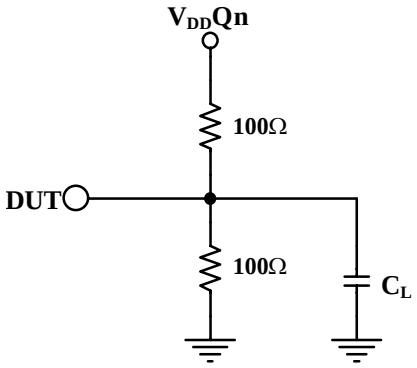
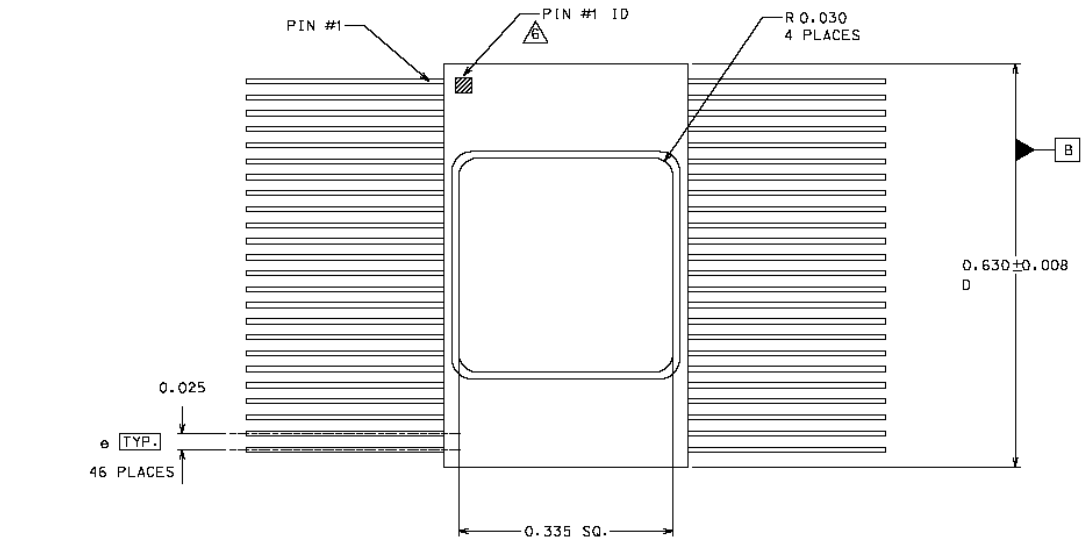
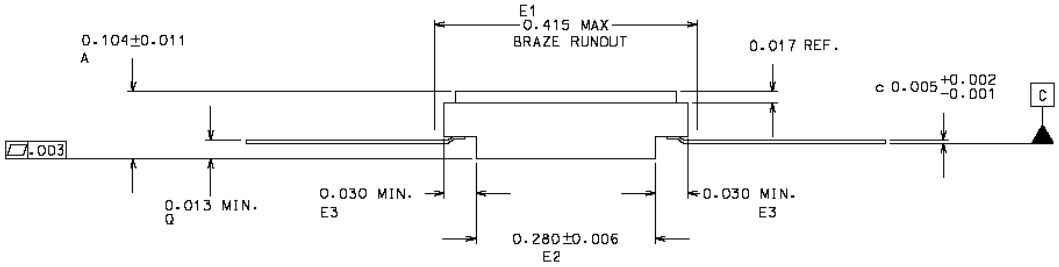
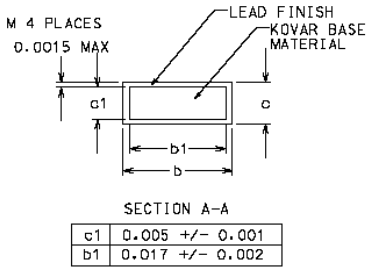


Figure 11.
Clock Output AC Test Load Circuit

Note: This is not the recommended termination for normal user operation.

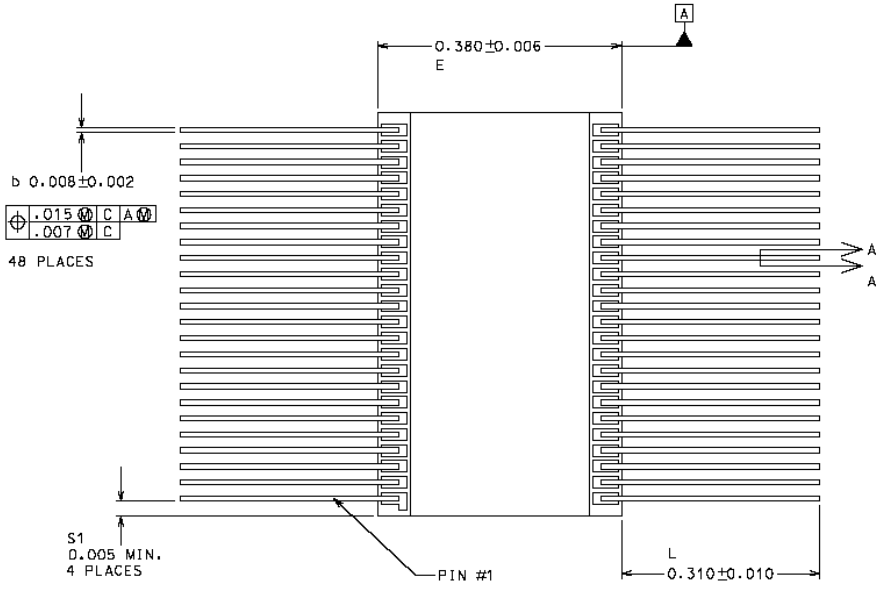






SECTION A-A

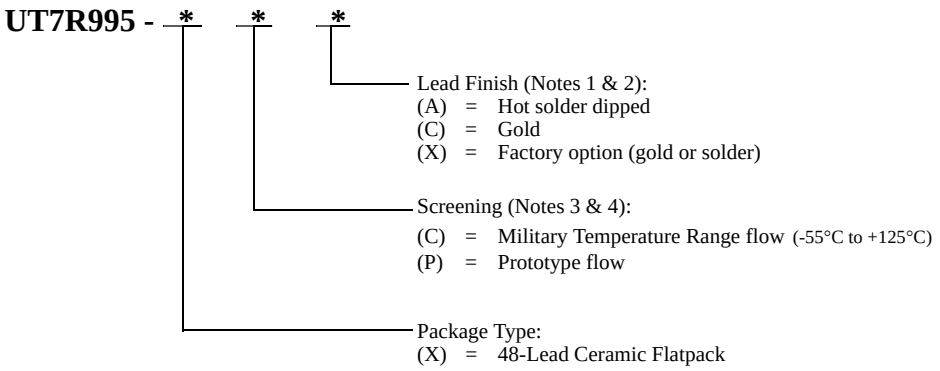
c1	0.005 +/- 0.001
b1	0.017 +/- 0.002

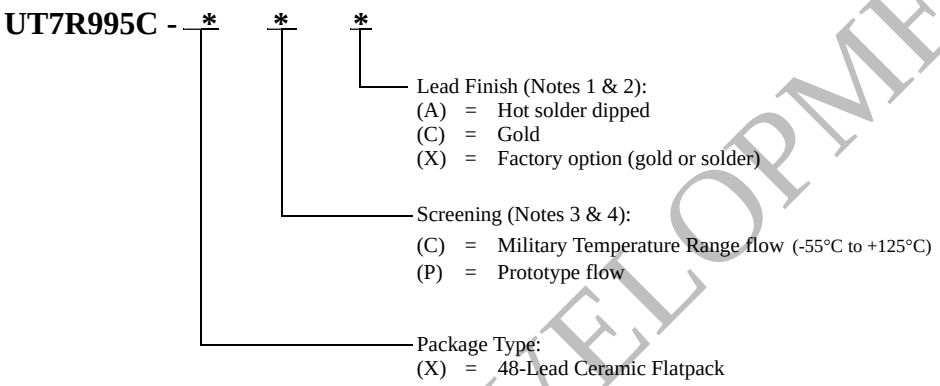


NOTES:
1. ALL EXPOSED METALIZED AREAS MUST BE GOLD PLATED OVER ELECTRICALLY PLATED NICKEL PER MIL-PRF-38535.
2. THE LID IS ELECTRICALLY CONNECTED TO VSS.
3. LEAD FINISHES ARE IN ACCORDANCE WITH MIL-PRF-38535.
4. DIMENSION SYMBOLOGY IS IN ACCORDANCE WITH MIL-PRF-38535.
5. LEAD POSITION AND COPLANARITY ARE NOT MEASURED
6. ID MARK SYMBOL IS VENDOR OPTION; NO ALPHANUMERICS.

ORDERING INFORMATION

UT7R995 and UT7R995C:





Notes:
1. Lead finish (A,C, or X) must be specified.
2. If an "X" is specified when ordering, then the part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
3. Prototype flow per UTMC Manufacturing Flows Document. Tested at 25°C only. Lead finish is GOLD ONLY. Radiation neither tested nor guaranteed.
4. Military Temperature Range flow per Aeroflex Colorado Springs Manufacturing Flows Document. Devices are tested at -55°C, room temp, and 125°C. Radiation neither tested nor guaranteed.

UT7R995 and UT7R995C: SMD

5962 * 05214 ** * * *

Lead Finish (Notes 1 & 2):
(A) = Hot solder dipped
(C) = Gold
(X) = Factory Option (gold or solder)

Case Outline:
(X) = 48-Lead Ceramic Flatpack

Class Designator:
(Q) = QML Class Q
(V) = QML Class V

Device Type
(01) = UT7R995 -> 6MHz-to-200MHz, High Speed, Multi-Phase, Zero-Delay, without Crystal Capability
(02) = UT7R995C -> 6MHz-to-200MHz, High Speed, Multi-Phase, Zero-Delay, with Crystal Capability

Drawing Number: 5962-05214

Total Dose (Note 3):
(R) = 1E5 rads(Si)
(F) = 3E5 rads(Si)
(G) = 5E5 rads(Si)
(H) = 1E6 rads(Si)

Federal Stock Class Designator: No options

Notes:
1.Lead finish (A,C, or X) must be specified.
2.If an "X" is specified when ordering, part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
3.Total dose radiation must be specified when ordering. QML Q and QML V are not available without radiation hardening.

NOTES:

NOTES:

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