Signetics

54F538
Decoder

1-of-8 Decoder (3-State)

Product Specification

Military Logic Product

DESCRIPTION

The 54F538 decoder/demultiplexer accepts three address (A_0 - A_3) input signals and decodes them to select one of eight mutually exclusive outputs. A polarity control (P) input determines whether the outputs are active Low or active High. The 54F538 has 3-State outputs and a High signal on the Output Enables ($\overline{OE}n$) will force all outputs to the high impedance state. Two active High and two active Low Enable inputs are available for easy expansion to 1-of-32 decoding with four packages, or for data demultiplexing to 1-of-8 or 1-of-16 destinations.

ORDERING INFORMATION

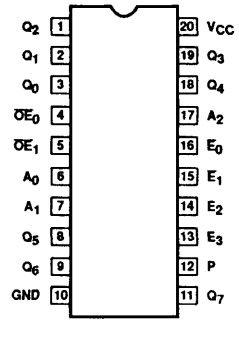
DESCRIPTION	ORDER CODE
20-Pin Ceramic DIP	54F538/BRA
20-Pin Ceramic FlatPack	54F538/BSA
20-Pin Ceramic LLCC	54F538/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0 - A_2	Address inputs	1.0/1.0	20µA/0.6mA
$\overline{E}_0$, $\overline{E}_1$	Enable input (Active Low)	1.0/1.0	20µA/0.6mA
E_2, E_3	Enable input (Active High)	1.0/1.0	20µA/0.6mA
P	Polarity control input	1.0/1.0	20µA/0.6mA
$\overline{OE}_0$, $\overline{OE}_1$	Output enable input (Active Low)	1.0/1.0	20µA/0.6mA
Q_0 - Q_7	Data outputs	150/33	3.0mA/20mA

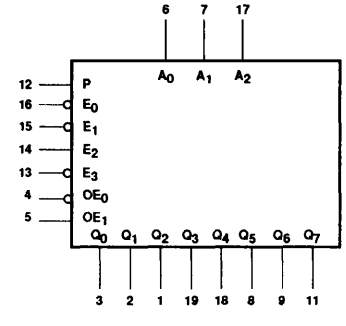
NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



For LLCC pin assignments, see JEDEC Standard No. 2

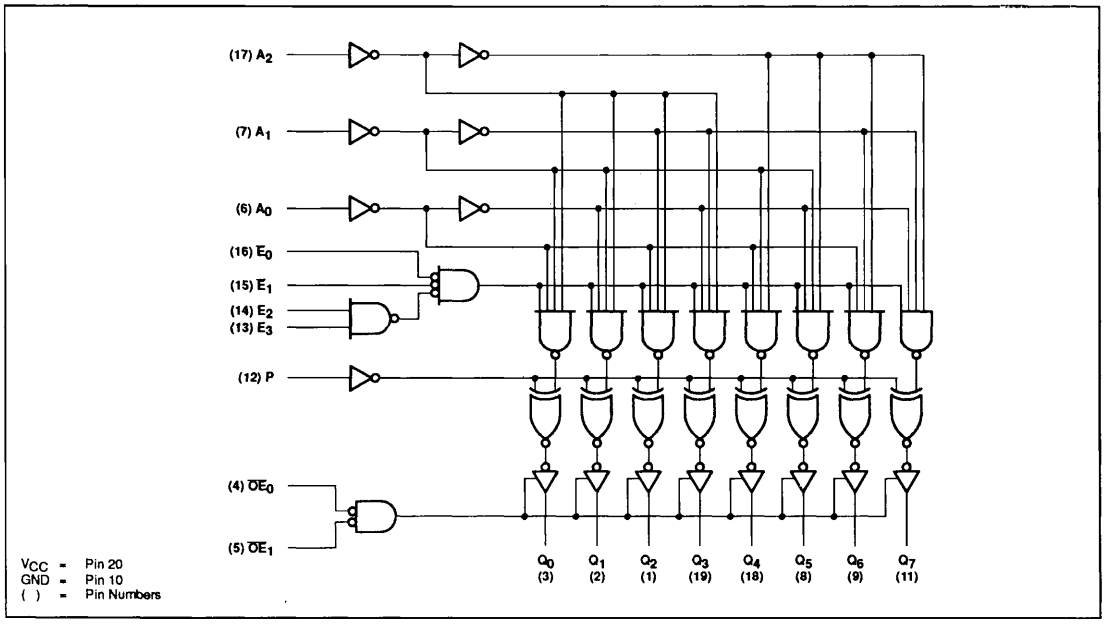
LOGIC SYMBOL



VCC = Pin 20
GND = Pin 10

For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS									OUTPUTS								OPERATING MODE
$\overline{OE}_0$	$\overline{OE}_1$	E_0	$\overline{E}_1$	E_2	E_3	A_2	A_1	A_0	Q_0	Q_1	Q2	Q3	Q4	Q5	Q6	Q7	
H	X	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z	High Impedance
X	H	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z	
L	L	H	X	X	X	X	X	X	Outputs equal P input								Disable
L	L	X	H	X	X	X	X	X									
L	L	X	X	L	X	X	X	X									
L	L	X	X	X	L	X	X	X									
L	L	L	L	H	H	L	L	L	H	L	L	L	L	L	L	L	Active High output (P = L)
L	L	L	L	H	H	L	L	H	L	H	L	L	L	L	L	L	
L	L	L	L	H	H	L	H	L	L	L	H	L	L	L	L	L	
L	L	L	L	H	H	L	H	H	L	L	L	H	L	L	L	L	
L	L	L	L	H	H	H	L	L	L	L	L	L	H	L	L	L	
L	L	L	L	H	H	H	L	H	L	L	L	L	L	H	L	L	
L	L	L	L	H	H	H	H	L	L	L	L	L	L	L	H	L	
L	L	L	L	H	H	H	H	H	L	L	L	L	L	L	L	H	
L	L	L	L	H	H	L	L	L	H	H	H	H	H	H	H	H	Active Low output (P = H)
L	L	L	L	H	H	L	L	H	H	L	H	H	H	H	H	H	
L	L	L	L	H	H	L	H	L	H	H	L	H	H	H	H	H	
L	L	L	L	H	H	L	H	H	H	H	H	L	H	H	H	H	
L	L	L	L	H	H	H	L	L	H	H	H	H	L	H	H	H	
L	L	L	L	H	H	H	L	H	H	H	H	H	H	L	H	H	
L	L	L	L	H	H	H	H	L	H	H	H	H	H	H	L	H	
L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.5 to +7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +5.0	mA
V_O	Voltage applied to output in High output state range	-0.5 to +5.5	V
I_O	Current applied to output in Low output state	48	mA
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	ma
I_{OH1}	High-level output current			-1.0	mA
I_{OH2}	High-level output current			-3.0	mA
I_{OL}	Low-level output current			20.0	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = Min, V_{IL} = Max,	I_{OH1} = -1.0mA	2.5			V
			V_{IH} = Min	I_{OH2} = -3.0mA	2.4	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = Min, V_{IL} = Max, I_{OL} = Max, V_{IH} = Min			0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = Min, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum		V_{CC} = Max, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = Max, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = Max, V_I = 0.5V				-0.6	mA
I_{OZH}	Off-state current High-level voltage applied		V_{CC} = Max, V_O = 2.7V				50	µA
I_{OZL}	Off-state current Low-level voltage applied		V_{CC} = Max, V_O = 0.5V				-50	µA
I_{OS}	Short-circuit output current[3]		V_{CC} = Max		-60		-150	mA
I_{CC}	Supply current	I_{CCH}	V_{CC} = Max			30	40	mA
		I_{CCL}				35	50	mA
		I_{CCZ}				35	50	mA

AC ELECTRICAL CHARACTERISTICS

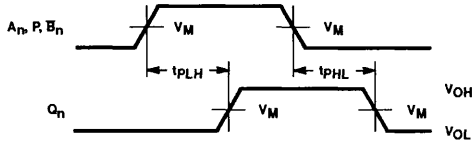
(When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to Q_n	Waveform 1, 2	5.5 3.0	6.5 7.5	13.0 12.5	5.0 3.0	14.0 13.5	ns ns
t_{PLH} t_{PHL}	Propagation delay E_0 or $\overline{E}_1$ to Q_n	Waveform 1, 2	5.5 3.0	8.5 7.5	12.0 12.0	5.0 3.0	13.0 12.5	ns ns
t_{PLH} t_{PHL}	Propagation delay E_2 or $\overline{E}_3$ to Q_n	Waveform 1, 2	6.5 4.0	9.0 7.0	12.5 12.5	5.5 3.5	13.5 13.0	ns ns
t_{PLH} t_{PHL}	Propagation delay P to Q_n	Waveform 1, 2	4.5 3.5	9.5 6.5	15.0 10.0	4.0 3.5	16.5 10.5	ns ns
t_{PZL} t_{PZL}	Output Enable time $\overline{OE}_0$ or $\overline{OE}_1$ to Q_n	Waveform 3 Waveform 4	2.5 6.5	5.5 9.5	9.5 13.5	2.0 6.0	11.0 15.0	ns ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}_0$ or $\overline{OE}_1$ to Q_n	Waveform 3 Waveform 4	1.0 1.0	3.0 3.5	6.0 8.5	1.0 1.0	7.0 9.5	ns ns

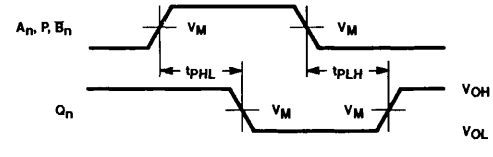
NOTES:

1. For conditions shown as Min or Max, use the appropriate value under the recommended operating conditions for the applicable conditions.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} should be performed last.

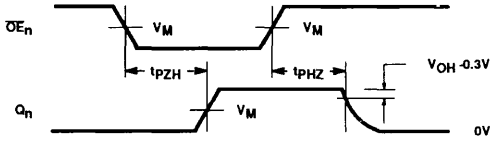
AC WAVEFORMS



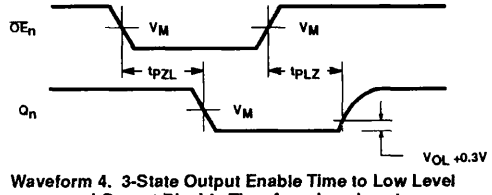
Waveform 1. Propagation Delay for Non-Inverting Outputs



Waveform 2. Propagation Delay for Inverting Outputs



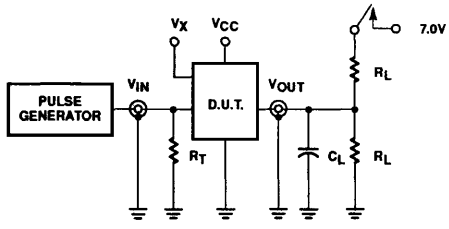
Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level



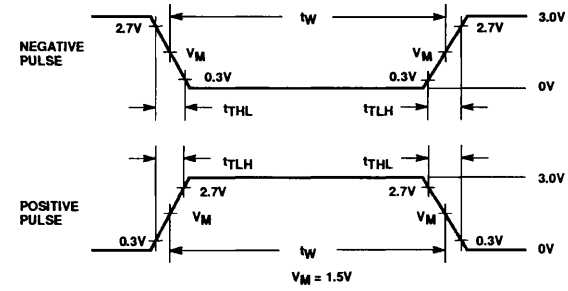
Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

V_M = 1.5V

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs and Open Collector Outputs



Input Pulse Definitions

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open

INPUT PULSE CHARACTERISTICS				
Family	**Rep. Rate**	**Pulse Width**	**t_{TLH}**	**t_{THL}**
54F	1MHz	500ns	≤2.5ns	≤2.5ns

DEFINITIONS:
R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V; ≥2.7V or open per Function Table.