Integrated Device Technology, Inc.

BiCMOS STATIC RAM 64K (8K x 8-BIT) CACHE-TAG RAM

PRELIMINARY INFORMATION
IDT71B74

FEATURES:

- High-speed address to MATCH comparison time
  - — Military: 15/18/25ns (max.)
  - — Commercial: 12/15/18ns (max.)
- High-speed address access time
  - — Military: 12/15/20ns (max.)
  - — Commercial: 10/12/15ns (max)
- High-speed chip select access time
  - — Military: 8/10/12ns (max.)
  - — Commercial: 6/8/10ns (max.)
- High-speed asynchronous RAM Clear on Pin 1
- Produced with advanced BiCEMOS™ high-performance technology
- Single 5V (+10%) power supply
- Input and output directly TTL-compatible
- Military product compliant to MIL-STD-883, Class B
- Standard 28-pin plastic and hermetic DIP (300 mil), 28-pin SOJ (300 mil)

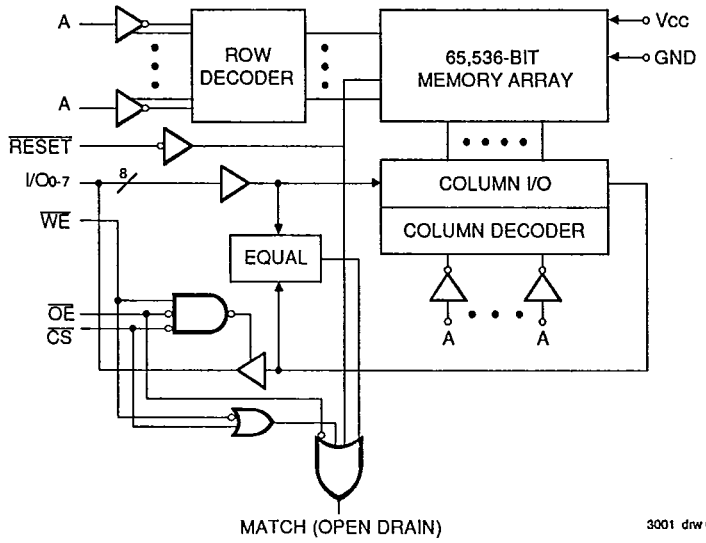
DESCRIPTION:

The IDT71B74 is a high-speed cache address comparator subsystem consisting of a 65,536-bit static RAM organized as 8K x 8 and an 8-bit comparator. A single IDT71B74 can map 8K cache words into a 1 megabyte address space by comparing 20 bits of address organized as 13 word cache address bits and 7 upper address bits. Two IDT71B74s can be combined to provide 28 bits of address comparison, etc. The IDT71B74 also provides a single RAM clear control, which clears all words in the internal RAM to zero when activated. This allows the tag bits for all locations to be cleared at power-on or system-reset, a requirement for cache comparator systems. The IDT71B74 can also be used as an 8K x 8 high-speed static RAM.

The IDT71B74 is fabricated using IDT's high-performance, high-reliability technology — CEMOS™. Address access times as fast as 12ns, chip select times of 6ns and address-to-comparison times of 10ns are available with maximum power consumption of 825mW.

The MATCH pin of several IDT71B74s can be wired-ORed together to provide enabling or acknowledging signals to the data cache or processor, thus eliminating logic delays and increasing system throughput. The device operates from a single 5V supply.

FUNCTIONAL BLOCK DIAGRAM



3001 drw 01

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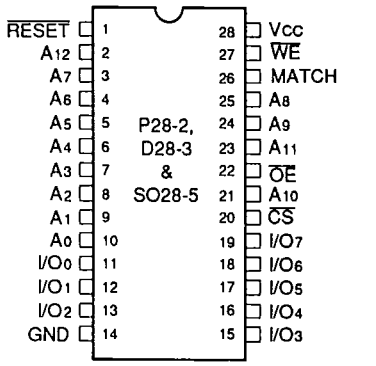
PIN CONFIGURATION



3001 drw 02

DIP/SOIC
TOP VIEW

TRUTH TABLE[1]

WE	CS	OE	RESET	MATCH	I/O	Function
X	X	X	L	H	—	Reset all bits to low
X	H	X	H	H	Hi Z	Deselect chip
H	L	H	H	L	DIN	No MATCH
H	L	H	H	H	DIN	MATCH
H	L	L	H	H	DOUT	Read
L	L	X	H	H	DIN	Write

NOTE:
1. H = VIH, L = VIL, X = DON'T CARE

3001 tbl 01

PIN DESCRIPTIONS

A0–12	Address
I/O0-7	Data Input/Output
CS	Chip Select
RESET	Memory Reset
MATCH	Data/Memory Match (Open Drain)
WE	Write Enable
OE	Output Enable
GND	Ground
Vcc	Power

3001 tbl 02

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Com'l.	Mil.	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +150	°C
PT	Power Dissipation	1.0	1.0	W
IOUT	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

3001 tbl 03

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 0V	8	pF
COUT	Output Capacitance	VOUT = 0V	8	pF

NOTE:
1. This parameter is determined by device characterization, but is not production tested.

3001 tbl 04

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RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage(1)	2.2	—	6.0	V
V_{IHR}	$\overline{RESET}$ Input Voltage	2.5(2)	—	6.0	V
V_{IL}	Input Low Voltage	-0.5(3)	—	0.8	V

3001 tbl 05

NOTE:
1. All inputs except $\overline{RESET}$.
2. When using bipolar devices to drive the $\overline{RESET}$ input, a pullup resistor of 1kΩ-10kΩ is usually required to assure this voltage.
3. V_{IL} (min.) = -3.0V for pulse width less than 5ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5V ± 10%
Commercial	0°C to +70°C	0V	5V ± 10%

3001 tbl 06

DC ELECTRICAL CHARACTERISTICS(1)

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	71B74S12		71B74S15		71B74S18		71B74S25		Unit
		Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
I_{CC}	Dynamic Operating Current Outputs Open, V_{CC} = Max., f = f_{MAX}	190	—	170	190	150	170	—	170	mA

3001 tbl 07

NOTE:
1. All values are maximum guaranteed values.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMERATURE AND SUPPLY VOLTAGE (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition		IDT71B74S Min.	IDT71B74S Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL.	—	10	µA
			COM'L.	—	5	
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL.	—	10	µA
			COM'L.	—	5	
V_{OL}	Output Low Voltage	I_{OL} = 18mA MATCH		—	0.5	V
		I_{OL} = 22mA MATCH		—	0.5	
		I_{OL} = 10mA, V_{CC} = Min. (Except MATCH)		—	0.5	
		I_{OL} = 8mA, V_{CC} = Min. (Except MATCH)		—	0.4	
V_{OH}	Output High Voltage	I_{OL} = -4mA, V_{CC} = Min. (Except MATCH)		2.4	—	V

3001 tbl 08

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1, 2 and 3

3001 tbl 09

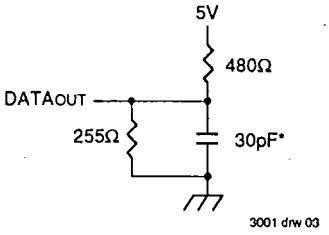


Figure 1. Output Load

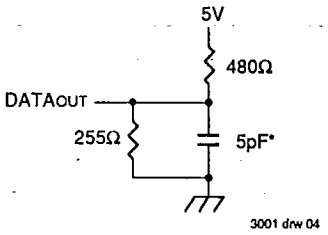
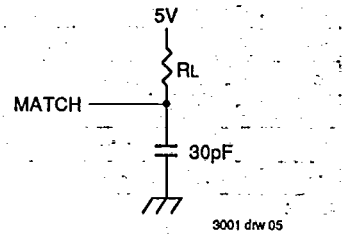


Figure 2. Output Load
(for tCLZ, tOLZ, tCHZ, tOHZ, tOW, tWHZ)

*Includes scope and jig.



RL = 200Ω (COM'L.)
= 270Ω (MIL.)

Figure 3. Output Load for MATCH

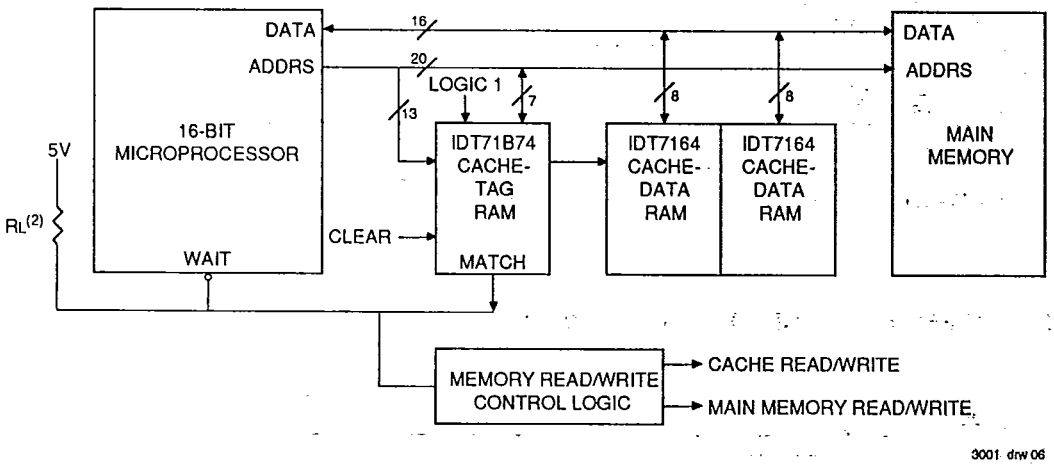


Figure 4. Example of Cache Memory System Block Diagram

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NOTES:
1. For more information, see application note AN-07 "Cache-Tag RAM Chips Simplify Cache Memory Design".
2. RL = 200Ω (commercial) or 270Ω (military).

AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

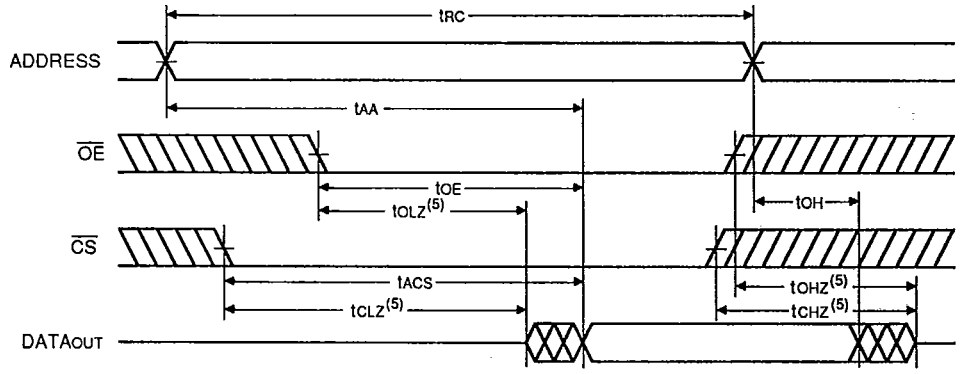
T-46-23-12

Symbol	Parameter	71B74S12[1] Min.	71B74S12[1] Max.	71B74S15 Min.	71B74S15 Max.	71B74S18 Min.	71B74S18 Max.	71B74S25[2] Min.	71B74S25[2] Max.	Unit
Read Cycle										
tRC	Read Cycle Time	10	—	12	—	15	—	20	—	ns
tAA	Address Access Time	—	10	—	12	—	15	—	20	ns
tACS	Chip Select Access Time	—	6	—	6	—	8	—	10	ns
tCLZ	Chip Select to Output in Low Z[3]	2	—	2	—	3	—	5	—	ns
tOE	Output Enable to Output Valid	—	6	—	7	—	8	—	10	ns
tOLZ	Output Enable to Output in Low Z[3]	2	—	3	—	3	—	3	—	ns
tCHZ	Chip Select to Output in High Z[3]	—	5	—	6	—	7	—	8	ns
tOHZ	Output Disable to Output in High Z[3]	—	4	—	6	—	6	—	8	ns
tOH	Output Hold from Address Change	2	—	3	—	3	—	3	—	ns

NOTES:
1. 0° to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter is guaranteed, but not tested.

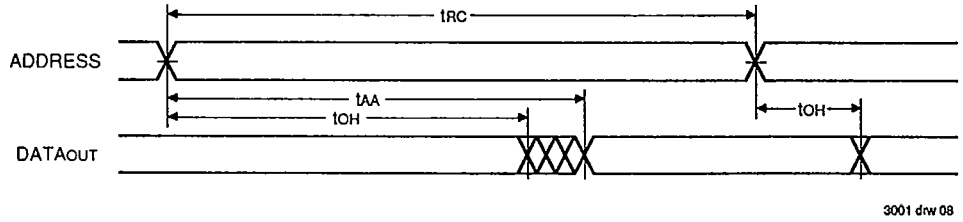
3001 tbl 10

TIMING WAVEFORM OF READ CYCLE NO. 1[1]



3001 drw 07

TIMING WAVEFORM OF READ CYCLE NO. 2[1, 2, 4]



3001 drw 08

NOTES:
1. $\overline{WE}$ is high for read cycle.
2. Device is continuously selected, $\overline{CS}$ = VIL.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = VIL.
5. Transition is measured ±200mV from steady state.

T-46-23-12

AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

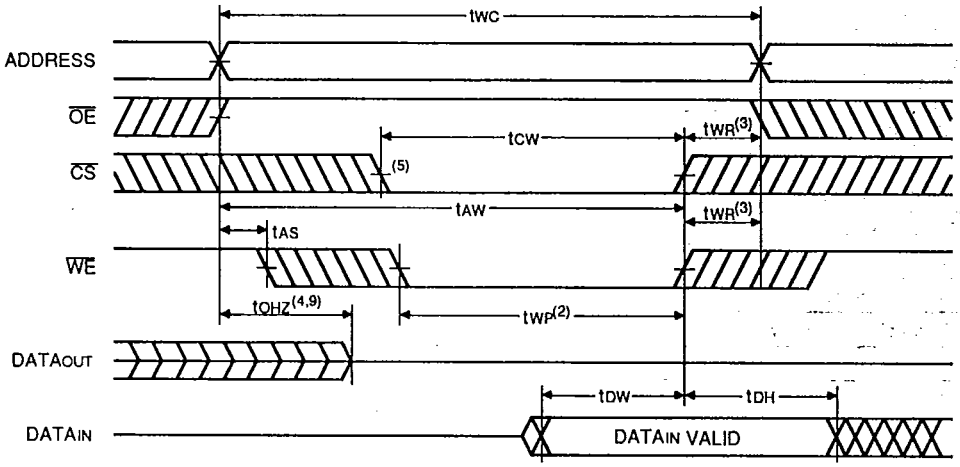
Symbol	Parameter	71B74S12[1] Min.	71B74S12[1] Max.	71B74S15 Min.	71B74S15 Max.	71B74S18 Min.	71B74S18 Max.	71B74S25[2] Min.	71B74S25[2] Max.	Unit
Write Cycle										
tWC	Write Cycle Time	10	—	12	—	15	—	20	—	ns
tCW	Chip Select to End of Write	8	—	10	—	12	—	15	—	ns
tAW	Address Valid to End of Write	8	—	10	—	12	—	15	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	7	—	9	—	12	—	15	—	ns
tWR	Write Recovery Time ($\overline{CS}$, $\overline{WE}$)	0	—	0	—	0	—	0	—	ns
tWHZ	Write Enable to Output in High Z[3]	—	5	—	6	—	7	—	8	ns
tDW	Data Valid to End of Write	5	—	6	—	9	—	10	—	ns
tDH	Data Hold from Write Time	0	—	0	—	0	—	0	—	ns
tOW	Output Active from End of Write[3]	2	—	2	—	3	—	5	—	ns

3001 tbl 07

NOTES:
1. 0° to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter is guaranteed, but not tested.

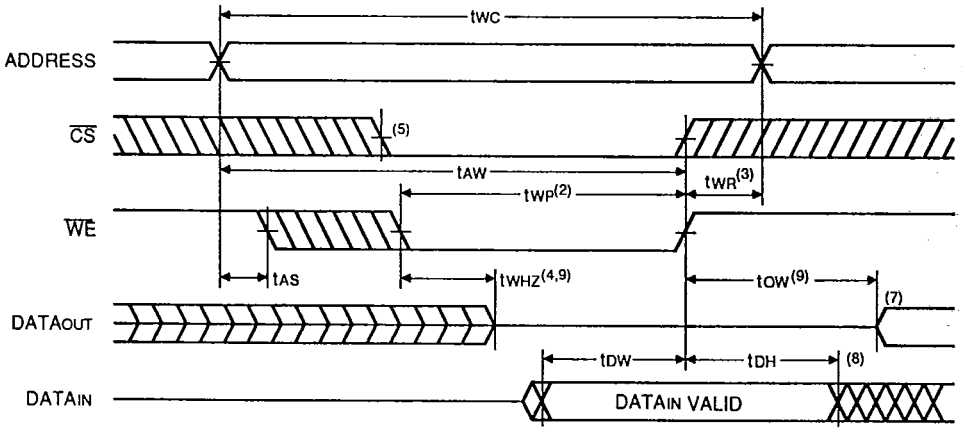
6

TIMING WAVEFORM OF WRITE CYCLE NO. 1(1)



3001 drw 10

TIMING WAVEFORM OF WRITE CYCLE NO. 2(1, 6)



3001 drw 11

NOTES:
1. $\overline{WE}$, $\overline{CS}$ must be inactive during all address transitions.
2. A write occurs during the overlap (tWP) of a low $\overline{WE}$ and a low $\overline{CS}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. $\overline{OE}$ is continuously low ($\overline{OE}$ = VIL).
7. DATAOUT is the same phase of write data of this write cycle.
8. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Data input signals of opposite phase to the outputs must not be applied to them.
9. Transition is measured ±200mV from steady state.

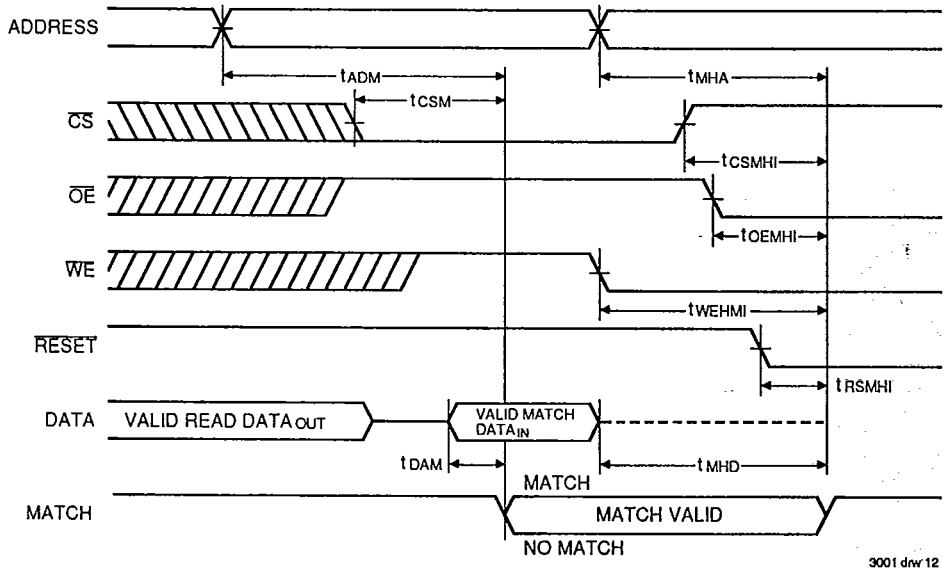
AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges) T-46-23-12

Symbol	Parameter	71B74S12[1] Min.	71B74S12[1] Max.	71B74S15 Min.	71B74S15 Max.	71B74S18 Min.	71B74S18 Max.	71B74S25[2] Min.	71B74S25[2] Max.	Unit
Match Cycle										
tADM	Address to MATCH Valid	—	12	—	15	—	18	—	25	ns
tCSM	Chip Select to MATCH Valid	—	8	—	10	—	12	—	17	ns
tCSMHI	Chip Select to MATCH High	—	10	—	12	—	15	—	20	ns
tDAM	Data Input to MATCH Valid	—	10	—	13	—	16	—	22	ns
tOEMHI	$\overline{OE}$ Low to MATCH High	—	10	—	12	—	15	—	20	ns
tWEMHI	$\overline{WE}$ Low to MATCH High	—	10	—	12	—	15	—	20	ns
tRSMHI	$\overline{RESET}$ Low to MATCH High	—	12	—	15	—	18	—	25	ns
tMHA	MATCH Valid Hold From Address	2	—	2	—	2	—	2	—	ns
tMHD	MATCH Valid Hold From Data	2	—	2	—	2	—	2	—	ns

NOTE:
1. 0° to +70°C temperature range only.
2. -55°C to +125°C temperature range only.

3001 tbl 12

MATCH TIMING[1]



3001 drw 12

NOTE:
1. It is not recommended to float data and address input pins while the MATCH pin is active.

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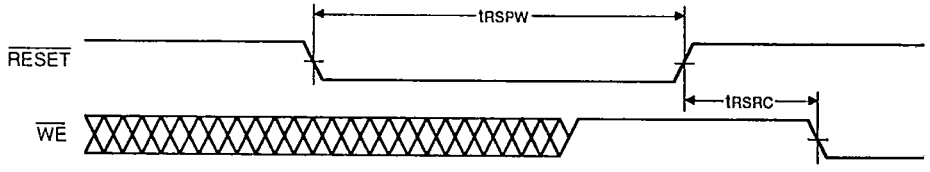
AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges) T-46-23-12

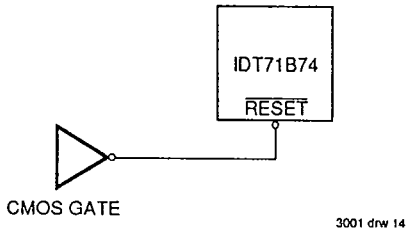
Symbol	Parameter	71B74S12[1] Min.	71B74S12[1] Max.	717B4S15 Min.	717B4S15 Max.	71B74S18 Min.	71B74S18 Max.	71B74S25[2] Min.	71B74S25[2] Max.	Unit
Read Cycle										
tRSPW	Reset Pulse Width[2]	25	—	30	—	35	—	45	—	ns
tRSRC	Reset High to $\overline{WE}$ Low	3	—	3	—	5	—	5	—	ns

NOTES: 3001 tbl 13
1. 0° to +70°C temperature range only.
2. Recommended duty cycle = 10% maximum.
3. -55°C to +125°C temperature range only.

RESET TIMING

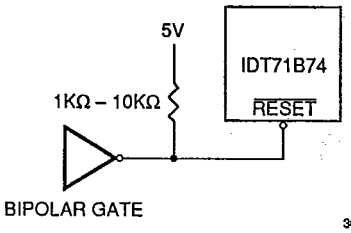


3001 drw 13



3001 drw 14

Driving the $\overline{RESET}$ pin with CMOS logic.

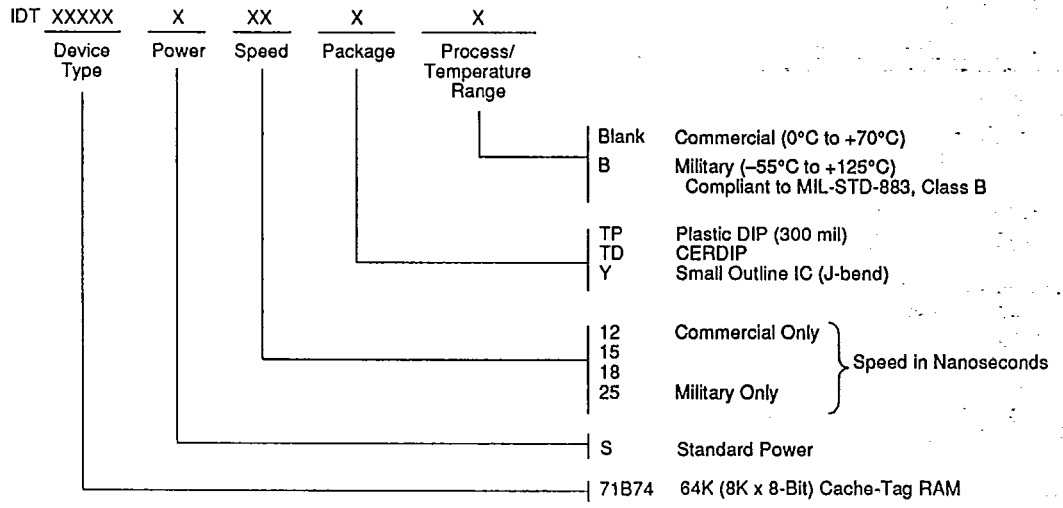


3001 drw 15

Driving the $\overline{RESET}$ pin with bipolar logic.

Figure 5.

ORDERING INFORMATION



3001 drw 16

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