36Mb QDR™ SRAM 4-WORD BURST

MT54V2MH18E
MT54V1MH36E

Features

- Separate independent read and write data ports with concurrent transactions
- 100 percent bus utilization DDR READ and WRITE operation
- High-frequency operation with future migration to higher clock frequencies
- Fast clock to valid data times
- Full data coherency, providing most current data
- Four-tick burst counter for reduced address frequency
- Double data rate operation on read and write ports
- Two input clocks (K and K#) for precise DDR timing at clock rising edges only
- Two output clocks (C and C#) for precise flight time and clock skew matching—clock and data delivered together to receiving device
- Echo clock outputs
- Single address bus
- Simple control logic for easy depth expansion
- Internally self-timed, registered writes
- 2.5V core and 1.5V to 1.8V (±0.1V) HSTL I/O
- Clock-stop capability
- 15mm x 17mm, 1mm pitch, 11 x 15 grid FBGA package
- User-programmable impedance outputs
- JTAG boundary scan

Options

Options	Marking[1]
• Clock Cycle Timing	
5ns (200 MHz)	-5
6ns (167 MHz)	-6
7.5ns (133 MHz)	-7.5
10ns (100 MHz)	-10
• Configurations	
2 Meg x 18	MT54V2MH18E
1 Meg x 36	MT54V1MH36E
• Operating Temperature Range	
Commercial (0°C ≤ T_A ≤ 70°C)	
• Package	
165-ball, 15mm x 17mm FBGA	F

NOTE:

1. A Part Marking Guide for FBGA devices can be found on Micron's Web site—*http://www.micron.com/numberguide*

Figure 1: 165-Ball FBGA

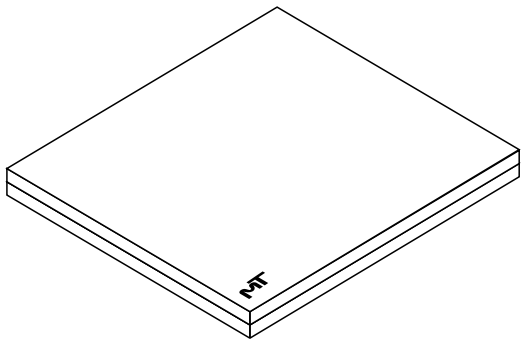


Table 1: Valid Part Numbers

PART NUMBER	DESCRIPTION
MT54V2MH18EF-xx	2 Meg x 18, QDRb4 FBGA
MT54V1MH36EF-xx	1 Meg x 36, QDRb4 FBGA

General Description

The Micron® QDR® (Quad Data Rate™) Synchronous Pipelined Burst SRAM employs high-speed, low-power CMOS designs using an advanced 6T CMOS process.

The QDR architecture consists of two separate DDR (double data rate) ports to access the memory array. The read port has dedicated data outputs to support READ operations. The write port has dedicated data inputs to support WRITE operations. This architecture eliminates the need for high-speed bus turnaround. Access to each port is accomplished using a common address bus. Addresses for reads and writes are latched on alternate rising edges of the K input clock. Each address location is associated with four 18-bit words that burst sequentially into or out of the device. Since data can be transferred into and out of the device on every rising edge of both clocks (K and K#, C and C#) memory bandwidth is maximized while simplifying system design by eliminating bus turnarounds. Asyn-

chronous inputs include impedance match (ZQ). Synchronous data outputs (Q) are closely matched to the two echo clocks (CQ and CQ#) which can be used as data receive clocks.

Depth expansion is accomplished with port selects for each port (read R#, write W#) which are received at K rising edge. Port selects permit independent port operation. All synchronous inputs pass through registers controlled by the K or K# input clock rising edges. Active LOW byte writes (BW0#, BW1#) permit byte write selection. Write data and byte writes are registered on the rising edges of both K and K#. The addressing within each burst of four is fixed and sequential. All synchronous data outputs pass through output registers controlled by the rising edges of the output clocks (C and C# if provided, otherwise K and K#).

Four balls are used to implement JTAG test capabilities: test mode select (TMS), test data-in (TDI), test clock (TCK), and test data-out (TDO). JTAG circuitry is used to serially shift data to and from the SRAM. JTAG inputs use JEDEC-standard 2.5V I/O levels to shift data during this testing mode of operation.

The SRAM operates from a 2.5V power supply, and all inputs and outputs are HSTL-compatible. The device is ideally suited for applications that benefit from a high-speed fully-utilized DDR data bus.

Please refer to Micron's Web site (www.micron.com/sramds) for the latest data sheet.

READ/WRITE Operations

All bus transactions operate on an uninterruptable burst of four data, requiring two full clock cycles of bus utilization. Any request that attempts to interrupt a burst in progress is ignored. The resulting benefit is that the address rate is kept down to the clock frequency even when both buses are 100 percent utilized.

READ cycles are pipelined. The request is initiated by asserting R# LOW at K rising edge. Data is delivered after the next rising edge of K using C and C# as the output timing references, or using K and K#, if C and C# are tied HIGH. If C and C# are tied HIGH, they may not be toggled during device operation. Output tri-stating is automatically controlled such that the bus is released if no data is being delivered. This permits banked SRAM systems with no complex output enable (OE) timing generation. Back-to-back READ cycles are initiated every second K rising edge. Any READ command in between is ignored, since the burst sequence may not be interrupted and requires two full clock cycles.

WRITE cycles are initiated by W# LOW at K rising edge. Data is expected at both rising edges of K andK# beginning one clock period later. Write registers are incorporated to facilitate pipelined self-timed WRITE cycles and provide fully coherent data for all combinations of READs and WRITEs. A READ can immediately follow a WRITE even if they are to the same address. Although the WRITE data has not been written to the memory array, the SRAM will deliver the data from the write register instead of using the older data from the memory array. The latest data is always utilized for all bus transactions. WRITE cycles are initiated every second K rising edge. Any WRITE command in between is ignored, since the burst sequence may not be interrupted.

BYTE WRITE Operations

BYTE WRITE operations are supported. The active LOW byte write controls, BW0# and BW1#, are registered coincident with their corresponding data. This feature can eliminate the need for some READ-MODIFY-WRITE cycles, collapsing it to a single BYTE WRITE operation in some instances.

Programmable Impedance Output Buffer

The QDR SRAM is equipped with programmable impedance output buffers. This allows a user to match the driver impedance to the system. To adjust the impedance, an external precision resistor (RQ) is connected between the ZQ ball and VSS. The value of the resistor must be five times the desired impedance. For example, a 350Ω resistor is required for an output impedance of 70Ω. To ensure that output impedance is one fifth the value of RQ (within 15 percent), the range of RQ is 175Ω to 350Ω. Alternately, the ZQ ball can be connected directly to VDDQ, which will place the device in a minimum impedance mode.

Output impedance updates may be required because variations may occur in supply voltage and temperature over time. The device samples the value of RQ. Impedance updates are transparent to the system; they do not affect device operation, and all data sheet timing and current specifications are met during an update.

The device will power up with an output impedance set at 50Ω. To guarantee optimum output driver impedance after power-up, the SRAM needs 1,024 cycles to update the impedance. The user can operate the part with fewer than 1,024 clock cycles, but optimal output impedance is not guaranteed.

Clock Considerations

The device does not utilize internal phase-locked loops and can therefore be placed into a stopped-clock state to minimize power without lengthy restart times. It is strongly recommended that the clocks operate for a number of cycles prior to initiating commands to the SRAM. This delay permits transmission line charging effects to be overcome and allows the clock timing to be nearer to its steady-state value.

The echo clocks (CQ and CQ#) provide another alternate for data synchronization. The echo clocks are controlled exactly like the DQ signals except that CQ and CQ# have an additional small delay for easier data capture by the bus master. Echo clocks must be separately received for each SRAM in the system. Use of echo clocks maximizes the available data window for each SRAM in the system.

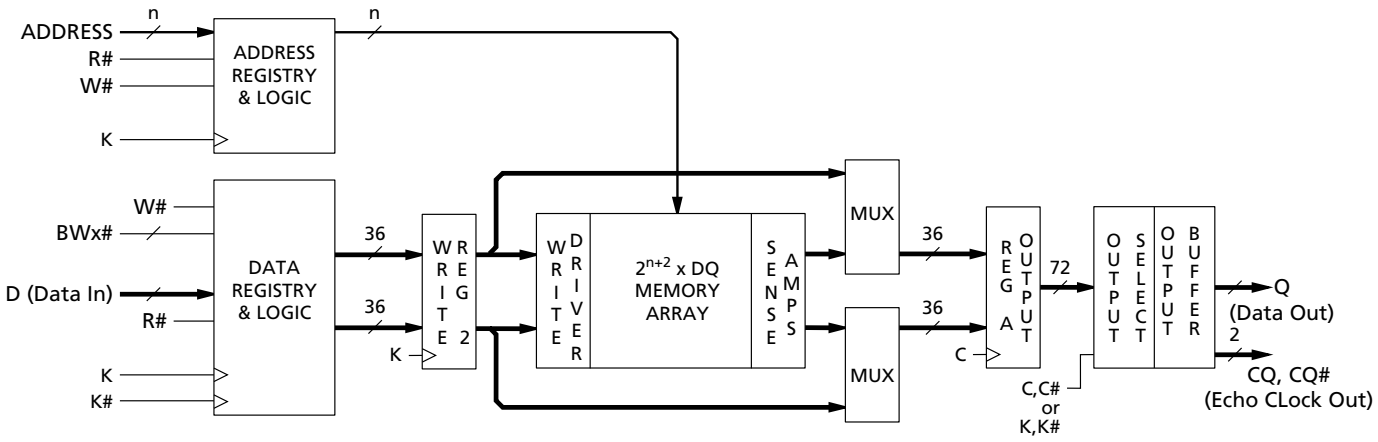
Single Clock Mode

The SRAM can be used with the single K, K# clock pair by tying C and C# HIGH. In this mode, the SRAM will use K and K# in place of C and C#. This mode provides the most rapid data output but does not compensate for system clock skew and flight times.

Depth Expansion

Port select inputs are provided for the read and write ports. This allows for easy depth expansion. Both port selects are sampled on the rising edge of K only. Each port can be independently selected and deselected and do not affect the operation of the opposite port. All pending transactions are completed prior to a port deselecting.

Figure 2: Functional Block Diagram
2 Meg x 18; 1 Meg x 36



NOTE:

1. Figure 2 illustrates simplified device operation. See truth tables, ball descriptions, and timing diagrams for detailed information.
2. For 2 Meg x 18, n = 19; D = 18, Q = 18; DQ = 18; BWx# = 2 separate byte writes.
   For 1 Meg x 36, n = 18; D = 36, Q = 36; DQ = 36; BWx# = 4 separate byte writes.

Figure 3: Application Example

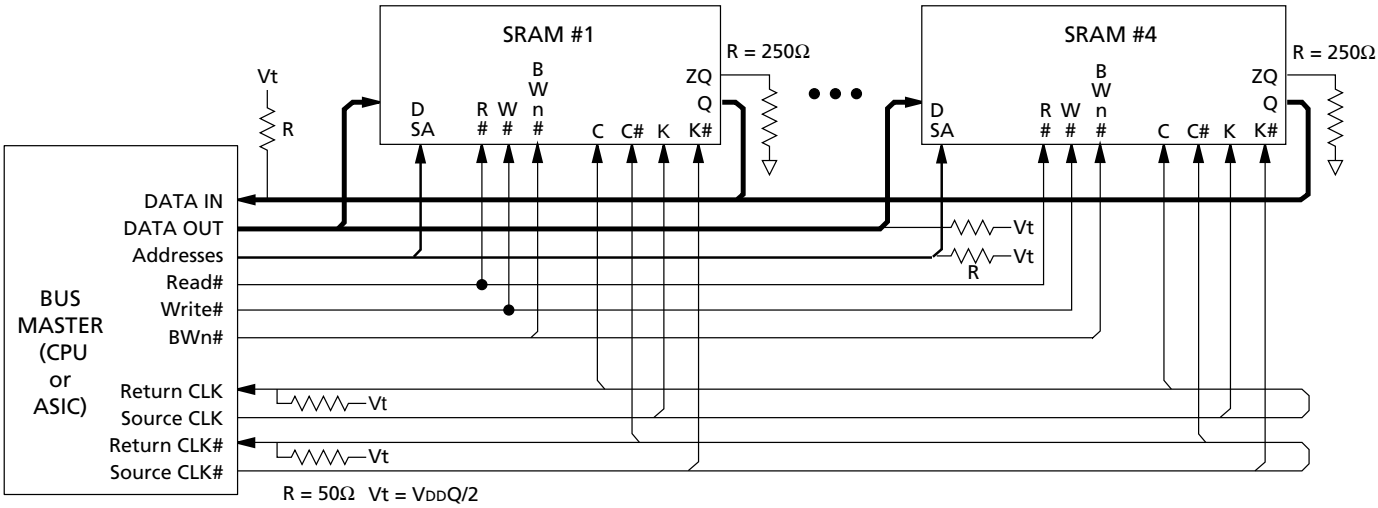


Table 2: 2 Meg x 18 Ball Assignment (Top View) 165-Ball FBGA

	1	2	3	4	5	6	7	8	9	10	11
A	CQ#	VSS	SA	W#	BW1#	K#	NC	R#	SA	VSS	CQ
B	NC	Q9	D9	SA	NC	K	BW0#	SA	NC	NC	Q8
C	NC	NC	D10	VSS	SA	NC	SA	VSS	NC	Q7	D8
D	NC	D11	Q10	VSS	VSS	VSS	VSS	VSS	NC	NC	D7
E	NC	NC	Q11	VDDQ	VSS	VSS	VSS	VDDQ	NC	D6	Q6
F	NC	Q12	D12	VDDQ	VDD	VSS	VDD	VDDQ	NC	NC	Q5
G	NC	D13	Q13	VDDQ	VDD	VSS	VDD	VDDQ	NC	NC	D5
H	NC	VREF	VDDQ	VDDQ	VDD	VSS	VDD	VDDQ	VDDQ	VREF	ZQ
J	NC	NC	D14	VDDQ	VDD	VSS	VDD	VDDQ	NC	Q4	D4
K	NC	NC	Q14	VDDQ	VDD	VSS	VDD	VDDQ	NC	D3	Q3
L	NC	Q15	D15	VDDQ	VSS	VSS	VSS	VDDQ	NC	NC	Q2
M	NC	NC	D16	VSS	VSS	VSS	VSS	VSS	NC	Q1	D2
N	NC	D17	Q16	VSS	SA	SA	SA	VSS	NC	NC	D1
P	NC	NC	Q17	SA	SA	C	SA	SA	NC	D0	Q0
R	TDO	TCK	SA	SA	SA	C#	SA	SA	SA	TMS	TDI

Table 3: 1 Meg x 36 Ball Assignment (Top View) 165-Ball FBGA

	1	2	3	4	5	6	7	8	9	10	11
A	CQ	VSS	NC	W#	BW2#[1]	K#	BW1#[2]	R#	SA	VSS	CQ
B	Q27	Q18	D18	SA	BW3#[3]	K	BW0#[4]	SA	D17	Q17	Q8
C	D27	Q28	D19	VSS	SA	NC	SA	VSS	D16	Q7	D8
D	D28	D20	Q19	VSS	VSS	VSS	VSS	VSS	Q16	D15	D7
E	Q29	D29	Q20	VDDQ	VSS	VSS	VSS	VDDQ	Q15	D6	Q6
F	Q30	Q21	D21	VDDQ	VDD	VSS	VDD	VDDQ	D14	Q14	Q5
G	D30	D22	Q22	VDDQ	VDD	VSS	VDD	VDDQ	Q13	D13	D5
H	NC	VREF	VDDQ	VDDQ	VDD	VSS	VDD	VDDQ	VDDQ	VREF	ZQ
J	D31	Q31	D23	VDDQ	VDD	VSS	VDD	VDDQ	D12	Q4	D4
K	Q32	D32	Q23	VDDQ	VDD	VSS	VDD	VDDQ	Q12	D3	Q3
L	Q33	Q24	D24	VDDQ	VSS	VSS	VSS	VDDQ	D11	Q11	Q2
M	D33	Q34	D25	VSS	VSS	VSS	VSS	VSS	D10	Q1	D2
N	D34	D26	Q25	VSS	SA	SA	SA	VSS	Q10	D9	D1
P	Q35	D35	Q26	SA	SA	C	SA	SA	Q9	D0	Q0
R	TDO	TCK	SA	SA	SA	C#	SA	SA	SA	TMS	TDI

NOTE:

1. BW2# controls writes to D18:D26
2. BW1# controls writes to D9:D17
3. BW3# controls writes to D27:D35
4. BW0# controls writes to D0:D8

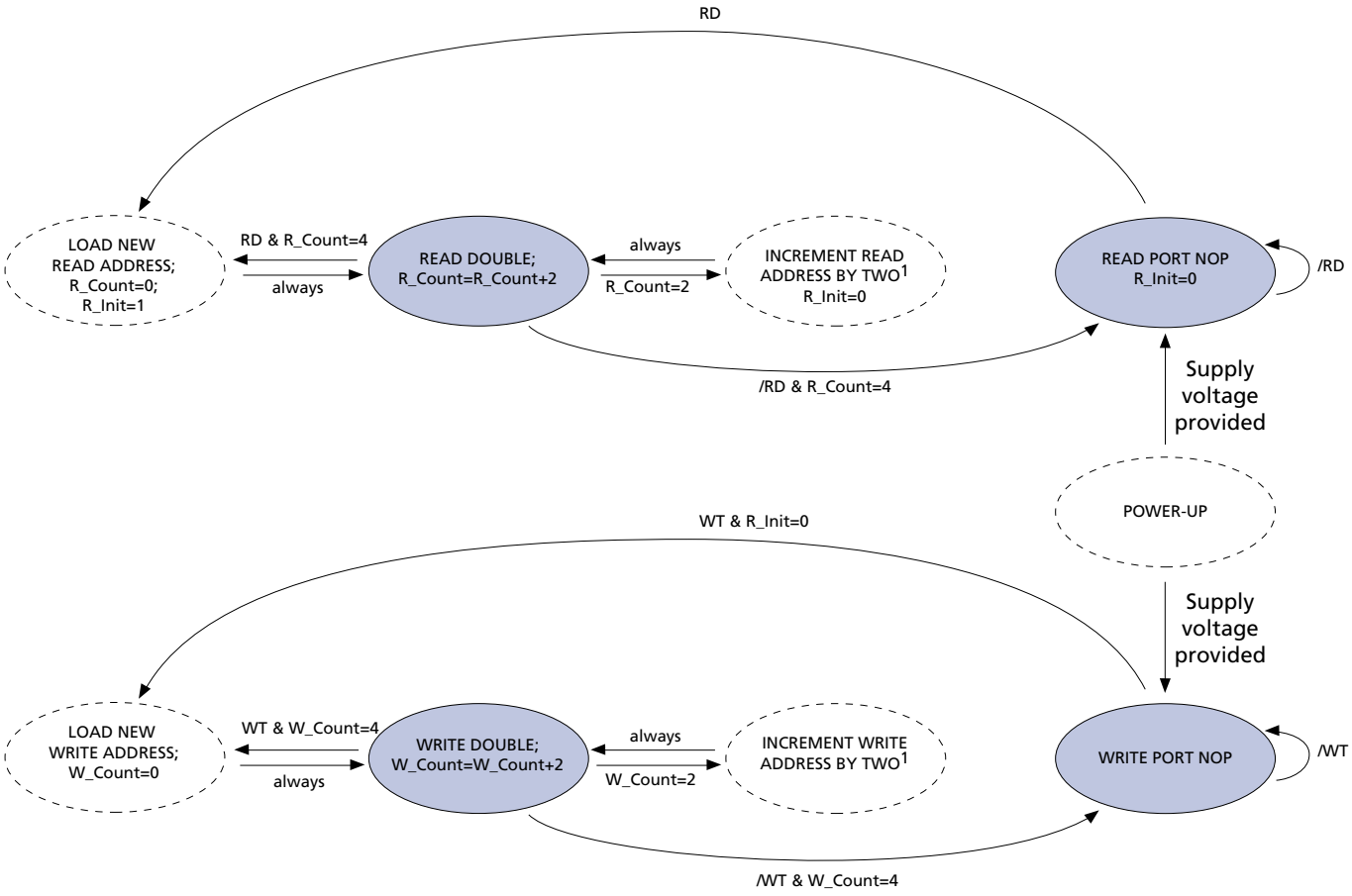
Table 4: Ball Descriptions

SYMBOL	TYPE	DESCRIPTION
BW_#	Input	Synchronous Byte Writes: When LOW, these inputs cause their respective bytes to be registered and written if W# had initiated a WRITE cycle. These signals must meet setup and hold times around the rising edges of K and K# for each of the four rising edges comprising the WRITE cycle. See Ball Assignment figures for signal to data relationships.
C C#	Input	Output Clock: This clock pair provides a user-controlled means of tuning device output data. The rising edge of C is used as the output timing reference for first and third output data. The rising edge of C# is used as the output reference for second and fourth output data. Ideally, C# is 180 degrees out of phase with C. C and C# may be tied HIGH to force the use of K and K# as the output reference clocks instead of having to provide C and C# clocks. If tied HIGH, these inputs may not be allowed to toggle during device operation.
D_	Input	Synchronous Data Inputs: Input data must meet setup and hold times around the rising edges of K and K# during WRITE operations. See Ball Assignment figures for ball site location of individual signals. The x18 device uses D0:D17, and the x36 device uses D0:D5.
K K#	Input	Input Clock: This input clock pair registers address and control inputs on the rising edge of K, and registers data on the rising edge of K and the rising edge of K#. K# is ideally 180 degrees out of phase with K. All synchronous inputs must meet setup and hold times around the clock rising edges.
R#	Input	Synchronous Read: When LOW, this input causes the address inputs to be registered and a READ cycle to be initiated. This input must meet setup and hold times around the rising edge of K and is ignored on the subsequent rising edge of K.
SA	Input	Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of K. All transactions operate on a burst of four data (two clock periods of bus activity). These inputs are ignored when both ports are deselected.
TCK	Input	IEEE 1149.1 Clock Input: 2.5V I/O levels. This ball must be tied to VSS if the JTAG function is not used in the circuit.
TMS TDI	Input	IEEE 1149.1 Test Inputs: 2.5V I/O levels. These balls may be left as No Connects if the JTAG function is not used in the circuit.
VREF	Input	HSTL Input Reference Voltage: Nominally VDDQ/2, but may be adjusted to improve system noise margin. Provides a reference voltage for the HSTL input buffer trip point.
W#	Input	Synchronous Write: When LOW, this input causes the address inputs to be registered and a WRITE cycle to be initiated. This input must meet setup and hold times around the rising edge of K and is ignored on the subsequent rising edge of K. This input is also ignored if a READ cycle is being initiated.
ZQ	Input	Output Impedance Matching Input: This input is used to tune the device outputs to the system data bus impedance. DQ output impedance is set to 0.2 x RQ, where RQ is a resistor from this ball to ground. Alternately, this ball can be connected directly to VDDQ, which enables the minimum impedance mode. This ball cannot be connected directly to GND or left unconnected.
CQ, CQ#	Output	Echo Clocks: The edges of these outputs are tightly matched to the synchronous data outputs and can be used as data valid indication. These signals run freely and do not stop when Q tri-states.
DNU	Output	Do Not Use: These balls should not be used.
Q_	Output	Synchronous Data Outputs: Output data is synchronized to the respective C and C# or to K and K# rising edges if C and C# are tied HIGH. This bus operates in response to R# commands. See Ball Assignment figures for ball site location of individual signals. The x18 device uses Q0:Q17, and the x36 device uses Q0:Q35.
TDO	Output	IEEE 1149.1 Test Output: JEDEC-standard 2.5V I/O level.
VDD	Supply	Power Supply: 2.5V nominal. See DC Electrical Characteristics and Operating Conditions for range.
VDDQ	Supply	Power Supply: Isolated Output Buffer Supply. Nominally 1.5V. See DC Electrical Characteristics and Operating Conditions for range.

Table 4: Ball Descriptions (Continued)

SYMBOL	TYPE	DESCRIPTION
VSS	Supply	Power Supply: GND.
NC	–	No Connect: These signals are internally connected and may be connected to ground to improve package heat dissipation.

Figure 4:
Bus Cycle State Diagram



NOTE:

1. The address is concatenated with 2 additional internal LSBs to facilitate BURST operation. The address order is always fixed as: xxx...xxx+0, xxx...xxx+1, xxx...xxx+2, xxx...xxx+3. Bus cycle is terminated at the end of this sequence (burst count = 4).
2. State transitions: RD = (R# = LOW); WT = (W# = LOW).
3. Read and write state machines can be simultaneously active . Read and write cannot be initiated simultaneously; read takes precedence.
4. State machine control timing sequence is controlled by K.

Table 5: Truth Table

Notes 1-8

OPERATION	K	R#	W#	D or Q	D or Q	D or Q	D or Q
WRITE Cycle: Load address, input write data on two consecutive K and K# rising edges	L→H	H[7]	L[8]	$D_A(A_0 + 0)$ at $K(t_0 + 0)\uparrow$	$D_A(A_0 + 1)$ at $K\#(t_0 + 1)\uparrow$	$D_A(A_0 + 2)$ at $K(t_0 + 2)\uparrow$	$D_A(A_0 + 3)$ at $K\#(t_0 + 3)\uparrow$
READ Cycle: Load address, output data on two consecutive C and C# rising edges	L→H	L[8]	X	$Q_A(A_0 + 0)$ at $C(t_0 + 0)\uparrow$	$Q_A(A_0 + 1)$ at $C\#(t_0 + 1)\uparrow$	$Q_A(A_0 + 2)$ at $C(t_0 + 2)\uparrow$	$Q_A(A_0 + 3)$ at $C\#(t_0 + 3)\uparrow$
NOP: No operation	L→H	H	H	D = X Q = High-Z	D = X Q = High-Z	D = X Q = High-Z	D = X Q = High-Z
STANDBY: Clock stopped	Stopped	X	X	Previous State	Previous State	Previous State	Previous State

Table 6: BYTE WRITE Operation

Note 9, 10

OPERATION	K	K#	BW0#	BW1#
WRITE D0-17 at K rising edge	L→H		0	0
WRITE D0-17 at K# rising edge		L→H	0	0
WRITE D0-8 at K rising edge	L→H		0	1
WRITE D0-8 at K# rising edge		L→H	0	1
WRITE D9-17 at K rising edge	L→H		1	0
WRITE D9-17 at K# rising edge		L→H	1	0
WRITE nothing at K rising edge	L→H		1	1
WRITE nothing at K# rising edge		L→H	1	1

NOTE:

1. X means "Don't Care." H means logic HIGH. L means logic LOW. ↑ means rising edge; ↓ means falling edge.
2. Data inputs are registered at K and K# rising edges. Data outputs are delivered at C and C# rising edges, except if C and C# are HIGH, then data outputs are delivered at K and K# rising edges.
3. R# and W# must meet setup and hold times around the rising edge (LOW to HIGH) of K and are registered at the rising edge of K.
4. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.
5. Refer to state diagram and timing diagrams for clarification. A_0 refers to the address input during a WRITE or READ cycle. $A_0 + 1$ refers to the next internal burst address in accordance with the burst sequence.
6. It is recommended that K = /K# = C =/C# when clock is stopped. This is not essential, but permits most rapid restart by overcoming transmission line charging symmetrically.
7. If this signal was LOW to initiate the previous cycle, this signal becomes a "Don't Care" for this operation; however, it is strongly recommended that this signal is brought HIGH as shown in the Truth Table.
8. This signal was HIGH on previous K clock rising edge. Initiating consecutive READ or WRITE operations on consecutive K clock rising edges is not permitted. The device will ignore the second request.
9. Assumes a WRITE cycle was initiated. BW0# and BW1# can be altered for any portion of the BURST WRITE operation provided that the setup and hold requirements are satisfied.
10. This table illustrates operation for the x18 devices. The x36 operation is similar except for the addition of BW2# (controls D18:D26) and BW3# (controls D27:D35).

Absolute Maximum Ratings

Voltage on VDD Supply
Relative to VSS ..... 0.5V to +3.4V
Voltage on VDDQ Supply
Relative to VSS ..... -0.5V to VDD
VIN ..... -0.5V to VDD +0.5V
Storage Temperature .....-55ºC to +125ºC
Junction Temperature ..... +125ºC
Short Circuit Output Current ..... ±70mA

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Maximum Junction Temperature depends upon package type, cycle time, loading, ambient temperature, and airflow. See Micron Technical Note TN-05-14 for more information.

Table 7: DC Electrical Characteristics and Operating Conditions

Notes appear following parameter tables on page 15; 0°C ≤ T_A ≤ +70°C; VDD = 2.5V ±0.1V unless otherwise noted

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		VIH(DC)	VREF + 0.1	VDDQ + 0.3	V	3, 4
Input Low (Logic 0) Voltage		VIL(DC)	-0.3	VREF - 0.1	V	3, 4
Clock Input Signal Voltage		VIN	-0.3	VDDQ + 0.3	V	3, 4
Input Leakage Current	0V ≤ VIN ≤ VDDQ	ILI	-5	5	µA	
Output Leakage Current	Output(s) disabled, 0V ≤ VIN ≤ VDDQ (Q)	ILO	-5	5	µA	
Output High Voltage	|IOH| ≤ 0.1mA	VOH (LOW)	VDDQ - 0.2	VDDQ	V	3, 5, 6
	Note 1	VOH	VDDQ/2 - 0.12	VDDQ/2 + 0.12	V	3, 5, 6
Output Low Voltage	IOL ≤ 0.1mA	VOL (LOW)	VSS	0.2	V	3, 5, 6
	Note 2	VOL	VDDQ/2 - 0.12	VDDQ/2 + 0.12	V	3, 5, 6
Supply Voltage		VDD	2.4	2.6	V	3
Isolated Output Buffer Supply		VDDQ	1.4	1.6	V	3
Reference Voltage		VREF	0.68	0.95	V	3

Table 8: AC Electrical Characteristics and Operating Conditions

Notes appear following parameter tables on page 15; 0°C ≤ T_A ≤ +70°C; VDD = 2.5V ±0.1V unless otherwise noted

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		VIH(AC)	VREF + 0.2	–	V	3, 4, 7
Input Low (Logic 0) Voltage		VIL(AC)	–	VREF - 0.2	V	3, 4, 7

Table 9: IDD Operating Conditions and Maximum Limits

Notes appear following parameter tables on page 15; 0°C ≤ T_A ≤ +70°C; VDD = 2.5V ±0.1V unless otherwise noted

				MAX					
DESCRIPTION	**CONDITIONS**	**SYM**	**TYP**	**-5**	**-6**	**-7.5**	**-10**	**UNITS**	**NOTES**
Operating Supply Current: DDR	All inputs ≤ VIL or ≥ VIH; Cycle time ≥ tKHKH (MIN); Outputs open; 100% bus utilization; 50% address and data bits toggling on each clock cycle	IDD x18 x36	TBD	 300 410	 250 350	 230 300	 200 260	mA	8, 9
Standby Supply Current: NOP	tKHKH = tKHKH (MIN); Device in NOP state; All addresses/data static	ISB1 x18 x36	TBD	 170 180	 145 155	 125 135	 110 120	mA	9, 10
Stop Clock Current	Cycle time = 0; Input Static	ISB	TBD	75	75	75	75	mA	9
Output Supply Current: DDR (Information only)	CL = 15pF	IDDQ x18 x36	TBD	 25 57	 21 47	 17 38	 13 29	mA	11

Table 10: Capacitance

Note 12; notes appear following parameter tables on page 15

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS
Address/Control Input Capacitance	T_A = 25°C; f = 1 MHz	CI	4	5	pF
Output Capacitance (D, Q)		CO	6	7	pF
Clock Capacitance		CCK	5	6	pF

Table 11: Thermal Resistance

Note 12; notes appear following parameter tables on page 15

DESCRIPTION	CONDITIONS	SYMBOL	TYP	UNITS	NOTES
Junction to Ambient (Airflow of 1m/s)	Soldered on a 4.25 x 1.125 inch, 4-layer, printed circuit board	θ_{JA}	25	°C/W	13
Junction to Case (Top)		θ_{JC}	10	°C/W	
Junction to Balls (Bottom)		θ_{JB}	12	°C/W	14

Table 12: AC Electrical Characteristics and Recommended Operating Conditions

Notes 15-17; notes appear following parameter tables; 0°C ≤ T_A ≤ +70°C; T_J ≤ +95°C; VDD = 2.5V ±1.5V

DESCRIPTION	SYM	-5		-6		-7.5		-10		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Clock											
Clock cycle time (K, K#, C, C#)	^tKHKH	5.0		6.0		7.5		10		ns	
Clock HIGH time (K, K#, C, C#)	^tKHKL	2.0		2.4		3.0		3.5		ns	
Clock LOW time (K, K#, C, C#)	^tKLKH	2.0		2.4		3.0		3.5		ns	
Clock to clock# (K↑→K#↑, C↑→C#↑)	$^tKHK\#H$	2.4		2.7		3.4		4.6		ns	
Clock# to clock (K#↑→K↑, C#↑→C↑)	$^tK\#HKH$	2.4		2.7		3.4		4.6		ns	
Clock to data clock (K↑→C↑, K#↑→C#↑)	^tKHCH	0.0	1.5	0.0	2.0	0.0	2.5	0.0	3.0	ns	
Output Times											
C, C# HIGH to output valid	^tCHQV		2.2		2.5		3.0		3.0	ns	
C, C# HIGH to output hold	^tCHQX	1.2		1.2		1.2		1.2		ns	
C HIGH to output High-Z	^tCHQZ		2.2		2.5		3.0		3.0	ns	12, 18
C HIGH to output Low-Z	$^tCHQX1$	1.2		1.2		1.2		1.2		ns	18
C, C# HIGH to CQ, CQ# HIGH	^tCHCQH	1.2	2.3	1.2	2.6	1.2	3.2	1.2	3.2	ns	17
CQ, CQ# HIGH to output valid	^tCQHQV		0.35		0.40		0.45		0.50	ns	
CQ, CQ# HIGH to output hold	^tCQHQX	-0.35		-0.40		-0.45		-0.50		ns	
CQ HIGH to output High-Z	^tCQHQZ		0.35		0.40		0.45		0.50	ns	12, 18
CQ HIGH to output Low-Z	$^tCQHQX1$	0.35		-0.40		-0.45		-0.50		ns	18
Setup Times											
Address valid to K rising edge	^tAVKH	0.6		0.7		0.8		1.0		ns	19
Control inputs valid to K rising edge	^tIVKH	0.6		0.7		0.8		1.0		ns	19
Data-in valid to K, K# rising edge	^tDVKH	0.6		0.7		0.8		1.0		ns	19
Hold Times											
K rising edge to address hold	^tKHAX	0.6		0.7		0.8		1.0		ns	19
K rising edge to control inputs hold	^tKHIX	0.6		0.7		0.8		1.0		ns	19

Table 12: AC Electrical Characteristics and Recommended Operating Conditions

Notes 15-17; notes appear following parameter tables; 0°C ≤ T_A ≤ +70°C; T_J ≤ +95°C; VDD = 2.5V ±1.5V

DESCRIPTION	SYM	-5		-6		-7.5		-10		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
K, K# rising edge to data-in hold	^{t}KHDX	0.6		0.7		0.8		1.0		ns	19

Notes

1. Outputs are impedance-controlled. |IOH| = (VDDQ/2)/(RQ/5) for values of 175Ω ≤ RQ ≤ 350Ω.
2. Outputs are impedance-controlled. IOL = (VDDQ/2)/(RQ/5) for values of 175Ω ≤ RQ ≤ 350Ω.
3. All voltages referenced to VSS (GND).
4. Overshoot: VIH(AC) ≤ VDD + 0.7V for t ≤ ^{t}KHKH/2
   Undershoot: VIL(AC) ≥ -0.5V for t ≤ ^{t}KHKH/2
   Power-up: VIH ≤ VDDQ + 0.3V and VDD ≤ 2.4V and VDDQ ≤ 1.4V for t ≤ 200ms
   During normal operation, VDDQ must not exceed VDD. R#, W#, and address signals may not have pulse widths less than ^{t}KHKL (MIN) or operate at cycle rates less than ^{t}KHKH (MIN).
5. AC load current is higher than the shown DC values. AC I/O curves are available upon request.
6. HSTL outputs meet JEDEC HSTL Class I and Class II standards.
7. To maintain a valid level, the transitioning edge of the input must:
   a. Sustain a constant slew rate from the current AC level through the target AC level, VIL(AC) or VIH(AC)
   b. Reach at least the target AC level
   c. After the AC target level is reached, continue to maintain at least the target DC level, VIL(DC) or VIH(DC)
8. IDD is specified with no output current and increases with faster cycle times. IDDQ increases with faster cycle times and greater output loading. Typical value is measured at 6ns cycle time.
9. Typical values are measured at VDD =2.5V, VDDQ = 1.5V, and temperature = 25°C.
10. NOP currents are valid when entering NOP after all pending READ and WRITE cycles are completed.
11. Average I/O current and power is provided for informational purposes only and is not tested. Calculation assumes that all outputs are loaded with CL (in farads), f = input clock frequency, half of outputs toggle at each transition (for example, n = 18 for x36), CO = 6pF, VDDQ = 1.5V and uses the equations: Average I/O Power as dissipated by the SRAM is:
    $P = 0.5 \times n \times f \times V_{DDQ}^2 \times (C_L + 2C_O)$. Average IDDQ = n x f x VDDQ x (CL + CO).
12. This parameter is sampled.
13. Average thermal resistance between the die and the case top surface per MIL SPEC 883 Method 1012.1.
14. Junction temperature is a function of total device power dissipation and device mounting environment. Measured per SEMI G38-87.
15. Control input signals may not be operated with pulse widths less than ^{t}KHKL (MIN).
16. Test conditions as specified with the output loading as shown in Figure 5, unless otherwise noted.
17. If C, C# are tied HIGH, then K, K# become the references for C, C# timing parameters.
18. ^{t}CHQXI is greater than ^{t}CHQZ at any given voltage and temperature.
19. This is a synchronous device. All addresses, data, and control lines must meet the specified setup and hold times for all latching clock edges.

AC Test Conditions

Input pulse levels	0.25V to 1.25V
Input rise and fall times	0.7ns
Input timing reference levels	0.75V
Output reference levels	VDDQ/2
ZQ for 50Ω impedance	250Ω
Output load	See Figure 5

Figure 5:
Output Load Equivalent

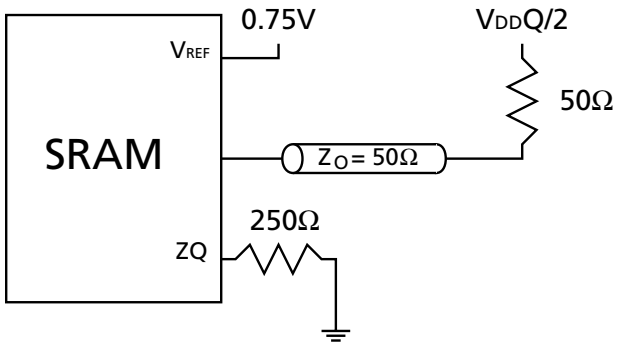
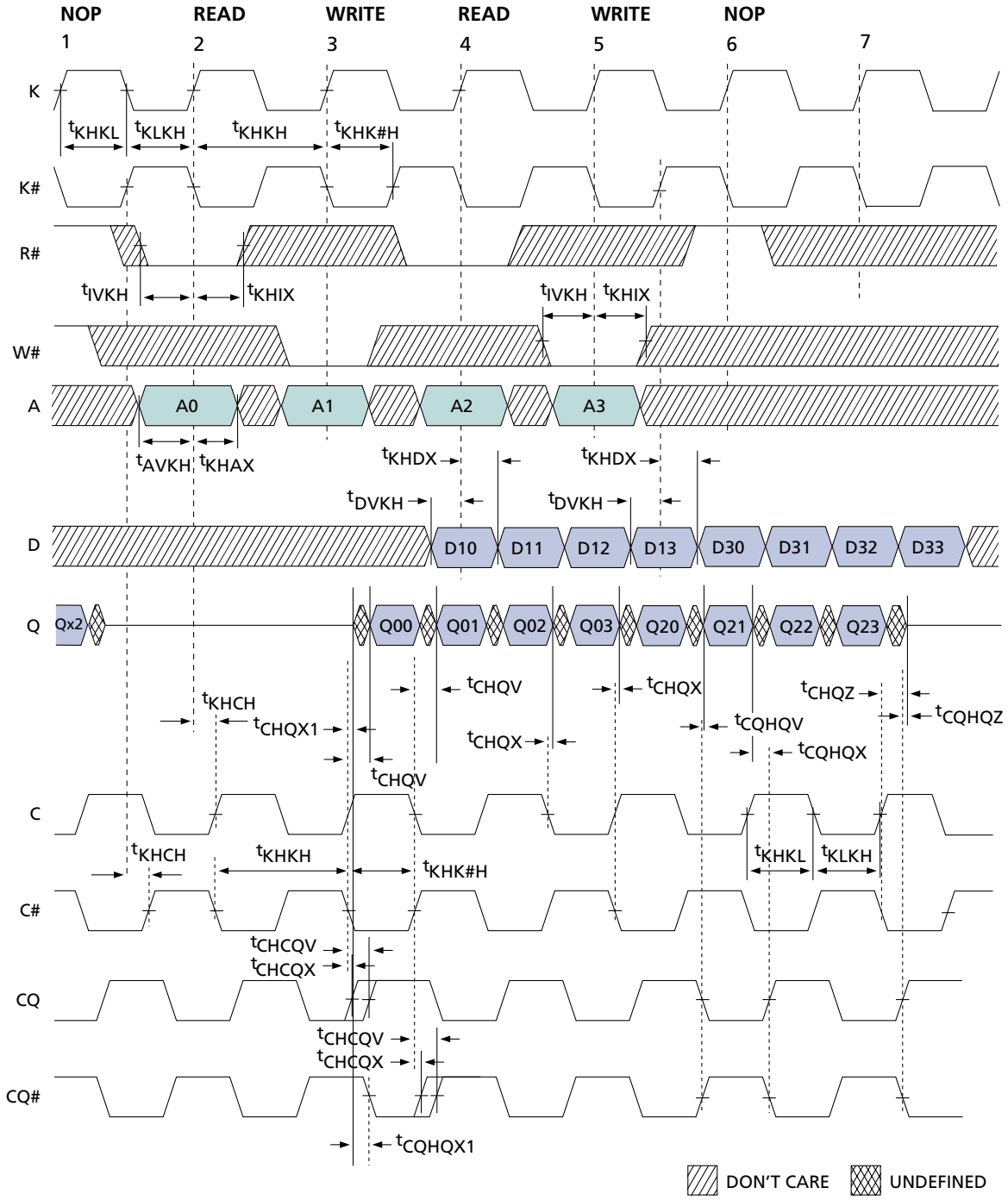


Figure 6:
READ/WRITE Timing



NOTE:

1. Q00 refers to output from address A0 + 0. Q01 refers to output from the next internal burst address following A_0, i.e., A_0 + 1, etc.
2. Outputs are disabled (High-Z) one clock cycle after a NOP.
3. In this example, if address A2 = A1, then data Q20 = D10, Q21 = D11, Q22 = D12, and Q23 = D13. Write data is forwarded immediately as read results.

IEEE 1149.1 SERIAL BOUNDARY SCAN (JTAG)

The SRAM incorporates a serial boundary scan test access port (TAP). This port operates in accordance with IEEE Standard 1149.1. The TAP operates using JEDEC-standard 2.5V I/O logic levels.

The SRAM contains a TAP controller, instruction register, boundary scan register, bypass register, and ID register.

Disabling the JTAG Feature

It is possible to operate the SRAM without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW (Vss) to prevent clocking of the device. TDI and TMS are internally pulled up and may be unconnected. They may alternately be connected to VDD through a pull-up resistor. TDO should be left unconnected. Upon power-up, the device will come up in a reset state which will not interfere with the operation of the device.

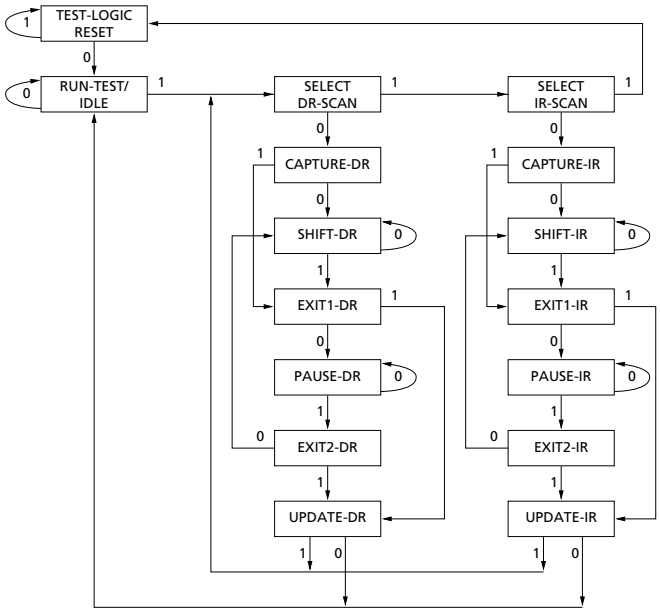
Test Access Port (TAP) Test Clock (TCK)

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

Test Mode Select (TMS)

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. It is allowable to leave this ball unconnected if the TAP is not used. The ball is pulled up internally, resulting in a logic HIGH level.

Figure 7:
TAP Controller State Diagram



NOTE:

The 0/1 next to each state represents the value of TMS at the rising edge of TCK.

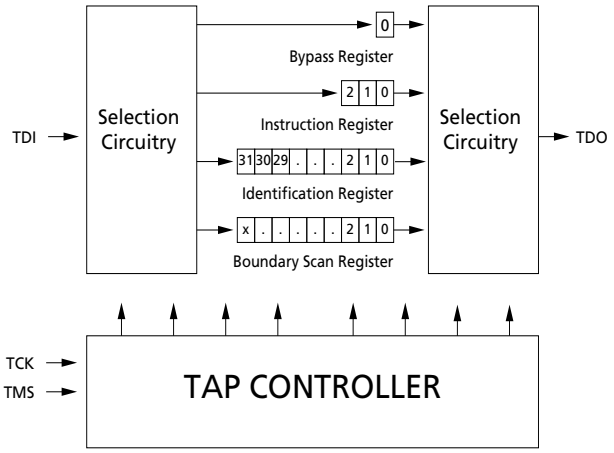
Test Data-In (TDI)

The TDI ball is used to serially input information into the registers and can be connected to the input of any of the registers. The register between the TDI and TDO balls is chosen by the instruction that is loaded into the TAP instruction register. For information on loading the instruction register, see Figure 7. TDI is internally pulled up and can be unconnected if the TAP is unused in an application. TDI is connected to the most-significant bit (MSB) of any register, as shown in Figure 8.

Test Data-Out (TDO)

The TDO output ball is used to serially clock data-out from the registers. The output is active depending upon the current state of the TAP state machine, as depicted in Figure 7. The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register, illustrated in Figure 8.

Figure 8:
TAP Controller Block Diagram



NOTE:

X = 108 for both configurations.

Performing a TAP RESET

A RESET is performed by forcing TMS HIGH (Vdd) for five rising edges of TCK. This RESET does not affect the operation of the SRAM and may be performed while the SRAM is operating.

At power-up, the TAP is reset internally to ensure that TDO comes up in a High-Z state.

TAP Registers

Registers are connected between the TDI and TDO balls and allow data to be scanned into and out of the SRAM test circuitry. Only one register can be selected at a time through the instruction register. Data is serially loaded into the TDI ball on the rising edge of TCK. Data is output on the TDO ball on the falling edge of TCK.

Instruction Register

Three-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO balls as shown in Figure 8. Upon power-up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as described in the previous section.

When the TAP controller is in the Capture-IR state, the two LSBs are loaded with a binary "01" pattern to allow for fault isolation of the board-level serial test data path.

Bypass Register

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain chips. The bypass register is a single-bit register that can be placed between the TDI and TDO balls. This allows data to be shifted through the SRAM with minimal delay. The bypass register is set LOW (Vss) when the BYPASS instruction is executed.

Boundary Scan Register

The boundary scan register is connected to all the input and bidirectional balls on the SRAM. Several no connect (NC) balls are also included in the scan register to reserve balls. The SRAM has a 109-bit-long register.

The boundary scan register is loaded with the contents of the RAM I/O ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO balls when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD, and SAMPLE Z instructions can be used to capture the contents of the I/O ring.

The Boundary Scan Order tables show the order in which the bits are connected. Each bit corresponds to one of the balls on the SRAM package. The MSB of the register is connected to TDI, and the LSB is connected to TDO.

Identification (ID) Register

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in the Identification Register Definitions table.

TAP Instruction Set Overview

Eight different instructions are possible with the three-bit instruction register. All combinations are listed in the Instruction Codes table. Three of these instructions are listed as RESERVED and should not be used. The other five instructions are described in detail below.

The TAP controller used in this SRAM is fully compliant to the 1149.1 convention.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state,

instructions are shifted through the instruction register and through the TDI and TDO balls. To execute the instruction once it is shifted in, the TAP controller needs to be moved into the Update-IR state.

EXTEST

The EXTEST instruction allows circuitry external to the component package to be tested. Boundary scan register cells at output balls are used to apply test vectors, while those at input balls capture test results. Typically, the first test vector to be applied using the EXTEST instruction will be shifted into the boundary scan register using the PRELOAD instruction. Thus, during the Update-IR state of EXTEST, the output drive is turned on and the PRELOAD data is driven onto the output balls.

IDCODE

The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the instruction register. It also places the instruction register between the TDI and TDO pins/balls and allows the IDCODE to be shifted out of the device when the TAP controller enters the Shift-DR state. The IDCODE instruction is loaded into the instruction register upon power-up or whenever the TAP controller is given a test logic reset state.

SAMPLE Z

The SAMPLE Z instruction causes the boundary scan register to be connected between the TDI and TDO balls when the TAP controller is in a Shift-DR state. It also places all SRAM outputs into a High-Z state.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is a 1149.1 mandatory instruction.

When the SAMPLE/PRELOAD instruction is loaded into the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the inputs and bi-directional balls is captured in the boundary scan register.

Once the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO balls.

The user must be aware that the TAP controller clock can only operate at a frequency up to 10 MHz, while the SRAM clock operates more than an order of magnitude faster. Because there is a large difference in the clock frequencies, it is possible that during the Capture-DR state, an input or output will undergo a transition. The TAP may then try to capture a signal while in transition (metastable state). This will not harm the device, but there is no guarantee as to the value that will be captured. Repeatable results may not be possible.

To guarantee that the boundary scan register will capture the correct value of a signal, the SRAM signal must be stabilized long enough to meet the TAP controller's capture setup plus hold time (tCS plus tCH). The SRAM clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the CK and CK# captured in the boundary scan register.

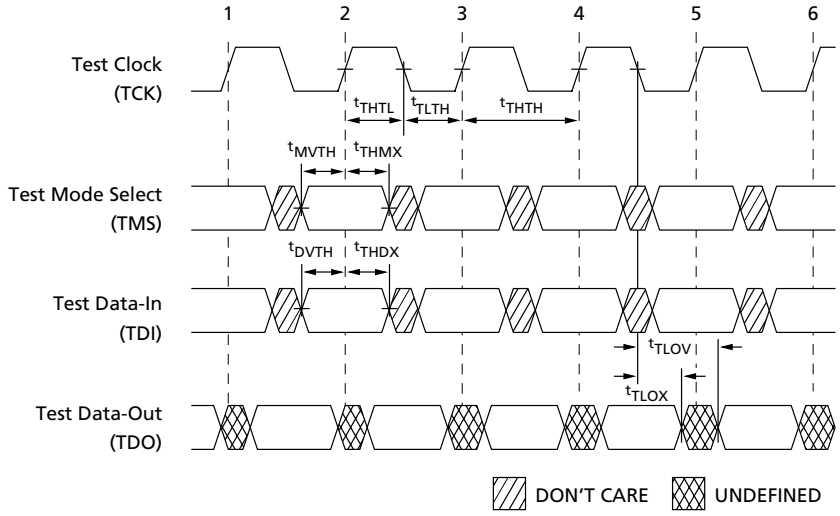
BYPASS

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between TDI and TDO. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

RESERVED

These instructions are not implemented but are reserved for future use. Do not use these instructions.

Figure 9: TAP Timing



NOTE:

Timing for SRAM inputs and outputs is congruent with TDI and TDO, respectively, as shown in Figure 9.

Table 13: TAP DC Electrical Characteristics

Notes 1, 2; 0°C ≤ T_A ≤ +70°C; VDD = 2.5V ±0.1V

DESCRIPTION	SYMBOL	MIN	MAX	UNITS
Clock				
Clock cycle time	^{t}THTH	100		ns
Clock frequency	^{f}TF		10	MHz
Clock HIGH time	^{t}THTL	40		ns
Clock LOW time	^{t}TLTH	40		ns
Output Times				
TCK LOW to TDO unknown	^{t}TLOX	0		ns
TCK LOW to TDO valid	^{t}TLOV		20	ns
TDI valid to TCK HIGH	^{t}DVTH	10		ns
TCK HIGH to TDI invalid	^{t}THDX	10		ns
Setup Times				
TMS setup	^{t}MVTH	10		ns
Capture setup	^{t}CS	10		ns
Hold Times				
TMS hold	^{t}THMX	10		ns
Capture hold	^{t}CH	10		ns

NOTE:

1. ^{t}CS and ^{t}CH refer to the setup and hold time requirements of latching data from the boundary scan register.
2. Test conditions are specified using the load in Figure 10.

TAP AC Test Conditions

Input pulse levels . . . . . VSS to 2.5V
Input rise and fall times 1ns
Input timing reference levels 1.25V
Output reference levels 1.25V
Test load termination supply voltage 1.25V

Figure 10:
TAP AC Output Load Equivalent

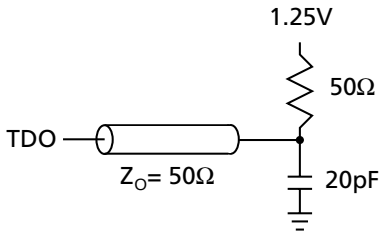


Table 14: TAP DC Electrical Characteristics and Operating Conditions

Note 3; 0°C ≤ T_A ≤ +70°C; VDD = 2.5V ±0.1V unless otherwise noted

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		VIH	1.7	VDD + 0.3	V	1, 2
Input Low (Logic 0) Voltage		VIL	-0.3	0.7	V	1, 2
Input Leakage Current	0V ≤ VIN ≤ VDD	ILI	-5.0	5.0	µA	
Output Leakage Current	Output(s) disabled, 0V ≤ VIN ≤ VDD	ILO	-5.0	5.0	µA	
Output Low Voltage	IOLC = 100µA	VOL1		0.2	V	
Output Low Voltage	IOLT = 2mA	VOL2		0.7	V	1
Output High Voltage	IOHC = -100µA	VOH1	2.1		V	1
Output High Voltage	IOHT = -2mA	VOH1	1.7		V	1

NOTE:

1. All voltages referenced to VSS (GND).
2. Overshoot: VIH(AC) ≤ VDD + 0.7V for t ≤ ^{t}KHKH/2
   Undershoot: VIL(AC) ≥ -0.5V for t ≤ ^{t}KHKH/2
   Power-up: VIH ≤ +2.6 and VDD ≤ +2.4V and VDDQ ≤ 1.4V for t ≤ 200ms
   During normal operation, VDDQ must not exceed VDD. Control input signals (R#, W#, etc.) may not have pulse widths less than ^{t}KHKL (MIN) or operate at frequencies exceeding ^{f}KF (MAX).
3. This table defines DC values for TAP control and data balls only. The DQ SRAM balls used in the JTAG operation will have the same values as defined in Table 7, "DC Electrical Characteristics and Operating Conditions," on page 11.

Table 15: Identification Register Definitions

INSTRUCTION FIELD	ALL DEVICES	DESCRIPTION
REVISION NUMBER (31:28)	000	Revision number.
DEVICE ID (28:12)	00def0wx0t0q0b0s0	def = 000 for 9Mb density def = 001 for 18Mb density def = 010 for 36Mb density wx = 11 for x36 width wx = 10 for x18 width t = 1 for DLL version t = 0 for non-DLL version q = 1 for QDR q = 0 for DDR b = 1 for 4-word burst b = 0 for 2-word burst s = 1 for separate I/O s = 0 for common I/O
MICRON JEDEC ID CODE (11:1)	00000101100	Allows unique identification of SRAM vendor.
ID Register Presence Indicator (0)	1	Indicates the presence of an ID register.

Table 16: Scan Register Sizes

REGISTER NAME	BIT SIZE
Instruction	3
Bypass	1
ID	32
Boundary Scan	109

Table 17: Instruction Codes

INSTRUCTION	CODE	DESCRIPTION
EXTEST	000	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. This operation does not affect SRAM operations.
IDCODE	001	Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operations.
SAMPLE Z	010	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all SRAM output drivers to a High-Z state.
RESERVED	011	Do Not Use: This instruction is reserved for future use.
SAMPLE/PRELOAD	100	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Does not affect SRAM operations.
RESERVED	101	Do Not Use: This instruction is reserved for future use.
RESERVED	110	Do Not Use: This instruction is reserved for future use.
BYPASS	111	Places the bypass register between TDI and TDO. This operation does not affect SRAM operations.

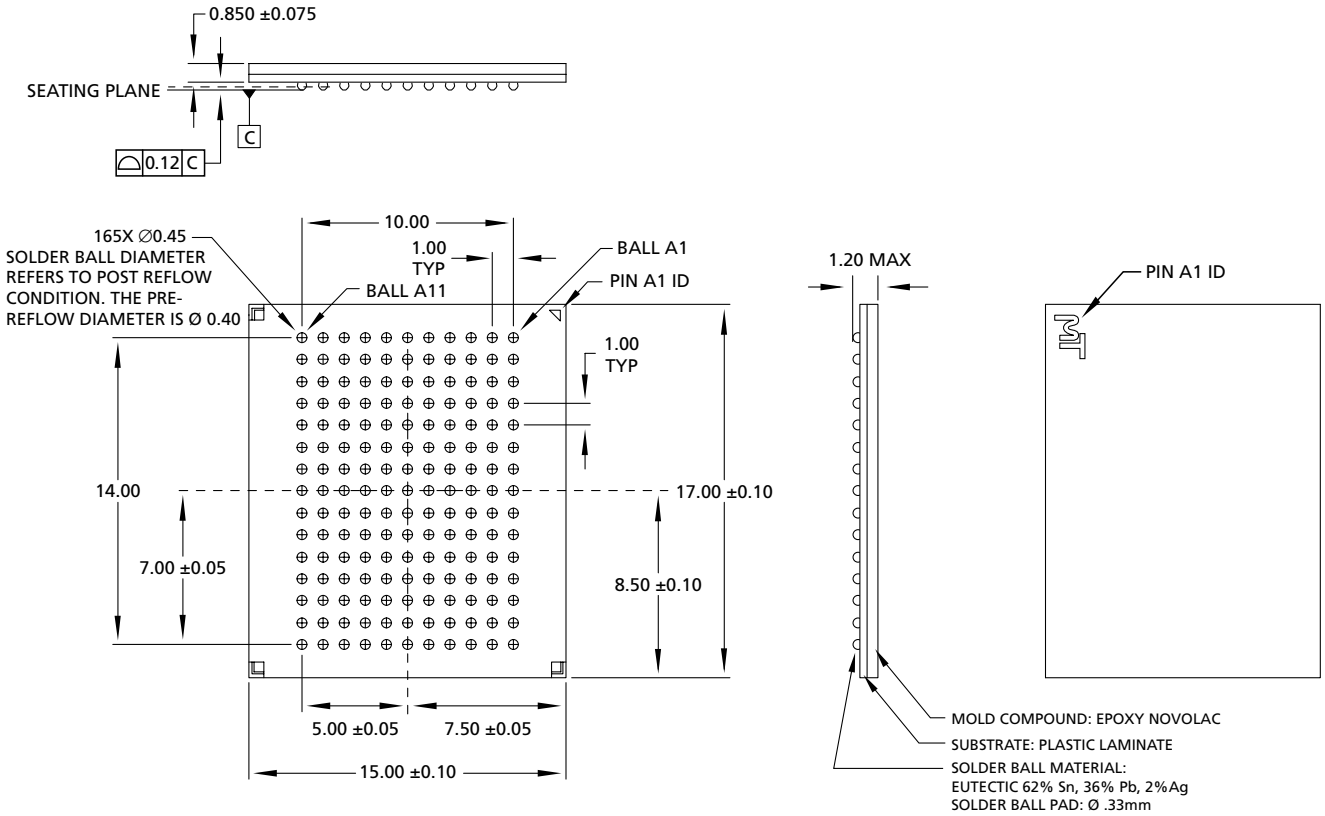
Table 18: Boundary Scan (Exit) Order

BIT#	FBGA BALL
1	6R
2	6P
3	6N
4	7P
5	7N
6	7R
7	8R
8	8P
9	9R
10	11P
11	10P
12	10N
13	9P
14	10M
15	11N
16	9M
17	9N
18	11L
19	11M
20	9L
21	10L
22	11K
23	10K
24	9J
25	9K
26	10J
27	11J
28	11H
29	10G
30	9G
31	11F
32	11G
33	9F
34	10F
35	11E
36	10E

BIT#	FBGA BALL
37	10D
38	9E
39	10C
40	11D
41	9C
42	9D
43	11B
44	11C
45	9B
46	10B
47	11A
48	10A
49	9A
50	8B
51	7C
52	6C
53	8A
54	7A
55	7B
56	6B
57	6A
58	5B
59	5A
60	4A
61	5C
62	4B
63	3A
64	2A
65	1A
66	2B
67	3B
68	1C
69	1B
70	3D
71	3C
72	1D

BIT#	FBGA BALL
73	2C
74	3E
75	2D
76	2E
77	1E
78	2F
79	3F
80	1G
81	1F
82	3G
83	2G
84	1H
85	1J
86	2J
87	3K
88	3J
89	2K
90	1K
91	2L
92	3L
93	1M
94	1L
95	3N
96	3M
97	1N
98	2M
99	3P
100	2N
101	2P
102	1P
103	3R
104	4R
105	4P
106	5P
107	5N
108	5R
109	INTERNAL

Figure 11:
165-Ball FBGA



NOTE:

1. All dimensions are in millimeters.

DATA SHEET DESIGNATION

Advance: This data sheet contains initial descriptions of products still under development.

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Revision History

- New ADVANCE data sheet for die revison A; Rev. A, Pub. 1 /03 ..... 1/03