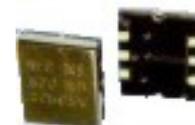


- Frequency range 38MHz to 640MHz
- LVDS Output
- Supply Voltage 3.3 VDC
- Phase jitter 0.4ps typical
- Pull range from $\pm 30\text{ppm}$ to $\pm 150\text{ppm}$



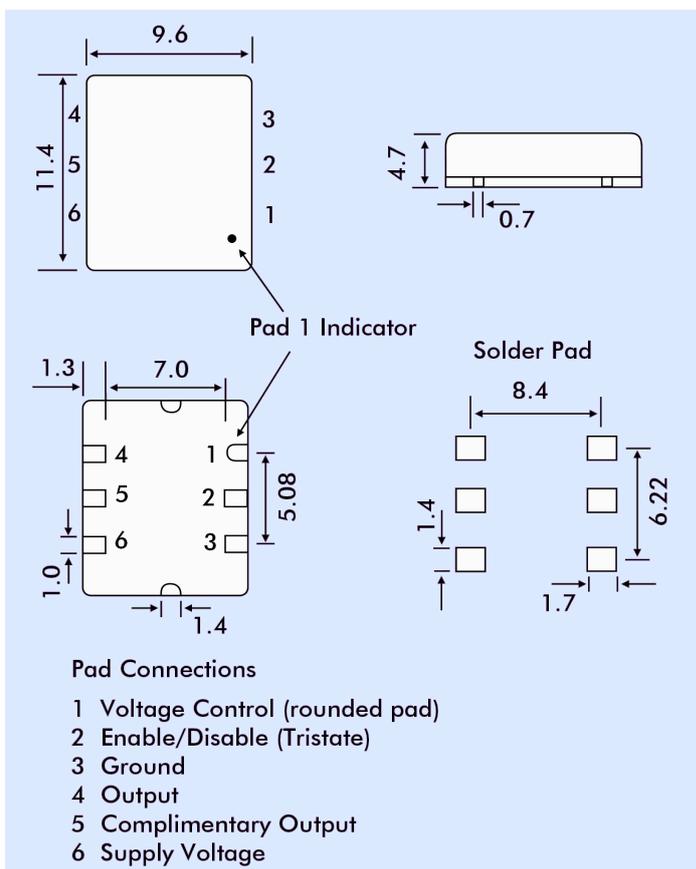
DESCRIPTION

GDF64 VCXOs are packaged in a 6 pad 11.4 x 9.6mm SMD package. Typical phase jitter for GDF series VCXOs is 0.4 ps. Output is LVDS. Applications include phase lock loop, SONET/ATM, set-top boxes, MPEG, audio/video modulation, video game consoles and HDTV.

SPECIFICATION

Frequency Range:	38.0MHz to 640.0MHz
Supply Voltage:	3.3 VDC $\pm 5\%$
Output Logic:	LVDS
RMS Period Jitter:	3.0ps typical
Peak to Peak Jitter:	20.0ps typical, 30.0ps maximum
Phase Jitter:	0.4ps typical, 5.0ps maximum
Initial Frequency Accuracy:	Tune to the nominal frequency with $V_c = 1.65 \pm 0.2\text{VDC}$
Output Voltage HIGH (1):	1.4 Volts typical
Output Voltage LOW (0):	1.1 Volts typical
Pulling Range:	From $\pm 30\text{ppm}$ to $\pm 150\text{ppm}$
Control Voltage Range:	1.65 ± 1.35 Volts
Temperature Stability:	See table
Output Load:	50Ω into Vdd or Thevenin equiv.
Rise/Fall Times:	0.5ns typ., 0.7ns max.
Duty Cycle:	20% Vdd to 80% Vdd 50% $\pm 5\%$ (Measured at Vdd-1.3V)
Start-up Time:	10ms maximum, 5ms typical
Current Consumption:	55mA typical, 60mA maximum (At 202.50MHz)
Static Discharge Protection:	2kV maximum
Storage Temperature:	-55° to $+150^\circ\text{C}$
Ageing:	$\pm 2\text{ppm}$ per year maximum
Enable/Disable:	See table
RoHS Status:	Fully compliant or non compliant

OUTLINE & DIMENSIONS



FREQUENCY STABILITY

Stability Code	Stability $\pm\text{ppm}$	Temp. Range
A	25	$0^\circ \sim +70^\circ\text{C}$
B	50	$0^\circ \sim +70^\circ\text{C}$
C	100	$0^\circ \sim +70^\circ\text{C}$
D	25	$-40^\circ \sim +85^\circ\text{C}$
E	50	$-40^\circ \sim +85^\circ\text{C}$
F	100	$-40^\circ \sim +85^\circ\text{C}$

If non-standard frequency stability is required Use 'I' followed by stability, i.e. I20 for $\pm 20\text{ppm}$

ENABLE/DISABLE FUNCTION

Tristate Pad Status	Output Status
Not connected	LVDS and Complimentary LVDS enabled
Below 0.3Vdd (Ref. to ground)	Both outputs are disabled (high impedance)
Above 0.7Vdd (Ref. to ground)	Both outputs are enabled

PART NUMBERING

