4-/8-Channel Wideband Video Multiplexers

Features

- Wide Bandwidth: 500 MHz
- Very Low Crosstalk: −97 dB @ 5 MHz
- On-Board TTL-Compatible Latches with Readback
- Optional Negative Supply
- Low $r_{DS(on)}$: 45 Ω

Benefits

- Improved System Bandwidth
- Improved Channel Off-Isolation
- Simplified Logic Interfacing
- Allows Bipolar Signal Swings
- Reduced Insertion Loss
- Allows Differential Signal Switching

Applications

- Wideband Signal Routing and Multiplexing
- Video Switchers
- ATE Systems
- Infrared Imaging

Description

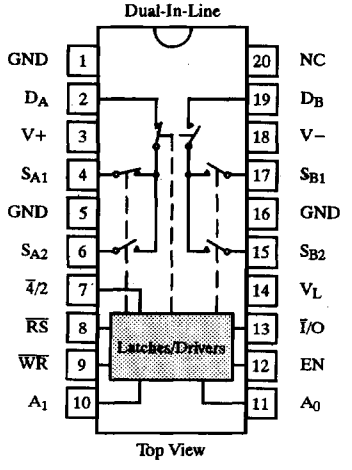
The DG534 is a digitally selectable 4-channel or dual 2-channel multiplexer. The DG538 is an 8-channel or dual 4-channel multiplexer. On-chip TTL-compatible address decoding logic and latches with data readback are included to simplify the interface to a microprocessor data bus. The low on-resistance and low capacitance of the these devices make them ideal for wideband data multiplexing and video and audio signal routing in channel selectors and crosspoint arrays. An optional negative supply pin allows the handling of bipolar signals without dc biasing.

The DG534/DG538 are built on a D/CMOS process that combines n-channel DMOS switching FETs with low-power CMOS control logic, drivers and latches. The low-capacitance DMOS FETs are in a "T" configuration to achieve extremely high levels of off isolation. Crosstalk is reduced to −97 dB at 5 MHz by including a ground line between each adjacent signal path.

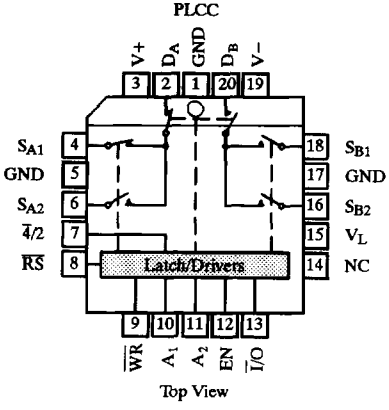
The DG534A/DG538A are recommended for new designs.

Functional Block Diagrams and Pin Configurations

DG534DJ



DG534DN



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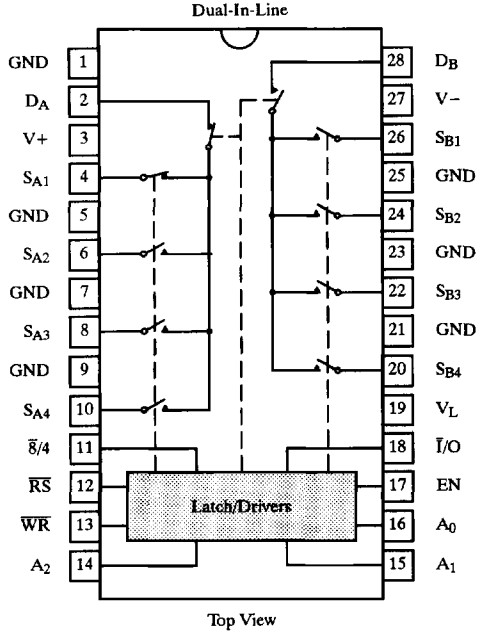
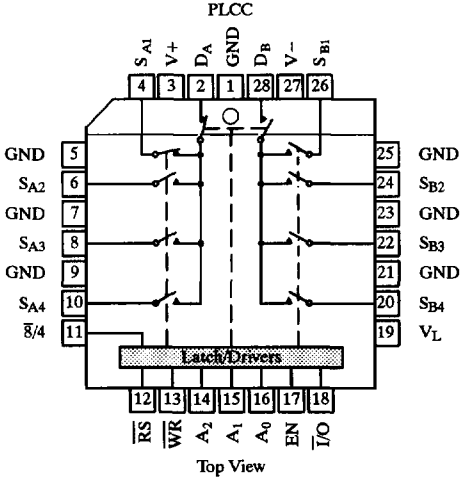
Functional Block Diagrams and Pin Configurations (Cont'd)

DG538DJ



DG538DN



Truth Tables and Ordering Information

Ordering Information – DG534

Temp Range	Package	Part Number
−40 to 85°C	20-Pin Plastic DIP	DG534DJ
	20-Pin PLCC	DG534DN
−55 to 125°C	20-Pin Sidebraze	DG534AP
		DG534AP/883

Truth Table — DG534

I/O	A_1	A_0	EN	WR	RS	4/2[a]	On Switch		
X	X	X	X	↓	1	1	Maintains previous state		
X	X	X	X	X	0	X	None (latches cleared)		
X	X	X	0	0	1	X	None		Latches Transparent
0	0	0	1	0	1	0	S_{A1}	D_A and D_B may be connected externally	
0	0	1	1	0	1	0	S_{A2}		
0	1	0	1	0	1	0	S_{B1}		
0	1	1	1	0	1	0	S_{B2}		
0	X	0	1	0	1	1	S_{A1} and S_{B1}		
0	X	1	1	0	1	1	S_{A2} and S_{B2}		
1	Note b			1	1	Note c			

Logic "0" = $V_{AL} \leq 0.8$ V
Logic "1" = $V_{AH} \geq 2$ V
X = Don't Care

Notes:
a. Connect D_A and D_B together externally for single-ended operation.
b. With I/O high, A_n pin becomes output and reflects latch contents. See timing diagrams for more detail.
c. 4/2 can be either "1" or "0" but should not change during these operations.

Not Recommended for New Designs

Truth Tables and Ordering Information (Cont'd)

Ordering Information – DG538

Temp Range	Package	Part Number
−40 to 85°C	28-Pin Plastic DIP	DG538DJ
	28-Pin PLCC	DG538DN
−55 to 125°C	28-Pin Sidebraze	DG538AP
		DG538AP/883

Truth Table — DG538

$\overline{I}/O$	A_2	A_1	A_0	EN	$\overline{WR}$	$\overline{RS}$	$\overline{8}/4$[a]	On Switch	
X	X	X	X	X	↓	1	1	Maintains previous state	
X	X	X	X	X	X	0	X	None (latches cleared)	
X	X	X	X	0	0	1	X	None	Latches Transparent
0	0	0	0	1	0	1	0	S_{A1}	Latches Transparent
0	0	0	1	1	0	1	0	S_{A2}	Latches Transparent
0	0	1	0	1	0	1	0	S_{A3}	Latches Transparent
0	0	1	1	1	0	1	0	S_{A4}	Latches Transparent
0	1	0	0	1	0	1	0	S_{B1}	Latches Transparent
0	1	0	1	1	0	1	0	S_{B2}	Latches Transparent
0	1	1	0	1	0	1	0	S_{B3}	Latches Transparent
0	1	1	1	1	0	1	0	S_{B4}	Latches Transparent
0	X	0	0	1	0	1	1	S_{A1} and S_{B1}	Latches Transparent
0	X	0	1	1	0	1	1	S_{A2} and S_{B2}	Latches Transparent
0	X	1	0	1	0	1	1	S_{A3} and S_{B3}	Latches Transparent
0	X	1	1	1	0	1	1	S_{A4} and S_{B4}	Latches Transparent
1	Note b				1	1	Note c		

D_A and D_B should be connected externally

Logic "0" = $V_{AL} \leq 0.8$ V
Logic "1" = $V_{AH} \geq 2$ V
X = Don't Care

Notes:
a. Connect D_A and D_B together externally for single-ended operation.
b. With $\overline{I}/O$ high, A_n pin becomes output and reflects latch contents. See timing diagrams for more detail.
c. $\overline{8}/4$ can be either "1" or "0" but should not change during these operations.

Absolute Maximum Ratings

V+ to GND ..... −0.3 V to +21 V
V+ to V− ..... −0.3 V to +21 V
V− to GND ..... −10 V to +0.3 V
V_L ..... 0 V to (V+) + 0.3 V
Digital Inputs ..... (V−) −0.3 V to (V+) + 0.3 V
or 20 mA, whichever occurs first
V_S, V_D ..... (V−) −0.3 V to (V−) + 14 V
or 20 mA, whichever occurs first
Current (any terminal) Continuous ..... 20 mA
Current(S or D) Pulsed l ms 10% Duty ..... 40 mA

Storage Temperature (A Suffix) ..... −65 to 150°C
(D Suffix) ..... −65 to 125°C
Power Dissipation (Package)[a]
Plastic DIP[b] ..... 625 mW
PLCC[c] ..... 450 mW
Sidebraze[d] ..... 1200 mW

Notes:
a. All leads soldered or welded to PC board.
b. Derate 8.3 mW/°C above 75°C.
c. Derate 6 mW/°C above 75°C.
d. Derate 16 mW/°C above 75°C.

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Specifications[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V− = −3 V, V_L = 5 V, $\overline{WR}$ = 0.8 V, $\overline{RS}$, EN = 2 V		Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	A Suffix −55 to 125°C Max[d]	D Suffix −40 to 85°C Min[d]	D Suffix −40 to 85°C Max[d]	Unit
Analog Switch										
Analog Signal Range[g]	V_{ANALOG}	V− = −5 V		Full		−5	8	−5	8	V
Drain-Source On-Resistance	$r_{DS(on)}$	I_S = −10 mA, V_S = 0 V, V_{AIL} = 0.8 V, V_{AIH} = 2 V Sequence Each Switch On		Room	45		90		90	Ω
				Full			120		120	
Resistance Match Between Channels	$\Delta r_{DS(on)}$			Room			9		9	Ω
Source Off Leakage Current	$I_{S(off)}$	V_S = 8 V, V_D = 0 V, EN = 0.8 V		Room	0.05	−5	5	−5	5	nA
				Full		−50	50	−50	50	
Drain Off Leakage Current	$I_{D(off)}$	V_S = 0 V, V_D = 8 V, EN = 0.8 V		Room	0.1	−20	20	−20	20	nA
				Full		−500	500	−100	100	
Drain On Leakage Current	$I_{D(on)}$	V_S = V_D = 8 V		Room	0.1	−20	20	−20	20	nA
				Full		−1000	1000	−200	200	
Digital Control										
Input Voltage High	V_{AIH}			Full		2		2		V
Input Voltage Low	V_{AIL}			Full			0.8		0.8	V
Address Input Current	I_{AI}	V_{AI} = 0 V, or 2 V or 5 V		Room	−0.1	−1	1	−1	1	µA
				Full		−10	10	−10	10	
Address Output Current	I_{AO}	V_{AO} = 2.7 V		Room	−300					µA
		V_{AO} = 0.4 V		Room	300					
Dynamic Characteristics										
On State Input Capacitance[g]	$C_{S(on)}$		PLCC	Room	28		40		40	pF
			DIP	Room	31		45		45	
Off State Input Capacitance[g]	$C_{S(off)}$		PLCC	Room	3		5		4	pF
			DIP	Room	4				5	
Off State Output Capacitance[g]	$C_{D(off)}$		PLCC	Room	6		10		8	pF
			DIP	Room	8				10	
Transition Time	t_{TRANS}			Room	170		300		300	ns
				Full			500		500	
Break-Before-Make Interval	t_{OPEN}			Room	80	50		50		ns
				Full		25		25		
EN, $\overline{WR}$ Turn On Time	t_{ON}			Room	180		300		300	ns
				Full			500		500	
EN, Turn Off Time	t_{OFF}			Room	95		175		175	ns
				Full			300		300	
Charge Injection	Qi			Room	−70					pC
Chip Disabled Crosstalk[f]	$X_{TALK(CD)}$	R_L = 75 Ω, f = 5 MHz EN = 0.8 V	PLCC	Room	−75					dB
			DIP	Room	−65					
Adjacent Input Crosstalk[f]	$X_{TALK(AI)}$	R_{IN} = 10 Ω, R_L = 10 kΩ f = 5 MHz	PLCC	Room	−97					dB
			DIP	Room	−87					
		R_{IN} = 75 Ω, R_L = 75 Ω f = 5 MHz	PLCC	Room	−80					dB
			DIP	Room	−70					

Not Recommended for New Designs

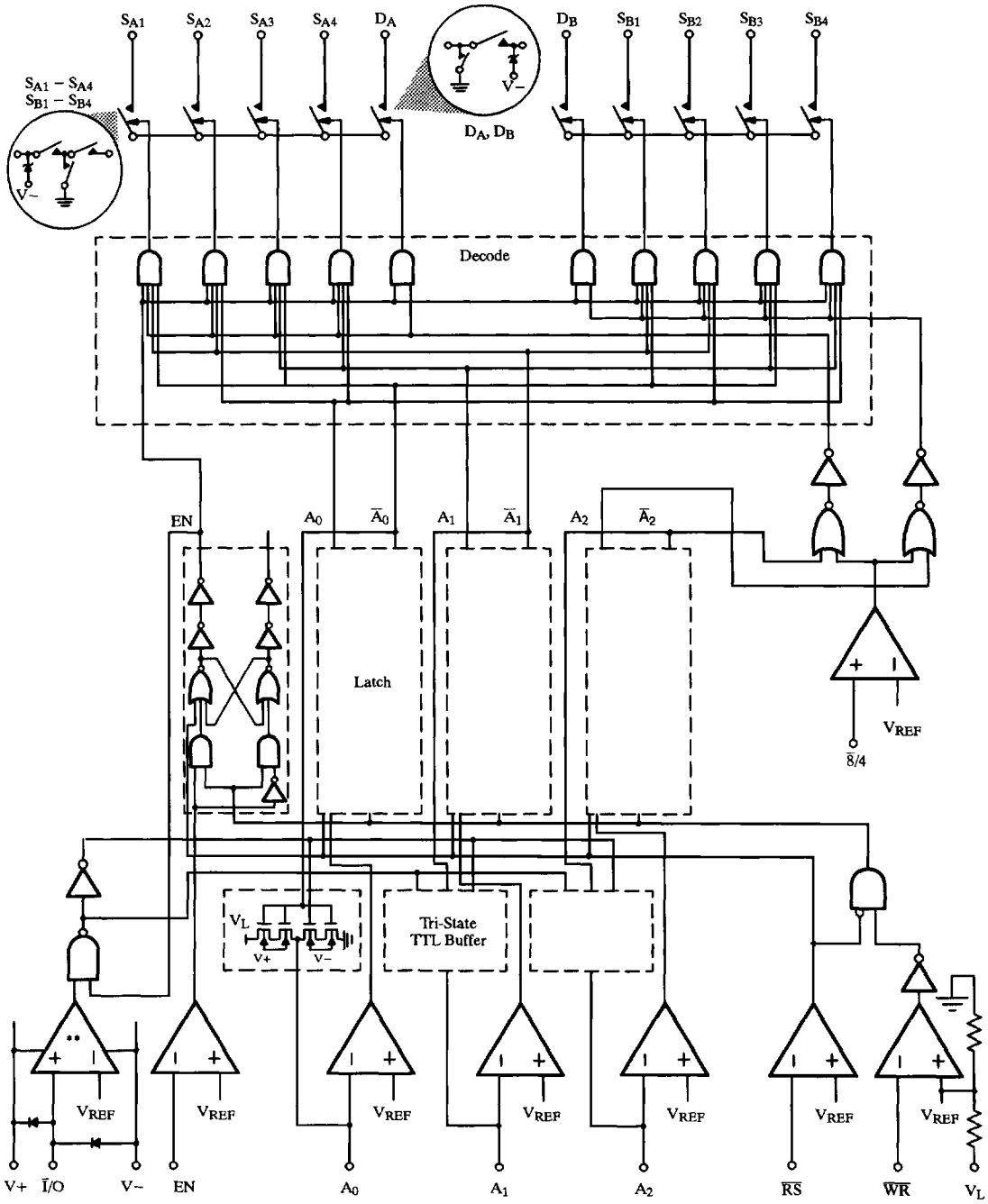
Specifications[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V− = −3 V, V_L = 5 V, $\overline{WR}$ = 0.8 V, $\overline{RS}$, EN = 2 V		Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	A Suffix −55 to 125°C Max[d]	D Suffix −40 to 85°C Min[d]	D Suffix −40 to 85°C Max[d]	Unit
Dynamic Characteristics (Cont'd)										
All Hostile Crosstalk	$X_{TALK(AH)}$	R_{IN} = 10 Ω, R_L = 10 kΩ, f = 5 MHz	PLCC	Room	−77					dB
			DIP	Room	−72					
		R_{IN} = 75 Ω, R_L = 75 Ω, f = 5 MHz	PLCC	Room	−77					
			DIP	Room	−72					
Differential Crosstalk	$X_{TALK(DIFF)}$	R_{IN} = 10 Ω, R_L = 10 kΩ, f = 5 MHz		Room	−84					
		R_{IN} = R_L = 75 Ω, f = 5 MHz		Room	−84					
Bandwidth	BW	R_L = 50 Ω		Room	500					MHz
Power Supplies										
Positive Supply Current	I+	Any One Channel Selected with Address Inputs at GND or V+		Room Full	0.6		2 5		2 5	mA
Negative Supply Current	I−			Room Full	0.6	−1.8 −2		−1.8 −2		
Functional Check of Maximum Operating Supply Voltage Range	V+ to V−	Functional Test Only		Full		10	21	10	21	V
	V− to GND			Full		−5.5	0	−5.5	0	
	V+ to GND			Full		10	21	10	21	
Logic Supply Current	I_L			Full	150		500		500	µA
Timing										
Reset to Write	t_{RW}	See Figure 1		Full		50		50		ns
$\overline{WR}$, $\overline{RS}$ Minimum Pulse Width	t_{MPW}			Full		200		200		
A_0, A_1, EN Data Valid to Strobe	t_{DW}			Full		100		100		
A_0, A_1, EN Data Valid after Strobe	t_{WD}			Full		50		50		
Address Bus Tri-State[e]	t_{AZ}			Room	25					
Address Bus Output	t_{AO}			Room	95					
Address Bus Input	t_{AI}			Room	110					

Notes:
a. Refer to PROCESS OPTION FLOWCHART (Section 5 of the 1994 Data Book or FaxBack number 7103).
b. Room = 25°C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
e. Defined by system bus requirements.
f. Each individual pin shown as GND must be grounded.
g. Guaranteed by design, not subject to production test.

2

Control Circuitry



* Decode section includes delay circuitry in AND gating to ensure proper break-before-make operation.
** Typical all digital inputs.

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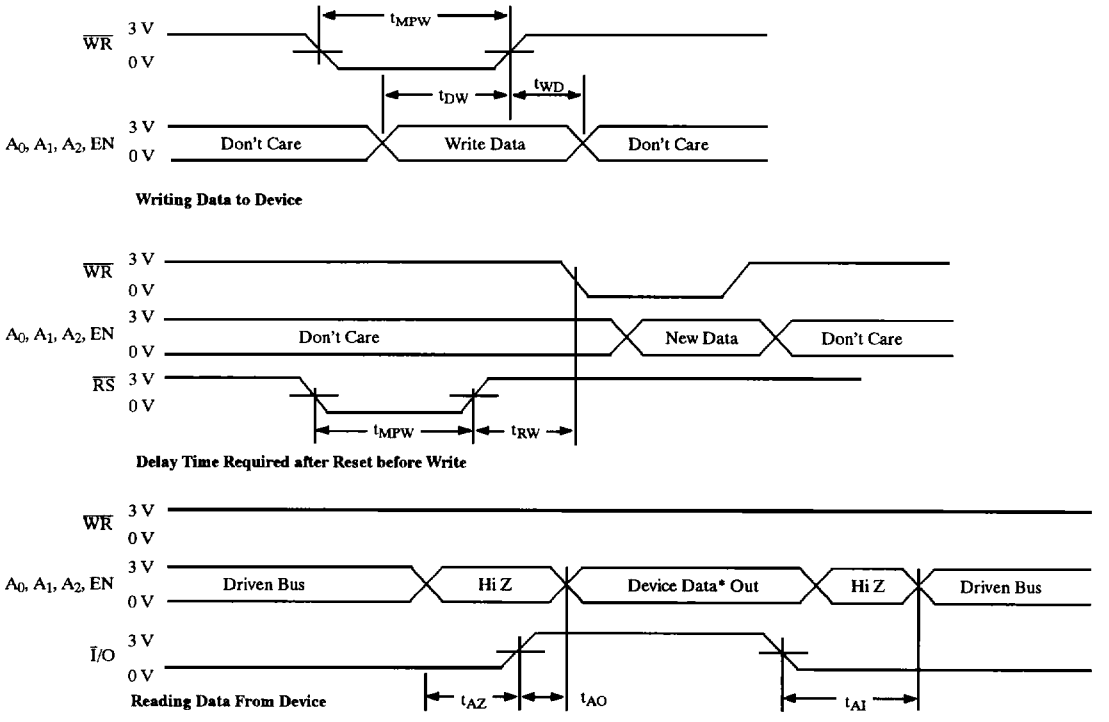
Output Timing Requirements



* Enable must be latched high to read data, otherwise BUS is high Z. V− ≤ −3 V required for readback functionality.

Figure 1.

Applications

To protect against latchup V_L must not exceed V+ by more than 0.3 V. This is easily achieved by generating V_L from V+ using a Zener or a resistor divider network as shown in Figure 2. When an external V_L is available the alternative simple protection circuit shown in Figure 3 should be used to prevent triggering the parasitic SCR during power up. The DG53XA does not require these protection diodes.

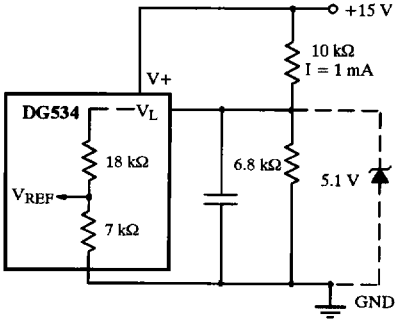


Figure 2. V_L Generated from V+

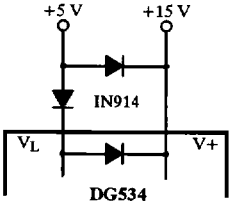


Figure 3. External Diodes Prevent Latchup

Not Recommended for New Designs