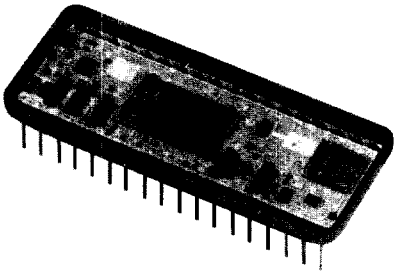
NATEL
HSD/HRD1024

Improved, Second-Generation Synchro (Resolver)-to-Digital Converter Microprocessor Compatible 14-bit Hybrid

Features

- **2.6 arc-minute accuracy**
- ✓ **BIT Output** (Built-in-Test)
- ✓ **Reference Synthesizer** (for improved dynamic accuracy)
- ✓ **No 180° false lock-up**
- **Analog Velocity Output** (use as Tachometer)
- **3-State Latched Output** (inhibit does not interrupt tracking)
- ✓ **Very High Tracking Rate** (7200°/second for high frequency option)
- **High Input Impedance** (solid-state differential input)
- **8- and 16-bit microprocessor compatible**
- **Hermetic 36-pin DDIP package**
- **MIL-STD-883 Processing is Available**



ACTUAL SIZE

Applications

Avionics systems
Antenna monitoring
Servo systems
Coordinate conversion
Fire control systems
Axis rotation
Engine controllers
Industrial control systems
Simulation
Robotics
Machine tool control systems
Solar panel control systems

Description

The HSD1024 (HRD1024), a 14-bit Synchro (Resolver)-to-Digital Converter, packaged in a 36-pin DDIP hybrid, offers a high accuracy of ±2.6 arc-minutes, both 8- and 16-bit microprocessor compatibility and excellent dynamic performance. Model 1024 is a second-generation technology product that provides both lower cost and improved performance with additional features, over its predecessor, the Model 1014. Additional superior features provided in Model 1024 include Built-in-Test, an anti-180° false lock-up circuit and a reference synthesizer. Requiring only a single +15 V-dc main power supply for its operation, the converter maintains both static and dynamic accuracy over a wide range of power supply variations. The digital output voltage levels can be controlled independently by a logic voltage input V_L. The logic supply voltage V_L can range from 4.5 V-dc to the main power supply voltage. At 5 V-dc logic supply the output is CMOS/TTL compatible and can drive one 54/74 gate load or four 54LS/74LS gate loads.

Using a high-accuracy differential signal conditioner for the resolver input and a resistive scott-tee for the synchro-input, the converter provides common mode rejection in excess of 70 dB. The input impedance remains constant and balanced independent of dc power to the converter. This feature prevents loading of the synchro and reference input lines when the converter is not powered. This technique also permits resistor programming for non-standard input voltages.

Model 1024 is a Type-II tracking converter with zero velocity lag error. An internal reference synthesizer permits improved dynamic accuracy by reducing the effects of "speed voltages" at high rotational speeds. The accuracy of the converter is maintained with signal-to-reference phase shifts up to ±45 degrees. An anti-180 degree false lock-up circuit is used to assure that the converter does not get locked onto an angle 180 degrees from the true angle when a step function of 180 degrees is applied. Transferring data from the 1024 is eased through the use of a transparent latch with tri-state outputs configured as two independently enabled bytes. Not only does this allow data to be read without interrupting converter tracking, it also permits memory-mapped data interface and control with the most popular 8- and 16-bit microprocessors and single-board computers.

A built-in-test (BIT) feature provides a logic "one" when the tracking error exceeds ±1°. Monitoring of converter dynamics is facilitated through the availability of analog signals corresponding to converter tracking velocity and instantaneous tracking error. A gain-control pin (Ge) is provided to allow the user to program the converter for non-standard input voltages.

Theory of Operation

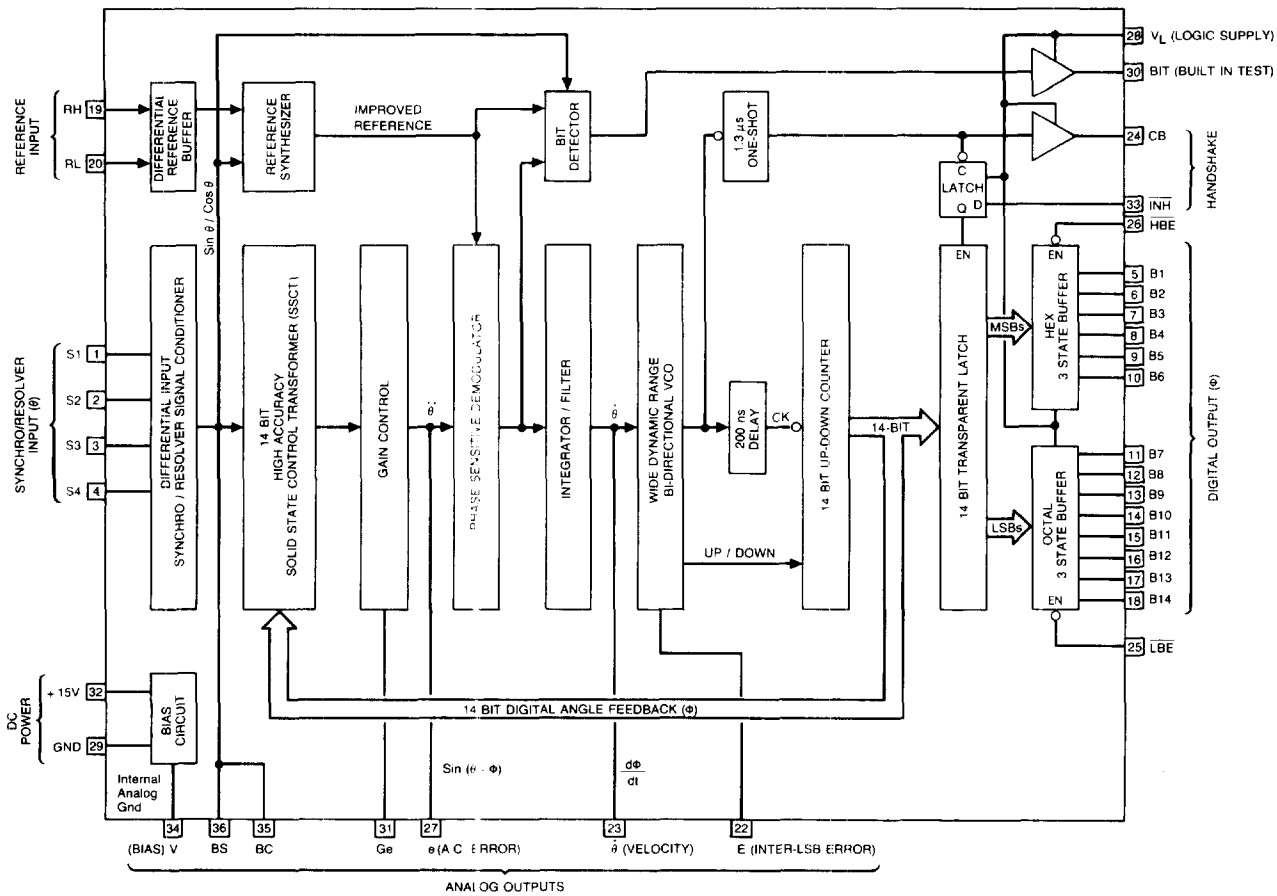


FIGURE 1 1024 Block Diagram

The operation of the Model 1024 is illustrated in the functional block diagram of Figure 1. The 1024 is a high-gain Type II tracking converter exhibiting zero error for a constant velocity input. The basic conversion process consists of continuously comparing the digital output angle (ϕ) and the synchro (or resolver) input angle (θ). An up-down counter, containing the feed-back angle, is changed (increased or decreased) until the feed-back angle equals the input angle. The input and feed-back signals are combined in a solid state control transformer to obtain an error voltage (e), according to the following trigonometric identity:

$$\text{"e"} = \sin(\theta-\phi) = \sin\theta\cos\phi - \cos\theta\sin\phi$$

When the error voltage goes to null, $\sin(\theta-\phi)$ is zero, which makes the angle θ equal to the angle ϕ. Thus, the digital output represents the input shaft angle. Once synchronized, the output angle always tracks the input shaft angle without any lag error for constant velocity input.

The input "signal conditioner" accepts either a synchro or a resolver input and converts it into low level signals $\sin\theta$ and $\cos\theta$, which are applied to the "solid state control transformer" (SSCT) discussed above. Output of SSCT goes to "gain control," which allows for external programming of converter gain for non-standard input voltages. The output is applied to a "phase sensitive demodulator" that is used to determine the polarity (phase) of the error signal "e" with respect to reference signal. Instead of using the external reference signal (RH, RL) as applied to the converter, Model 1024 generates an improved reference internally. The "reference synthesizer" obtains this improved reference from $\sin\theta$ and $\cos\theta$ signals and uses an external reference for coarse phase determination only. Use of the improved reference for demodulating allows the Model 1024 to better reject quadrature components in the error signal "e." The demodulated error signal is applied to an "integrator/filter" which, in addition to ripple and noise filtering, provides the first integration required for the Type II servo loop. The integrator/filter is also used for appropriate gain and phase compensation for loop stability (optmized for low over-shoot and fast settling time). The "wide dynamic range bi-directional VCO" performs a voltage-to-frequency conversion whose pulses or counts are accumulated in the "14-bit up-down counter." The up-down counter performs the second integration in the Type II loop. The input to the VCO inherently provides an analog indication of the digital output rate of change (velocity).

The "14-bit transparent latch" provides a means of holding the digital output steady during data transfer, while allowing the converter to continuously track the input angle. The "1.3 μs one shot" provides an output pulse (CB) for every LSB of output change. It is also used as a clock or gate for the inhibit $\overline{\text{INH}}$ "latch" to prevent attempted "data read" commands during an up-down counter output transition. The "200 ns delay" is used to prevent a race condition between the CB (Converter Busy) output and $\overline{\text{INH}}$ input.

The "3-state buffer" output is split into two bytes to allow interfacing on both 8- and 16-bit data bus systems. The "BIT detector" provides a fault indication as well as help in eliminating false 180 degree digital output readings. The following pages provide more detailed technical discussions for some of these functions.

Reference Synthesizer

To maintain the highest accuracy under both static and dynamic conditions, the 1024 utilizes a "reference synthesizer" to correct for a phase difference between the signal and reference inputs of up to ±45°.

Conventional tracking synchro (resolver)-to-digital converters use a phase sensitive demodulator to detect the phase and amplitude of the error voltage, sin (θ-ϕ). One of the functions of the demodulator is to reject quadrature components in the error signal (e). A phase sensitive demodulator rejects any quadrature signal (signal 90° out of phase) only if the synchro input and its reference are exactly in phase. Zero degree phase shift between reference and signal inputs is not practical in most applications using synchro (resolver)-to-digital converters. Quadrature signal voltage can result from any of the following:

— dynamic synchro/resolver "speed voltages." — a quadrature signal that is proportional to the shaft rotational speed

— synchro/resolver "null voltages"

— capacitive coupling between synchro lines

— differential phase shift in synchro/resolver lines

This quadrature voltage will cause angular error as a variable offset if there is a phase difference between input signals and reference. For example for a 60-Hz synchro with a 5° phase shift rotating at 2 rps (720°/sec), the dynamic error due to speed voltage would be 0.17 degree or 10 arc-minutes!

Natel's model 1024 greatly reduces the effects of this error by creating a synthetic reference. The sine and cosine voltages from the signal conditioner are combined to obtain an in-phase internal reference. Together with the external reference voltage (to determine phase) this improved reference is used for demodulating the error voltage.

Built-in-Test (BIT)

A BIT signal (pin 30) provides an over-velocity or fault indication output signal. The error voltage of the converter is monitored continuously, and when the tracking error exceeds approximately 1 degree (over-velocity or failure), a logic "1" signal is generated to indicate invalid data. Under normal operation the BIT output is at logic "0." Possible conditions that will cause the BIT output to show fault indication are:

- Power-turn-on — BIT output will return to logic "0" when the converter synchronizes to correct input angle ±1°.
- Step-input — Instantaneous input changes greater than ±1° until the converter synchronizes.
- Over velocity condition.
- Excessive shaft angle modulation.
- Reference voltage disconnected.
- Loss of signal — all signal lines are disconnected.
- Converter malfunction — any converter failure which prevents synchronization to the input angle.

Note that BIT output has ≥50% duty cycle logic "1" when reference lines and/or signal lines are disconnected. The cycle frequency is synchronous with the carrier frequency when either the signal or reference (but not both) is missing. When both signal and reference lines are disconnected, the cycle frequency is ≥2 Hz.

From above discussion it is apparent that the BIT output not only serves to self-test the converter but also provides an indication of the operation of the synchro transmission system as well.

No 180° False Lock-up

An additional function of the "Bit Detector" (built-in-test detector), incorporated into the Model 1024 is to eliminate "false 180° digital output readings," during instantaneous 180° input step changes. "180° false lock-up" can occur in most synchro-to-digital converters whenever the synchro (resolver) input angle is "electronically switched" or stepped from one angle to another by 180 degrees. This occurrence, is most common in applications where the input is being supplied by a digital-to-synchro converter and the MSB (180° bit) is turned "ON" or "OFF."

The reason this occurs in most synchro-to-digital converters is because the "solid-state control transformer" (SSCT) used in the conversion process can produce two (2) "nulls" at the error output "e" for a given digital feedback angle. This is easily understood by trignometric indentity

$$\sin[(\theta - \phi) + 180] = -\sin(\theta - \phi)$$
$$= \sin(\theta - \phi)$$
when
$$(\theta - \phi) = \text{zero}$$

Since error output "e" is a sine function (see theory of operation) this creates a possibility of a second null and the converter locking-up 180 degrees away from true angle.

Natel Model 1024 gets around this problem by continuously monitoring sin θ and cos θ signals and comparing the phase relationship with the digital angle output and reference input (RH, RL). When a 180 degree input step is applied, the internal bit-detect circuit is activated, which forces an error in the converter loop to move the digital output angle to the correct reading. As soon as the digital output is properly phased with the shaft angle input, this "intentional error" is removed from the converter loop.

Digital I/O Interface

The output interface circuit consists of a 14-bit holding register (latches) and dual three-state buffers. This not only imparts a versatile interface capability (data multiplexing on 8- or 16-bit data bus) to the 1024, but also enables the $\overline{\text{INH}}$ (inhibit) control to be used without opening the converter loop. The 14-bit holding register holds the digital output steady during data transfer, while allowing the converter to continuously track the input angle.

When $\overline{\text{INH}}$ is at logic "1" or open, each clock pulse from the VCO changes the up-down counter and output by 1 LSB. When $\overline{\text{INH}}$ is at logic "0," the holding register is latched as soon as the CB pulse goes low, and although the up-down counter is updated continuously, the output data is stable. A 1.3 μsec pulse is generated at CB (pin 24) every time the up-down counter changes by 1 LSB.

The outputs of the holding register are buffered by two (a 6-bit and an 8-bit) three-state buffers with separate enable controls. When $\overline{\text{HBE}}$ is at logic "low," the 6 MSB's (B1 through B6) are enabled. When $\overline{\text{LBE}}$ is at logic "low," the 8 LSB's (B7 through B14) are enabled. When $\overline{\text{HBE}}$ and/or $\overline{\text{LBE}}$ are at logic "high" the corresponding bits are in the high impedance state (disabled) and the data-bus sees an essentially open line.

Note that applying inhibit to the converter will latch the data in the 14-bit holding register (and will prevent it from being updated) . . . but will not interfere with the continuous operation of the conversion process.

Enable controls $\overline{\text{HBE}}$ and $\overline{\text{LBE}}$ operate only on the three-state buffers and do not affect the converter loop.

Pin Designations

+15 V	Main Power Supply - 11 V-dc to 17 V-dc
V_L	Logic Voltage - 5 V-dc (For TTL compatible I/O) 4.5 V-dc to +15 V supply (For CMOS compatible I/O)
GND	Power Supply Ground Digital Ground
B1 - B14	Parallel Output Data Bits - B1 is MSB = 180 degrees B14 is LSB = 0.022 degree
S1, S2, S3, S4	Input Analog Signals - Leave S4 unconnected for synchro-input
BS, BC	Buffered Sin θ and Cos θ outputs
RH, RL	Reference Voltage input
BIT	Built-in-Test - A Logic "high" output indicates that output is not tracking the input analog signal within $\pm 1°$.
Ge	External Gain Control
e	Unfiltered ac null error - Output is referenced to bias voltage (V)
$\dot{\theta}$	Velocity Output - dc analog voltage proportional to rotational speed of the input shaft angle. Output is referenced to bias voltage (V)
E	dc Error (Inter-LSB Error) - Error between the digital output and the true shaft angle input between "LSB counts." The output is referenced to the bias voltage (V). (See text for details).
V	Bias Voltage - Internally generated reference voltage. Reference ground for all analog outputs.
$\overline{INH}$	Inhibit Function - A logic "low" freezes the digital angular output. Internal loop keeps tracking the analog input. All other outputs keep following the input. For continuous operation this pin may be left unconnected. Internal active pull-up will apply V_L to the pin.

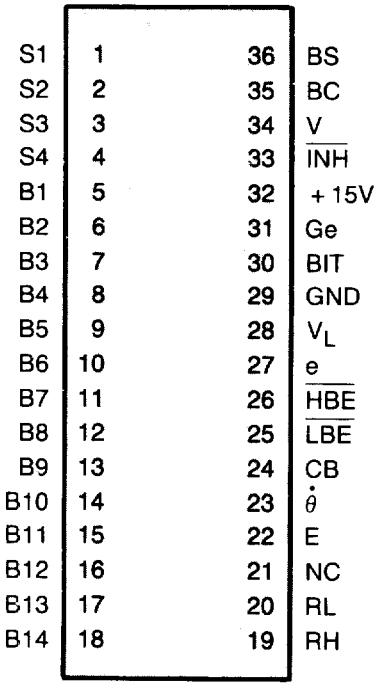


FIGURE 2 HSD1024/HRD1024 Pin Assignment

CB	Converter Busy - A 1.3 μs pulse which occurs during each converter update. Output data can be transferred at the trailing edge of the CB pulse. When converter output is not changing CB is at logic "low." (see text for details)
$\overline{HBE}$	High Byte Enable - Data bits B1 through B6 are enabled (low-impedance state of 3-state output) when $\overline{HBE}$ is set to a logic "low." When $\overline{HBE}$ is set to a logic "high," the data bits B1 through B6 are disabled (high-impedance state of 3-state output).
$\overline{LBE}$	Low Byte Enable - Data bits B7 through B14 are enabled when $\overline{LBE}$ is set to a logic "low." When $\overline{LBE}$ is set to a logic "high," the data bits B7 through B14 are disabled.
Note:	For continuous 14-bit parallel output $\overline{HBE}$ and $\overline{LBE}$ may be left open. Internal active pulldown to ground will apply logic "low" to these pins thus enabling all data bits B1 through B14.

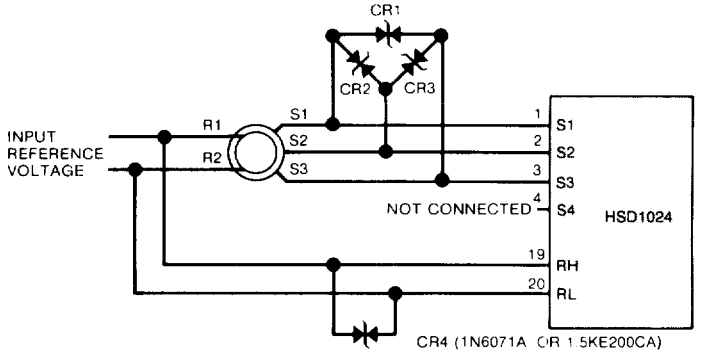
Absolute Maximum Ratings

Signal Inputs	Twice Normal Voltage
Reference Input	200 V-rms
Main Power Supply (+15 V)	+18 V-dc
Logic Voltage (V_L)	−0.3 V-dc to +15 V supply
Digital Inputs	−0.3 V-dc to V_L
Storage Temperature	−65°C to +135°C

When installing or removing the converter from printed circuit boards or sockets, it is recommended that the power supplies and input signals be turned off. Decoupling capacitors are recommended on the main power supply (+15 V) as well as logic voltage (V_L). A 1-μF tantalum capacitor in parallel with 0.01-μF ceramic capacitor should be mounted as close to the supply pins (32 and 28) as possible.

Synchro/Resolver Connections and Phasing

V_{L-L} INPUT	CR1-CR3
11.8 V-rms	1N6049A OR 1.5KE27CA
90 V-rms	1N6070A OR 1.5KE200CA



$$E_{S3-S1} = V_{max} \sin\theta$$
$$E_{S2-S3} = V_{max} \sin(\theta + 120^\circ)$$
$$E_{S1-S2} = V_{max} \sin(\theta + 240^\circ)$$

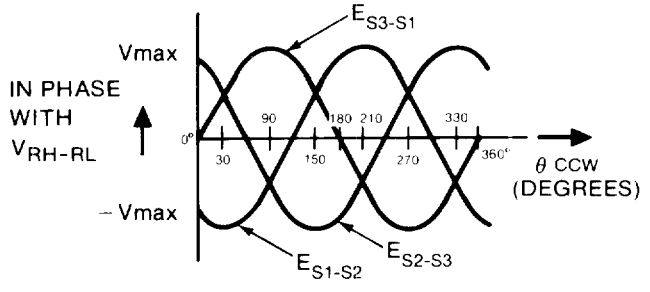
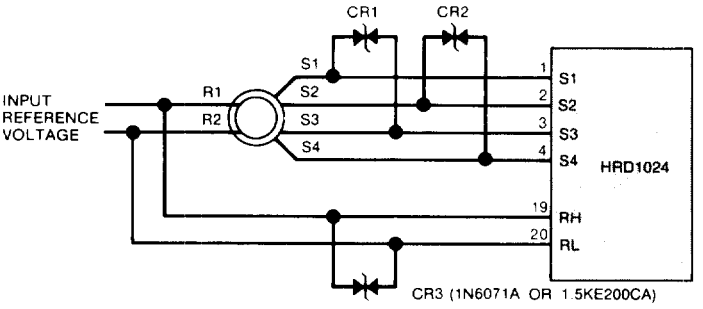


FIGURE 3 Synchro Inputs

V_{L-L} INPUT	CR1, CR2
11.8 V-rms	1N6049A OR 1.5KE27CA
26 V-rms	1N6057A OR 1.5KE56CA
90 V-rms	1N6070A OR 1.5KE200CA



$$E_{S3-S1} = V_{max} \sin\theta$$
$$E_{S2-S4} = V_{max} \cos\theta$$

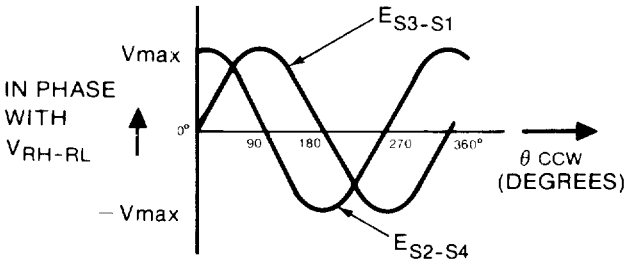
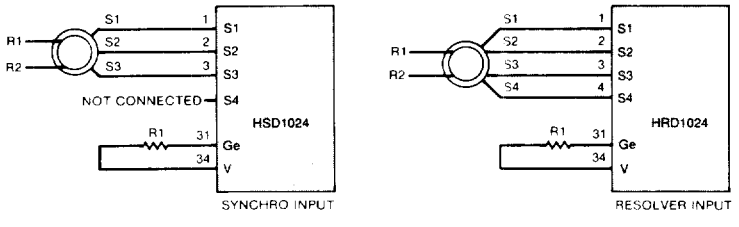


FIGURE 4 Resolver Inputs

The connections for synchro and resolver inputs are shown in figure 3 and figure 4. The input signal conditioner of the Model 1024 converter is designed to accept either synchro or resolver inputs. In addition it uses differential amplifiers and matched precision resistors to provide a high common-mode rejection ratio. This eliminates the need for external transformers for most applications. The input signal conditioner performs two functions. For both synchro and resolver format inputs it serves as a precision attenuator reducing the amplitude of high level ac input signals to levels which can be processed by the converter. For a synchro input, this network transforms three wire synchro information into resolver format (sin θ and cos θ).

Both signal and reference inputs are true differential inputs and use precision thin-film resistors for signal attenuation. If input voltages exceed the absolute maximum ratings, the thin-film resistors may be destroyed. To prevent this from happening, it is recommended that transient voltage suppressors be installed on both signal and reference lines. Synchros and resolvers are highly inductive and can generate or couple transients many times greater than their normal signal voltages and can easily exceed the absolute maximum ratings. This situation is particularly likely to occur in cases where the excitation or source voltage for the synchro (resolver) is switched on or off. Transients can also occur by other equipment being turned on or off. Figures 3 and 4 show recommended methods of connecting synchro and resolver inputs. Transient voltage suppressors given in the tables (or equivalent) must be used to assure input protection.

Resistor Programming for Non-standard Input Voltages



FOR INPUT VOLTAGES V_{IN} (LINE-TO-LINE)	USE MODEL NUMBER	RESISTOR VALUE R1
LESS THAN 11.8 V-rms	1024-TF 1 A	$R1 = \frac{V_{IN}}{11.8\text{-}V_{IN}}$ KΩ
11.8 V-rms to 26V-rms	1024-TF 2 A	$R1 = \frac{V_{IN}}{26 - V_{IN}}$ KΩ
26V-rms to 90V-rms	1024-TF 9 A	$R1 = \frac{V_{IN}}{90\text{-}V_{IN}}$ KΩ

FIGURE 5 Resistor Programming for Non-standard Inputs

Non-standard input signal voltages are accommodated with the addition of an external resistor connected between Gain control, Ge (pin 31), and Bias Voltage, V (pin 34). The circuit configuration for resistor programming is shown in figure 5. The formulas for determining the value of external resistor R1 and the converter model to be used are shown in the table. The resistor R1 increases the gain of the error amplifier, thereby compensating for lower input voltages. For input voltages greater than 90 V-rms line-to-line, the method described in the Natel HSRD1006 data sheet can be used. Contact the factory if you require assistance.

Data Transfer

Due to the nature of the Type II servo conversion mechanism incorporated in the 1024, the output data angle always tracks the synchro (resolver) input shaft angle within the converter's rated maximum tracking rate (angular velocity) and bandwidth. Theoretically, for every 0.022 degree of input angle change, there will be a corresponding data output change of one LSB. To prevent reading data during an output change or transition, the following methods of data transfer can be used:

1) Synchronous transfer with shaft angle change.

   Use CB (Converter Busy) pulse to clock data into an external register. Use the falling edge of CB as an edge triggered clock. (Rising edge of CB could be used but data would have an additional error of ±1 LSB.) Data changes within 800 ns after the rising edge of the CB pulse.

2) Asynchronous transfer with shaft angle change (using CB).

   Monitor the CB (Converter Busy) during a data transfer attempt. If CB is at logic "1," (the data will be void) . . . try another data transfer attempt. If CB is at logic "0" the data will be good. Note that the longest CB pulsewidth and therefore the longest wait period is 2 μsec. The CB pulse can essentially be used to gate an external data clock enable since the converter updates within the CB logic "1" duration (2 μs maximum).

3) Asynchronous transfer with shaft angle change (using $\overline{INH}$).

   The simplest method of data transfer (which is completely independent of input shaft angle change) is to use the inhibit ($\overline{INH}$) function to hold or freeze the current data output angle. Set the $\overline{INH}$ input to logic "0" . . . wait a minimum of 1 μs . . . transfer the data . . . return $\overline{INH}$ to logic "1" for a minimum of 2 μs. This method of asynchronous data transfer from the 1024 is shown in Figure 6. Control functions $\overline{HBE}$ and $\overline{LBE}$ have internal pull down circuitry, permitting these pins to be left open (unconnected).

It should be noted that the $\overline{INH}$ control does not affect the conversion process . . . it only affects the transparent output latch. If the synchro (resolver) angle input changes while an inhibit is applied ($\overline{INH}$ = "0"), the internal data angle (up-down counter output) will still track the input. Fresh output data (B1-B14) will be available within 2 μs after the $\overline{INH}$ input returns to logic "1" (un-inhibit), regardless of the previous $\overline{INH}$ logic "0" duration.

Note: The CB output (Converter Busy) will always produce a pulse for every LSB of output angle change, regardless the state of the $\overline{INH}$ (inhibit) input.

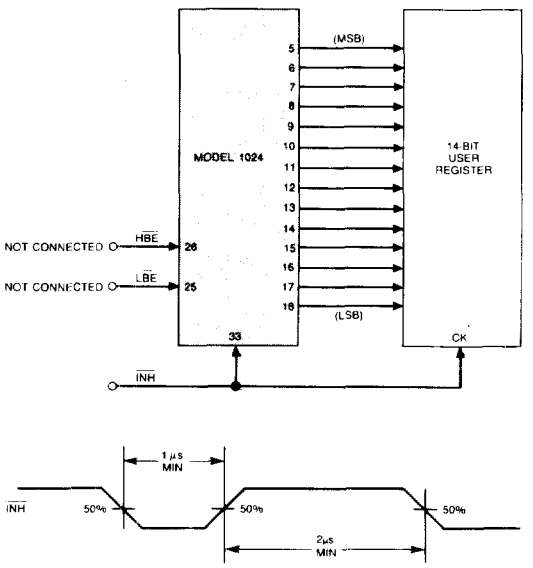
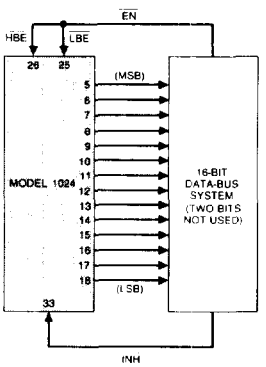


FIGURE 6 Asynchronous Data Transfer

Single-Byte Data Transfer on 16-Bit Data Bus



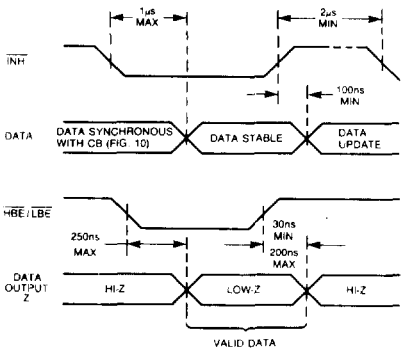


FIGURE 7 Digital Connections and Timing for Single-Byte Data Transfer

The circuit configuration and timing diagram for transferring data from the Model 1024 to a 16-bit 3-state data-bus system is shown in Figure 7. A typical sequence of events would be as follows:

1) Apply the $\overline{INH}$ input for a minimum of 1 μs before transferring valid data.

2) Set $\overline{HBE}$ and $\overline{LBE}$ to logic "0" (3-state enables) for a minimum of 250 ns before transferring valid data.

   Note: The last device on the data-bus should be set to high impedance state no later than 30 ns after $\overline{HBE}$ and $\overline{LBE}$ are set to logic "0."

3) Transfer Data

4) Return $\overline{HBE}$ and $\overline{LBE}$ to logic "1" at least 200 ns before the next device is put on the data bus.

   Note: The data output remains in the low-Z state for a minimum of 30 ns after the rising edge of $\overline{HBE}$ and $\overline{LBE}$, therefore data can be transferred at the rising edge of $\overline{HBE}$ and $\overline{LBE}$ . . . provided the data hold requirement of the external device is less than 30 ns.

5) Return $\overline{INH}$ to logic "1" no earlier than 100 ns before valid data is transferred. The $\overline{INH}$ input may remain at logic "0" indefinitely . . . but must return to logic "1" for a minimum of 2 μs to allow update of fresh accurate output data.

   Note: $\overline{INH}$ (inhibit) input function is independent from $\overline{HBE}$ and $\overline{LBE}$ (3-state enable) inputs.

Two-Byte Data Transfer on 8-Bit Data Bus

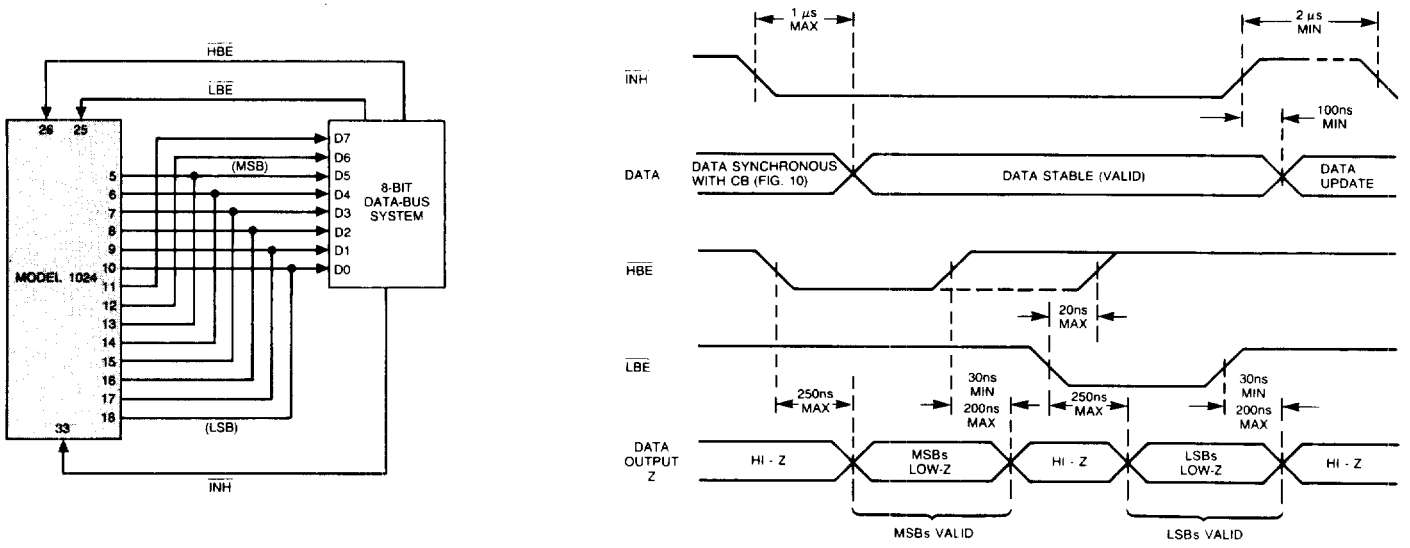


FIGURE 8 Digital Connections and Timing for Two-Byte Data Transfer

The circuit configuration and timing diagram for transferring data from Model 1024 to an 8-bit 3-state data-bus system is shown in Figure 8. A typical sequence of events would be as follows:

1) Apply the $\overline{INH}$ input for a minimum of 1 μs before transferring valid data.

2) Set $\overline{HBE}$ to logic "0" (high-byte-enable) for a minimum of 250 ns before transferring valid data (MSBs).

   Note: The last device on the data-bus should be set to high impedance state no later than 30 ns after $\overline{HBE}$ is set to logic "0."

3) Transfer MSBs. (B1-B6)

4) Return $\overline{HBE}$ to logic "1" no later than 20 ns after $\overline{LBE}$ is set to logic "0."

5) Set $\overline{LBE}$ to logic "0" (low-byte-enable) for a minimum of 250 ns before transferring valid data (LSBs), but not more than 20 ns before $\overline{HBE}$ has returned to logic "1" (rising edge).

6) Transfer LSBs. (B7-B14)

7) Return $\overline{LBE}$ to logic "1" at least 200 ns before the next "device" is put on the data-bus.

8) Return $\overline{INH}$ to logic "1" no earlier than 100 ns before valid data is transferred. The $\overline{INH}$ input may remain at logic "0" indefinitely . . . but must return to logic "1" for a minimum of 2 μs to allow update of fresh accurate output data.

Notes:

— $\overline{HBE}$ and $\overline{LBE}$ data bytes can be transferred in any sequence ($\overline{HBE}$ or $\overline{LBE}$ first). The timing requirements are the same for both $\overline{HBE}$ and $\overline{LBE}$ data byte enables.

— The data output remains in the low-Z state for a minimum of 30 ns after the rising edge of $\overline{HBE}$ and/or $\overline{LBE}$, therefore data can be transferred at the rising edge of $\overline{HBE}$ and/or $\overline{LBE}$ respectively . . . provided the data hold requirement of the external device is less than 30 ns.

— $\overline{INH}$ (inhibit) input function is independent from $\overline{HBE}$ and $\overline{LBE}$ (3-state enable) inputs.

— The CB output (Converter Busy) will always produce a pulse for every LSB of output angle change, regardless of the state of the $\overline{INH}$ (inhibit) input or $\overline{HBE}$/$\overline{LBE}$ (3-state enable) inputs.

Interfacing With a 16-Bit Microprocessor

Interface between the synchro-to-digital converter (Model 1024) and a 16-bit microprocessor is illustrated in Figure 9. To simplify the system interface to peripherals and memory devices with varying access times, the microprocessor communicates with a system via an asynchronous bus. The address decoder generates the $\overline{INH}$ chip select for the converter. When the converter returns the CB signal, the microprocessor reads the data and terminates the bus cycle. Data strobes $\overline{UDS}$ and $\overline{LDS}$ enable the converter for 14-bit word transfers. If the interface software attempts an 8-bit read (i.e., the microprocessor generates only one data strobe), then a bus error ($\overline{BERR}$) is generated. $\overline{BERR}$ terminates the bus cycle and automatically generates an exception call to the operating system. Data could be transferred from the converter using the instruction MOVE.W 1024, EA, which moves a 14-bit data word from the peripheral to an effective address — either in a register on the microprocessor chip or in a system memory location.

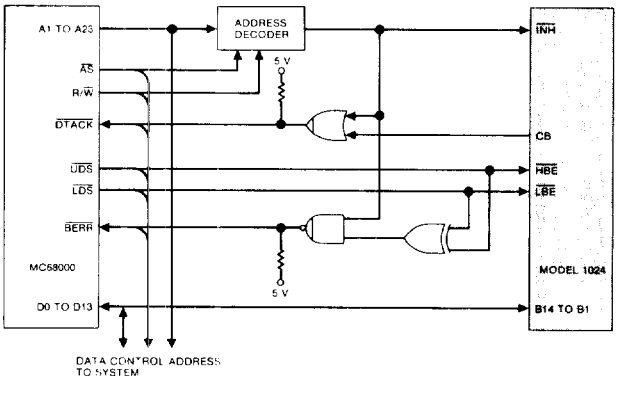


FIGURE 9 Interfacing 1024 Converter with 16-bit Microprocessor (MC68000) Via Asynchronous Bus

Specifications

PARAMETER	VALUE	REMARKS	TEST LEVEL
Digital Output Resolution	14-bits (1.32 arc-minutes)	MSB = 180° LSB = 0.022°	Note 2
Accuracy	±5.2 arc-minutes (Option S) ±2.6 arc-minutes (Option H)	Accuracy applies over operating temperature range, ±10% frequency variation and includes hysteresis	Note 1
Reference Input			
Voltage	4 to 130 V-rms		Note 2
Frequency	700 to 3000 Hz (Option 8) 360 to 1000 Hz (Option 4) 47 to 1000 Hz (Option 6)	800 Hz Models 400 Hz Models 60 Hz Models	Note 3
Input Impedance (Minimum)	250 KΩ Single Ended 500 KΩ Differential		Note 2
Common Mode Range	±250 V peak maximum	dc plus recurrent ac peak	Note 3
Synchro/Resolver Inputs			
Input Voltages (line-to-line)	11.8 V-rms (Option 1) 26 V-rms (Option 2) 90 V-rms (Option 9)	Accuracy of the converter is maintained with ±10% variation in signal voltages	Note 1
Input Impedance (Minimum)	Differential / Line-to-GND 60 KΩ / 30 KΩ 150 KΩ / 75 KΩ 500 KΩ / 250 KΩ	11.8 V-rms L-L Models 26 V-rms L-L Models 90 V-rms L-L Models	Note 2
Impedance Unbalance	0.1% maximum	For all Models	Note 3
Common Mode Range	± 25 V peak ± 55 V peak ±180 V peak	11.8 V-rms Models 26 V-rms Models 90 V-rms Models	Note 3
Common Mode Rejection Ratio	70 dB minimum	dc to 1000 Hz	Note 3
Harmonic Distortion	10% maximum	Without degradation in accuracy specification	Note 3
Digital Inputs		CMOS transient protected	
$\overline{INH}$	Logic "1" Logic "0"	Digital output follows analog input signals Output data latched in holding register (Does not interrupt converter tracking loop)	Note 1
$\overline{HBE}$	Logic "1" Logic "0"	6 MSBs are in high impedance state of 3-state output 6 MSBs are enabled	Note 1
$\overline{LBE}$	Logic "1" Logic "0"	8 LSBs are in high impedance state of 3-state output 8 LSBs are enabled	Note 1
Voltage Levels Logic "0" Logic "1"	 −0.3 V-dc to 0.8 V-dc 2.4 V-dc to 5 V-dc	 For V_L = 5 V-dc	 Note 2
Logic "0" Logic "1"	−0.3 V-dc to 2.0 V-dc 10 V-dc to 15 V-dc	For V_L = 15 V-dc	Note 3
Inputs Currents $\overline{INH}$	 −15 μA typical (−30 μA max), "active" pull-up to power supply (V_L)	 When not used, may be left unconnected	 Note 3
$\overline{HBE}$, $\overline{LBE}$	15 μA typical (30 μA max), "active" pull-down to ground (GND)	When not used, may be left unconnected	Note 3
Digital Outputs		CMOS Outputs	
Data Bits (B1-B14)	Natural Binary Angle	Positive logic B1 = 180° B14 = 0.022°	
CB	Logic "0" Logic "1" (Nominal 1.3 μsec pulse for every LSB change)	Output angle not changing Output angle changing (leading edge initiates output change---see Figure 10)	Note 1
BIT	Logic "0" Logic "1"	Digital output tracking analog input Fault indication (tracking error > ±1° typical)	Note 1

PARAMETER	VALUE	REMARKS	TEST LEVEL
Digital Outputs (cont.)			
Drive Capability Data Bits (B1-B14), CB, BIT "0" Sink Current "1" Source Current	1 Standard TTL minimum 1.6 mA (min) @ 0.40 V-dc −1.6 mA (min) @ 3.0 V-dc	For V_L = 4.5 V-dc and over operating temperature range See Figure 15 for typical drive currents	Note 3
Hi-Z Output Leakage Data Bits (B1-B14)	±10 μA maximum	Output Capacitance ≈ 5 pf	Note 3
Analog Outputs	Typical, unless specified		
V (Bias Voltage)	1/2 (+15V − 0.7) ±10%	7.15 V-dc ±10% for +15 V-dc main power supply	Note 3
e (Unfiltered Error)	16 mV-rms typical per 1 LSB	ac voltage referenced to V	Note 3
BS, BC (Buffered Sin θ and Cos θ)	1 V-rms nominal	ac voltage referenced to V (θ is input shaft angle)	Note 3
Drive Capability	±1 mA minimum	All analog outputs	Note 3
E (dc Error/Inter-LSB Error)	−1.0 V-dc per 1 LSB (typical) ±0.8 V-dc range (typical)	dc voltage referenced to V	Note 3
$\dot{\theta}$ **(Velocity Output)**	Typical, unless specified	dc voltage referenced to V (BIAS)	
Scale Factor (Gain) @ 25°C	0.7 mV/deg/sec (typical) 1.4 mV/deg/sec (typical) 7.0 mV/deg/sec (typical)	800 Hz Models 400 Hz Models 60 Hz Models	Note 2
Full Scale Output @ 25°C	5.04 V-dc @ 7200°/sec (typical) @ 3600°/sec (typical) @ 720°/sec (typical)	800 Hz Models 400 Hz Models 60 Hz Models	Note 2
Linearity @ 25°C	±5% of full scale (maximum) ±2% of full scale (maximum) ±1% of full scale (maximum)	800 Hz Models 400 Hz Models 60 Hz Models	Note 2
Output Noise Static Input Input changing at a constant maximum tracking rate	 10 mV-rms typical 10 mV-rms typical 10 mV-rms typical 50 mV-rms typical 50 mV-rms typical 90 mV-rms typical	 800 Hz Models 400 Hz Models 60 Hz Models 800 Hz Models 400 Hz Models 60 Hz Models	Note 3 Note 3
Output Offset @ 25°C	± 5 mV-dc typical ±20 mV-dc maximum	Static output voltage	Note 2
Polarity	Positive output for increasing angle		Note 3
ΔGain vs Polarity (Gain Differential)	10% Maximum	Between positive and negative outputs (reversal error)	Note 2
Temperature Coefficients Gain Linearity Output Offset ΔGain vs Polarity	 ±500 PPM/°C (typical) ±200 PPM/°C (typical) ± 30 μV/°C (typical) ±200 PPM/°C (typical)		Note 3
Power Supply Dependence Gain Linearity Output Offset ΔGain vs Polarity	 −1% per percent (maximum) 0.1% per percent (typical) ±20 μV per percent (typical) 0.1% per percent (typical)	+15 V-dc power supply	Note 3
Analog Gain Control	Range of 4 to 1	Using Ge (pin 31) external gain programming	Note 3
Dynamic Characteristics	Typical, unless specified	Specified for Main Power Supply = +15 V-dc	
Maximum Tracking Rate	±20 rps (7200° per sec) minimum ±10 rps (3600° per sec) minimum ±2 rps (720° per sec) minimum	800 Hz Models 400 Hz Models 60 Hz Models	Note 1
Velocity Constant (K_V)	∞	Type II Servo loop	
Maximum Acceleration	1,200,000°/sec^2 (typical) 300,000°/sec^2 (typical) 12,000°/sec^2 (typical)	800 Hz Models 400 Hz Models 60 Hz Models	Note 3

Specifications Continued

PARAMETER	VALUE	REMARKS	TEST LEVEL
Dynamic Characteristics (cont.)			
Acceleration Constant (K_A)	192,000/sec^2 (nominal) 48,000/sec^2 (nominal) 1,900/sec^2 (nominal)	800 Hz Models 400 Hz Models 60 Hz Models	Note 3
Acceleration for 1 LSB error (LSB = 0.022°)	4000°/sec^2 (typical) 1000°/sec^2 (typical) 40°/sec^2 (typical)	800 Hz Models 400 Hz Models 60 Hz Models	Note 3
Settling Time to 1 LSB (for 179° step change)	75 msec maximum 150 msec maximum 500 msec maximum	800 Hz Models 400 Hz Models 60 Hz Models	Note 2
Settling Time to 1 LSB (Small signal step ≤1.4°)	20 msec maximum 40 msec maximum 180 msec maximum	800 Hz Models 400 Hz Models 60 Hz models	Note 2
Converter Bandwidth	180 Hz typical 90 Hz typical 18 Hz typical	800 Hz Models 400 Hz Models 60 Hz Models	Note 3
Reference Synthesizer			
Phase-shift allowed between Input signals and Input reference	±45° guaranteed ±65° typical	Without any degradation of converter accuracy	Note 2
Power Supplies			
Main Power Supply (+15V)			
Voltage	11 V-dc to 17 V-dc	Without degradation in accuracy specification	Note 3
Current	30 mA typical, 45 mA maximum 15 mA typical, 25 mA maximum 15 mA typical, 25 mA maximum	800 Hz Models 400 Hz Models 60 Hz Models	Note 1
Logic Power Supply (V_L)			
Voltage	4.5 V-dc to main power supply	5 V-dc ±10% for TTL compatible I/O	Note 3
Current	1 mA maximum 3 mA maximum	For V_L = 5 V-dc For V_L = 15 V-dc	Note 1 Note 3
Thermal Characteristics			
Junction Temperature Rise Above Case	2°C typical, 5°C maximum	For component with highest temperature rise	Note 3
Case Temperature Rise Above Ambient	7°C typical, 15°C maximum 25°C maximum (800 Hz Models)	Without any heat sink	Note 3
Power Dissipation	230 mW typical, 380 mW max. 680 mW max. (800 Hz Models)	For V_L = 5 V-dc and Main Power Supply = 15 V-dc	Note 3
Physical Characteristics			
Type Size Weight	36 PIN Hermetic Double DIP 0.78 x 1.9 x 0.21 inch (20 x 48 x 5.3 mm) 0.6 oz (17 g) maximum	3 Standoffs are added to the package to insulate it from printed circuit board traces (Standoffs included in 0.21 inch height dimension)	Note 3

NOTE 1. Compliance of each component to this specification is 100% guaranteed by Natel. To assure compliance, this key parameter is 100% tested.

NOTE 2. Compliance of each component to this specification is 100% guaranteed by Natel. To assure compliance, AQL levels are verified using a lot sample level in the range of one to five percent.

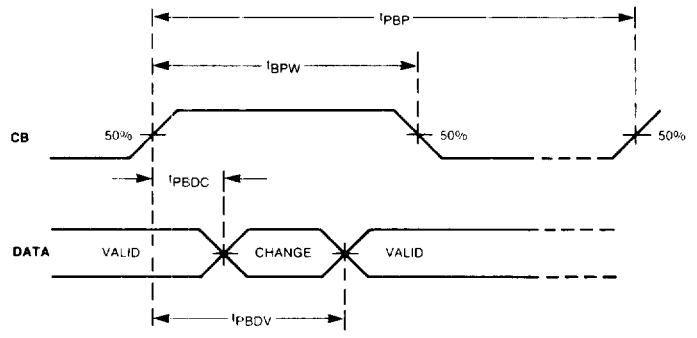
NOTE 3. Compliance of each component to this specification is 100% guaranteed by Natel. To assure compliance, AQL levels are verified using a lot sample level of less than one percent. Note 3 parameters are maximum design limits.

If your application requires 100% testing of any additional parameters of the specification or requires non-standard input or output characteristics, please contact a Natel Applications Engineer or the Sales Department.

Digital I/O Characteristics and Timing

T_a = 25°C R_L = 200 K Ω Input t_r t_f = 20 ns V_L = 5 V-dc C_L = 50 pF

CHARACTERISTIC	LIMITS			UNITS	FIGURE
	MIN	TYP	MAX		
BUSY PULSE WIDTH (t_{BPW})	0.8	1.3	2.0	μs	10
BUSY PERIOD (t_{PBP})	2.0	NOTE 1	∞	μs	10
BUSY TO DATA CHANGE (t_{PBDC})	100	500	—	ns	10
BUSY TO DATA VALID (t_{PBDV})	—	600	800	ns	10
INHIBIT TO DATA STABLE (t_{PIDS})	0	—	1.0	μs	11, 12
INHIBIT TO DATA UP-DATE (t_{PIDU})	100	—	—	ns	11, 12
INHIBIT UPDATE PULSE WIDTH(t_{IPW})	2.0	—	—	μs	12
HIGH Z TO LOW Z (t_{PHZL})	30	150	250	ns	13
LOW Z TO HIGH Z (t_{PLZH})	30	100	200	ns	13
TRANSITION HIGH TO LOW (t_{THL}) 90%-10%	—	45	75	ns	14
TRANSITION LOW TO HIGH (t_{LHT}) TTL 10%-50% (t_{TLH}) CMOS 10%-90%	— —	60 120	100 200	ns ns	14



NOTE 1: **Busy Period (t_{PBP})** = $\frac{K \cdot 10^6}{2^N \cdot R}$ (μs)

For Reference:

Busy Frequency = $\frac{2^N \cdot R}{K}$ (Hz)

Rate (R) = $\frac{K \cdot \text{Busy Frequency}}{2^N}$

Where,

N = Converter Resolution (14)

K = 360 (For Degrees) or
= 2π (For Radians)
and

R = Rate (Degrees / Second) or
= Rate (Radians / Second)

FIGURE 10 Converter Busy and Data Timing

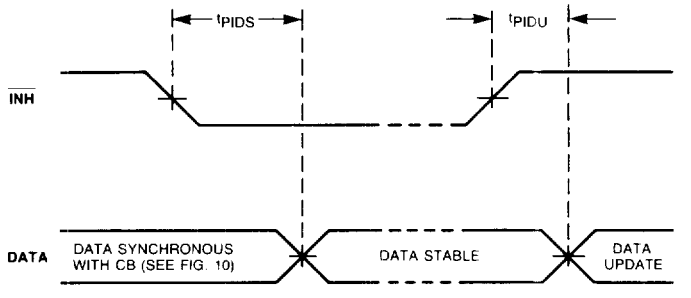


FIGURE 11 Inhibiting Output Data Update

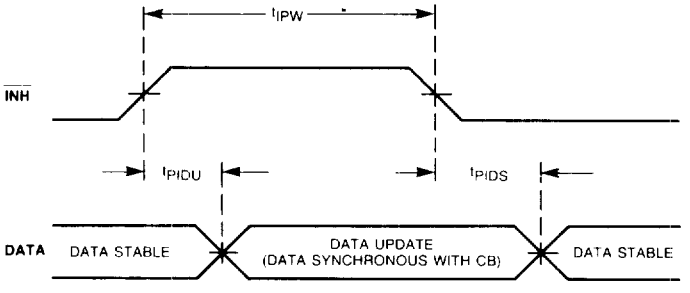


FIGURE 12 Enabling Output Data Update

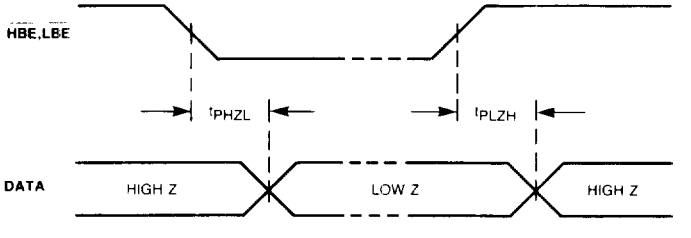


FIGURE 13 3-State Output Timing

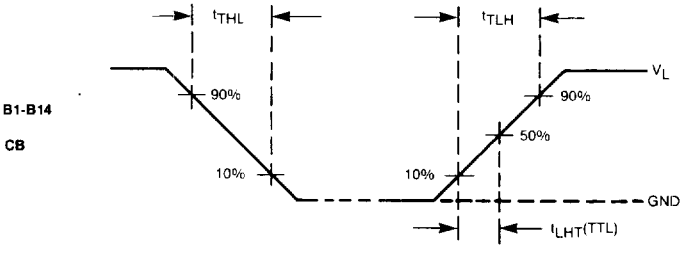
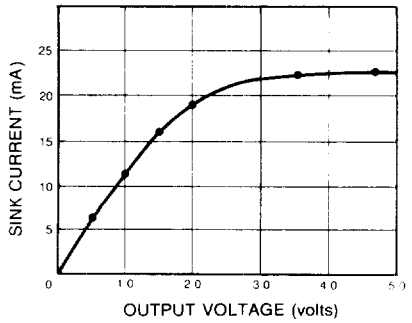
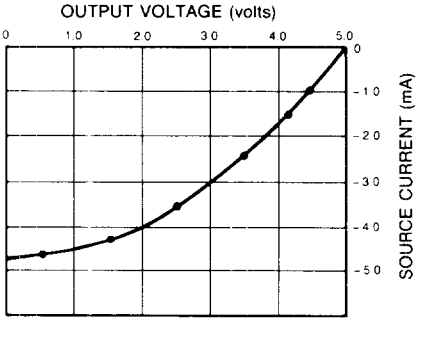


FIGURE 14 Transition Times



SINK



SOURCE

FIGURE 15 Output Drive Current (Typical @ V_L = 5V-dc, Ta = 25°C)

As a by-product of the conversion process, the Model 1024 produces various analog signals. Some of these analog signals have proven useful in various applications and are therefore brought out. The absolute value of these analog outputs is not critical to the overall conversion process. Therefore, unless otherwise specified, they are not closely controlled or characterized functions. These outputs are:

- BS (pin 36), Buffered Sin θ
- BC (pin 35), Buffered Cos θ
- V (pin 34), Internal Analog Ground (Bias)
- e (pin 27), ac Error
- $\dot{\theta}$ (pin 23), Velocity Output
- E (pin 22), dc Error (Inter-LSB Error)

"BS" and "BC" are the outputs of the synchro/resolver signal conditioner. They provide a buffered (operational amplifier output) ac representation of the sine and cosine of the input shaft angle. The nominal maximum output level is 1 V-rms (sin 90°, cos 0°) for specified input voltages.

"e," the ac error, is an ac voltage (at the output of error amplifier) which is proportional to the instantaneous error of the converter $\sin(\theta\text{-}\phi)$ . . . see theory of operation. The output "e" is also proportional to the input angular acceleration . . . the rate of change of angular velocity. This angular error as a function of acceleration is inversely proportional to the acceleration constant (K_A).

$$\text{error (degrees)} = \frac{\text{angular acceleration (degrees/sec}^2)}{K_A\,(\text{sec}^{-2})}$$

For 1 LSB error, the magnitude of the error voltage is 16 mV-rms. Polarity of the error is determined by demodulating (phase sensitive) this voltage with the reference voltage (RH, RL).

"$\dot{\theta}$" is a dc voltage proportional to the velocity of the digital output angle (thereby the input shaft angle). The voltage goes positive for increasing digital angle and goes negative for decreasing digital angle. At maximum tracking velocity, the output voltage is 5.04 volts-dc. Detailed specification for velocity functions are provided on page 9. Dynamic characteristics including open loop and closed loop transfer functions are provided on pages 13 and 14.

"E," the dc Error (Inter-LSB Error), provides a dc output voltage that is proportional to the difference between the digital position output and the actual shaft angle input (between LSB counts). The actual input shaft angle is equal to the digital output angle "minus" the Inter-LSB output (E). This output can be used to further resolve the input shaft angle. The nominal scale factor is −1 V-dc per +1 LSB of "Inter-LSB" error. The nominal output voltage range is ±0.8 V-dc (with respect to V "bias"), which is equivalent to converter hysteresis +1 LSB. Figure 16 shows detailed waveforms for this "Inter-LSB Error."

"V," internal analog ground, also referred to as the "bias voltage" provides a reference point for all analog functions. The typical value of the bias voltage, V, is:

V = 1/2 (Main Power Supply −0.7 V-dc)

= 7.15 V-dc ±10% (for Main Power Supply = +15 V-dc)

All analog outputs have a minimum output drive of ±1 mA with respect to V (bias). For a main power supply of +15 V-dc, the minimum output swing is ±5 V peak with respect to V (bias).

If a bipolar signal, with respect to power supply ground, is required for any analog output, a difference circuit, as shown in Figure 17, may be used. The output can be scaled to a desired value by selecting the gain of the circuit. Also if reverse polarity output is desirable, the bias and signal connections to the difference amplifier should be reversed.

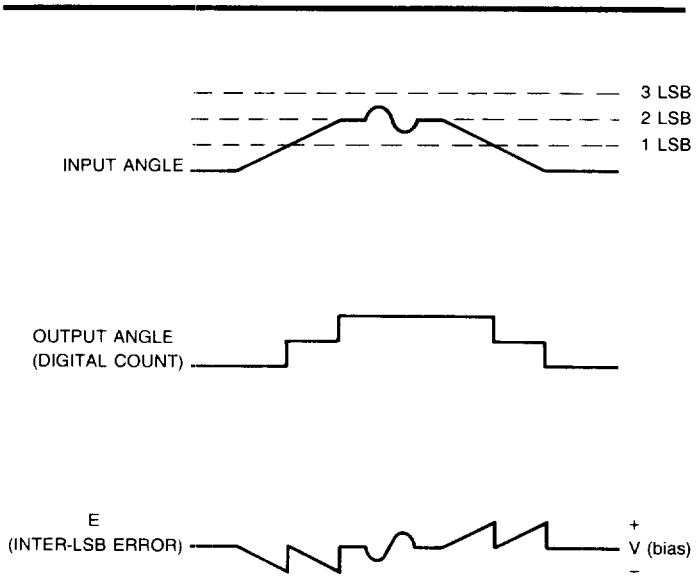


FIGURE 16 "E" dc Error (Inter-LSB Error) Waveforms

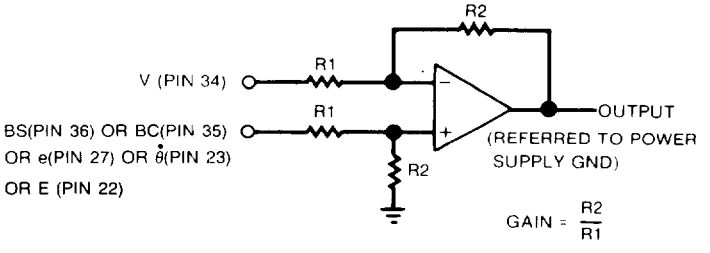


FIGURE 17 Difference Circuit for Bipolar Analog Outputs

Dynamic Performance

The HSD1024 (HRD1024) incorporates a high gain. Type II, servo loop to provide accurate real-time synchro (resolver)-to-digital conversion. The converter is characterized for the following dynamic input angle conditions:

(1) Static Input Angle

(2) Constant Rate of Change of Input Angle Position (Constant Velocity)

(3) Constant Rate of Change of Input Angular Velocity (Constant Acceleration)

(4) Variable Rate of Change of Angular Velocity (Sinusoidal Modulation)

(5) Infinite Rate of Change of Angular Velocity (Step Input)

The 1024 accuracy specification applies for **Static (1)** and **Constant Velocity (2)** input conditions, as long as the maximum converter tracking rate is not exceeded.

For **Constant Acceleration (3)** of input angle, the digital output will lag the input by the following amount:

$$\text{Acceleration Lag (error)} = \frac{\text{Input Angle Acceleration}}{K_A}$$

The values of maximum tracking rate and acceleration constant (K_A) for different frequency options are given in specification table (pages 8, 9 and 10). Note that the specified K_A is typical and is not a tightly controlled parameter (converter K_A is analogous to open-loop gain of an operational amplifier). Also, K_A varies proportional to input voltage (line-to-line) variations.

For **Sinusoidal Shaft Angle Modulation (4),** the digital angle output will lag the input by the following amount:

$$\text{Sinusiodal Lag (error p-p)} = \frac{2 \times \pi^2 \times \text{Amp (p-p)} \times F^2}{K_A}$$

Where: Amp (p-p) = peak-peak angle modulation level

F = modulation frequency (Hz)

K_A = converter acceleration constant

The Peak Rate (Velocity) for a given sinusoidal modulation is:

$$\text{Rate (degrees/sec)} = \pi \times \text{Amp (degrees p-p)} \times F \text{ (Hz)}$$

For **Step Inputs (5)**, the digital angle output will respond as a function of the converter's Large Signal and Small Signal transient response.

The ***Large Signal*** transient response is dependent solely on the maximum velocity (ω_{max}) and the maximum acceleration (α_{max}) of which the converter is capable. The large signal parameters are defined in figure 18. The synchronizing time (t_{SYNC}) for large signals can be partitioned into three distinct intervals. Acceleration time (t_{ACC}) Slew time (t_{SLEW}) and Overshoot time (t_{OS}).

Acceleration time is the time interval from application of the step-input to the point at which the converter reaches its maximum velocity.

Slew time is the time interval from the point at which maximum velocity is obtained to the point at which the output angle is first equal to the input angle.

Overshoot time is the time interval from the point at which the converter output angle first equals the input angle (and applies constant acceleration in the opposite direction) to the point at which the output angle again reaches the input angle.

At the end of overshoot time, the small signal response becomes dominant and the converter will settle to the final value according to its small signal transient response function.

The ***Small Signal*** settling time (t_s) is specified for step inputs of less than 1.4 degrees. For small signal steps, the settling time is a function of the transient response of the converter.

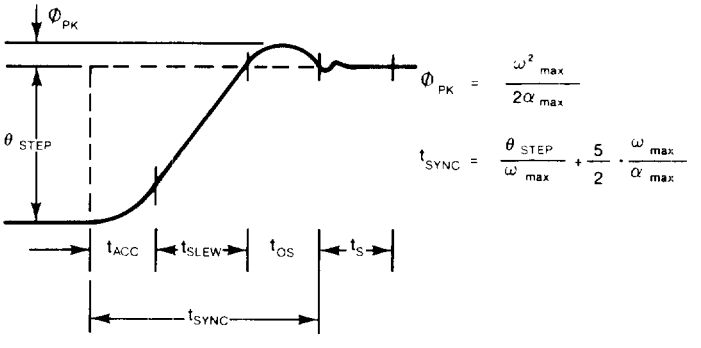


FIGURE 18 Large Signal (≥1.4°) Response Parameters

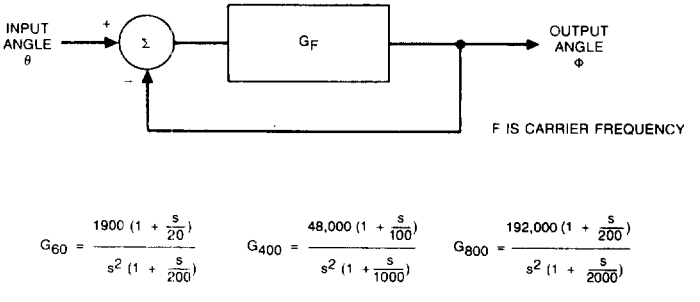


FIGURE 19 Transfer Functions for 1024

Transfer Function

The basic control loop model and transfer functions for 60-Hz, 400-Hz and 800-Hz models are shown in Figure 19. A more detailed model with corresponding transfer functions for both position and velocity outputs is shown in Figure 20. Typical values for transfer function parameters for different frequency options are shown in Table 1.

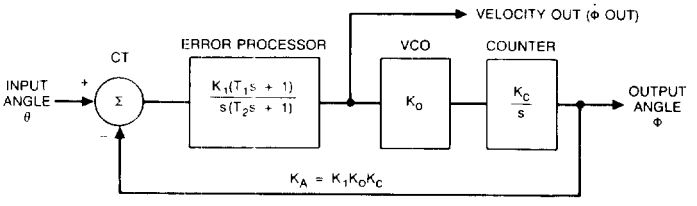
Transfer function parameters are determined by the specified frequency option of the converter. When a converter is operated at a frequency higher than the specified, these parameters remain the same. For some applications it may be advantageous to use a lower bandwidth converter operating at a higher carrier frequency. For example, to improve the position noise rejection, velocity output noise/ripple and velocity linearity, a 60-Hz frequency (option 6) could be used and operated at higher carrier frequency such as 400 Hz.

PARAMETER	UNITS	FREQUENCY OPTION		
		60 Hz	400 Hz	800 Hz
K_A	sec^{-2}	1900	48,000	192,000
K_O	Counts / Volt • Sec	6500	32,500	65,000
K_C	Radians / Count	3.835×10^{-4}	3.835×10^{-4}	3.835×10^{-4}
K_1	Volts / Radian	763	3852	7702
T_1	ms	50	10	5
T_2	ms	5	1.0	0.5
K_OK_C	Radians / Volt • Sec	2.49	12.46	24.93

TABLE 1 Transfer Function Parameters (Typical Values)

For better understanding of the dynamics of the 1024, Bode plots for converter gain and output phase for 60-Hz, 400-Hz and 800-Hz options are shown in Figures 21 and 22.

Results of actual performance of step responses for both large and small signal inputs performed on typical converters are shown in Figure 23.



$$\text{POSITION GAIN (OPEN LOOP)} \quad \frac{\Phi_{OUT}}{\theta_{IN}} = \frac{K_A(T_1 s + 1)}{s^2(T_2 s + 1)}$$

$$\text{POSITION GAIN (CLOSED LOOP)} \quad \frac{\Phi_{OUT}}{\theta_{IN}} = \frac{T_2 s + 1}{\frac{T_2 s^3}{K_A} + \frac{s^2}{K_A} + T_1 s + 1}$$

$$\text{VELOCITY GAIN (OPEN LOOP)} \quad \frac{\dot{\Phi}_{OUT}}{\theta_{IN}} = \frac{K_1(T_1 s + 1)}{s(T_2 s + 1)}$$

$$\text{VELOCITY GAIN (CLOSED LOOP)} \quad \frac{\dot{\Phi}_{OUT}}{\theta_{IN}} = \frac{T_1 s^2 + s}{\frac{T_2 s^3}{K_1} + \frac{s^2}{K_1} + T_1 K_O K_C s + K_O K_C}$$

FIGURE 20 Detailed Transfer Function Model

Bode Plots

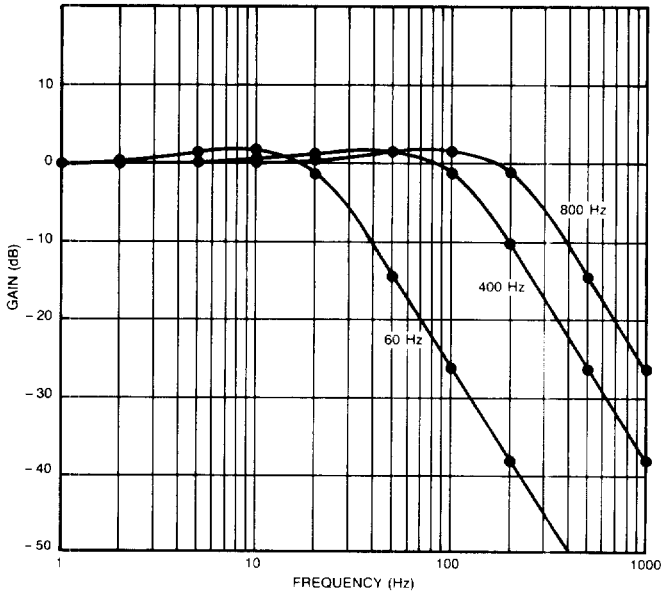


FIGURE 21 Gain Plot (Converter Gain Vs Frequency)

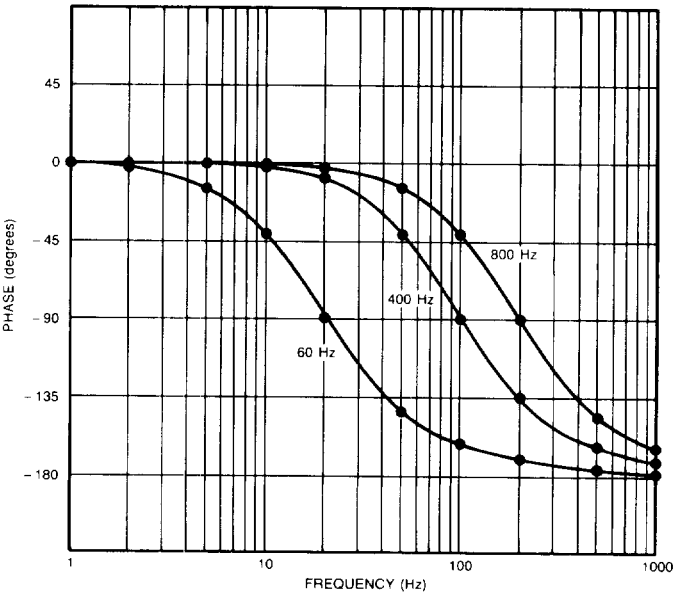
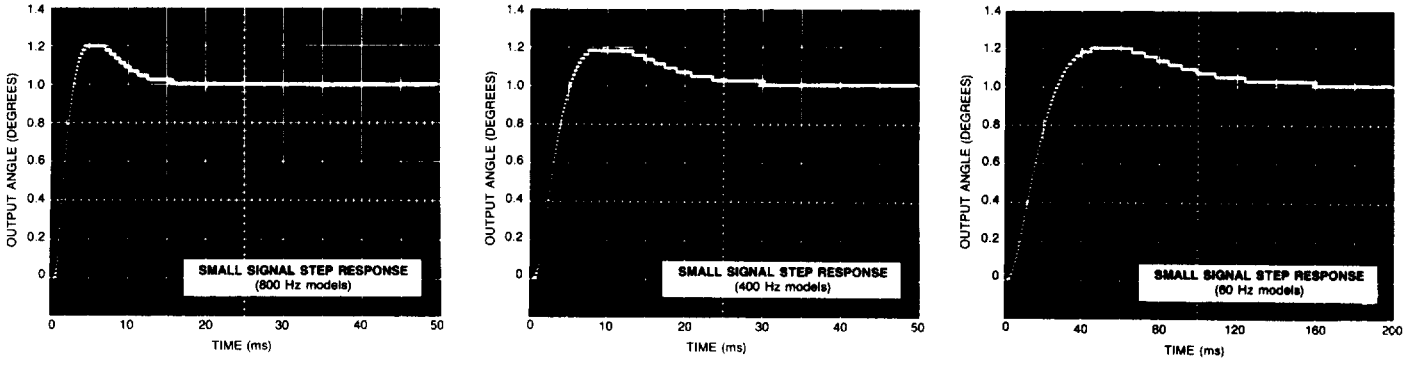


FIGURE 22 Phase Plot (Output Phase Vs Frequency)

Step Response

Main Power Supply = +15 V-dc, V_L = +5 V-dc, T_a = 25°C

Small Signal Input Step = 1.0 Degree



Large Signal Input Step = 179 Degrees

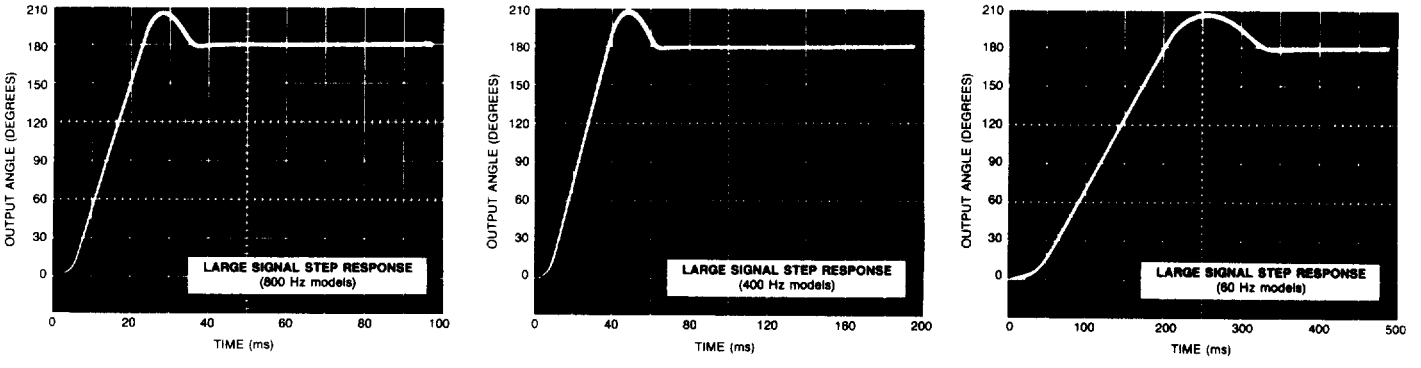


FIGURE 23 Small Signal and Large Signal Step Response

Testing Synchro (Resolver)-to-Digital Converters

All Model 1024 converters are guaranteed to meet the specifications described in the data sheet. All converters are tested per specifications (Pages 8, 9, 10) at the factory. A copy of the data sheet with a record of the accuracy test is supplied with each unit.

Figure 24 shows a convenient test set-up for checking the static accuracy of the converter at incoming inspection. The synchro (resolver) input is set to "test angles." The output is monitored on a 6-digit numerical readout and compared with the standard angles for their accuracy.

Equipment described in figure 24 or equivalent may be used for testing. Synchro (Resolver) standard or simulator used must have an accuracy of at least 5 times (preferably 10 times) better than the unit under test. If the required equipment is not available arrangements may be made with Natel for source inspection at our facilities.

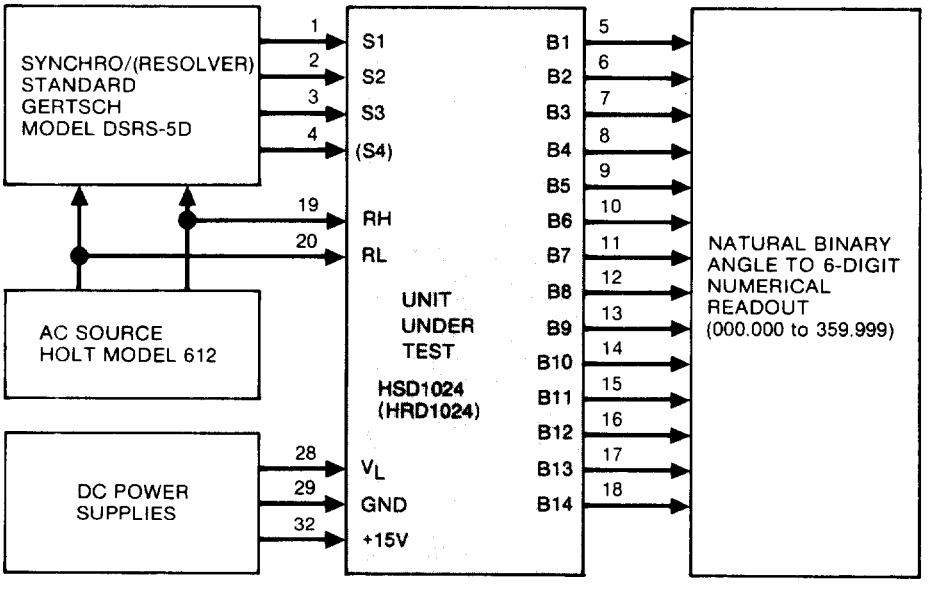
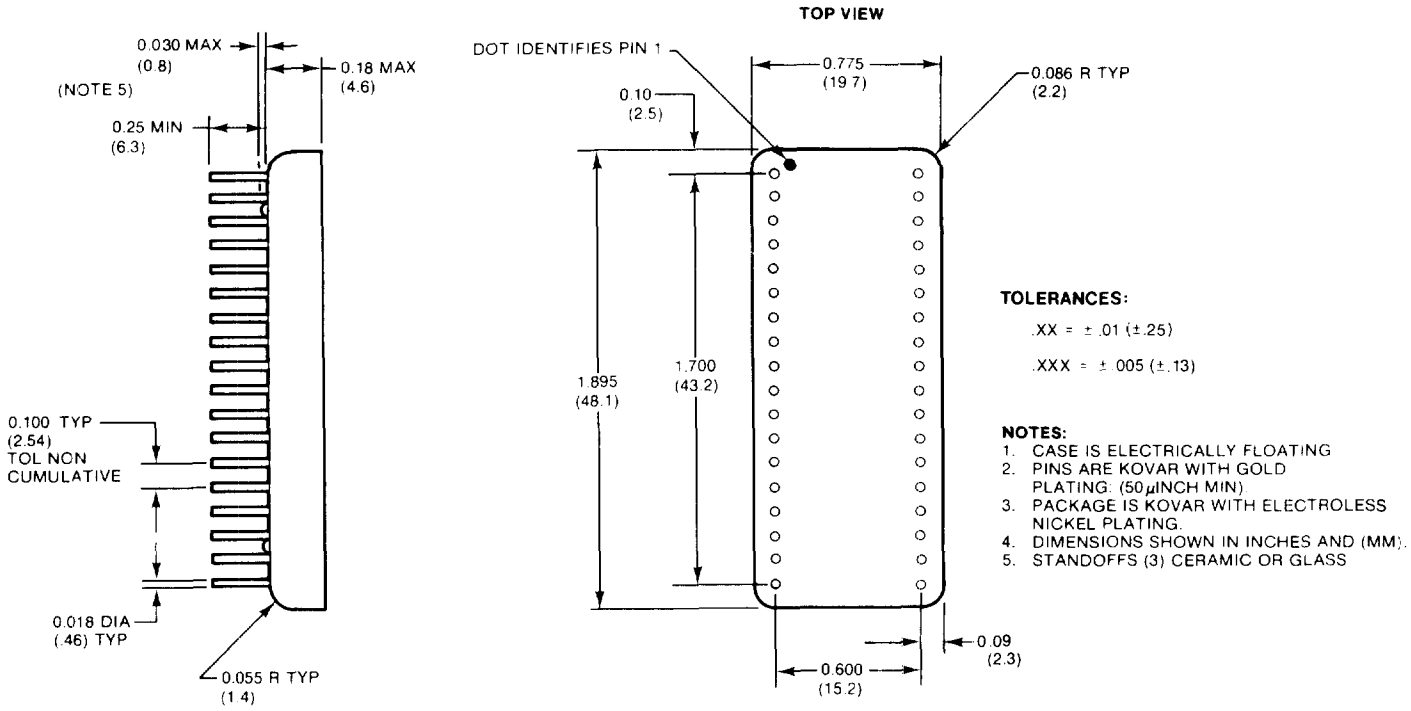


FIGURE 24 Static Accuracy Test Configuration



MECHANICAL OUTLINE (36 PIN DOUBLE DIP)

Ordering Information

HSD1024 - T F I A

Temperature Range
1 = 0° C to + 70° C
2 = −25° C to + 85° C
3 = −55° C to +125° C

Frequency
4 = 400 Hz
6 = 60 Hz
8 = 800 Hz

Input Signal
1 = 11.8 V-rms
2 = 26 V-rms
9 = 90 V-rms
0 = Ext. Signal XFMRS
5 = Ext. Signal and Reference XFMRS

Accuracy
S = ±5.2 arc-minutes
H = ±2.6 arc-minutes

SPECIFY HRD1024 FOR RESOLVER INPUT

MIL-STD-883 COMPLIANT HYBRIDS AVAILABLE
Contact Natel Engineering for Delivery

Other Products Available From NATEL

- Hybrid (36-pin DDIP size) Synchro (Resolver)-to-Digital converters with 10- to 16-bit resolutions (1000 series)
- Second generation Four-Quadrant Multiplying Sin/Cos DAC (HDSC2026)
- Low cost Digital-to-Sin/Cos converter in a ceramic package (HDSC2306)
- 2-channel Digital-to-Sin/Cos converter in a single 36-pin hybrid (HDSC2036)
- 2 VA output, Digital to Resolver Converter in a 32-pin package (HDR2116)
- Resolver Control Differential Transmitter in a single 36-pin package (HCDX3106)
- 22-bit Binary-to-BCD and BCD-to-Binary converters (SBD227 and SDB724)

A wide range of applications assistance is available from Natel. Application Notes can be requested when available . . . and Natel's applications engineers are at your disposal for solving specific problems.

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