4MX1 Bit CMOS Dynamic RAM with Static Column Mode

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM41C4002A- 7	70ns	20ns	130ns
KM41C4002A- 8	80ns	20ns	150ns
KM41C4002A-10	100ns	25ns	180ns

- **Static Column Mode operation**
- **$\overline{CS}$-before-$\overline{RAS}$ Refresh Capability**
- **$\overline{RAS}$-only and Hidden Refresh Capability**
- **8-bit fast parallel test mode Capability**
- **TTL compatible inputs and output**
- **Common I/O using Early Write**
- **Single +5V±10% power supply**
- **1024 cycles/16ms refresh**
- **JEDEC standard pinout**
- **Available in Plastic SOJ, DIP, ZIP**

GENERAL DESCRIPTION

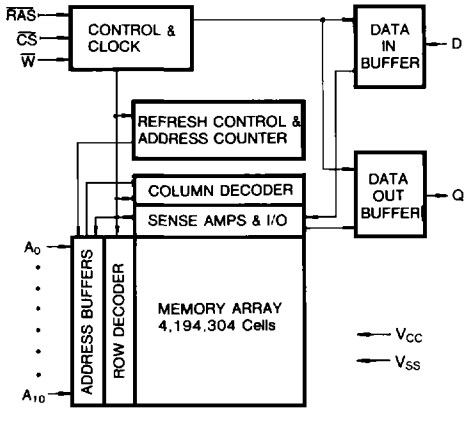
The Samsung KM41C4002A is a high speed CMOS 4,194,304 bit X 1 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes and mini computers, graphics and high performance microprocessor systems.

The KM41C4002A features Static Column Mode operation which allows high speed random or sequential access within a row. Static Column Mode operation offers high performance while relaxing many critical system timing requirements for fast usable speed.

$\overline{CS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and output are fully TTL compatible.

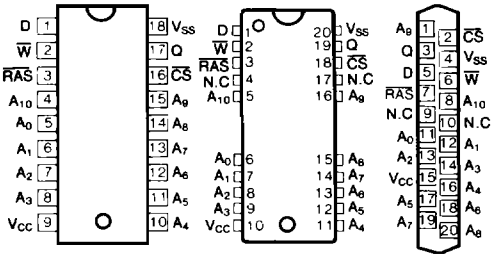
The KM41C4002A is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top Views)

- **KM41C4002AP** - **KM41C4002AJ** - **KM41C4002AZ**



Pin Name	Pin Function
A0-A10	Address Inputs
D	Data In
Q	Data Out
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CS}$	Chip Select Input
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No connection

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	600	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS ($0°C \leq Ta \leq 70°C$, V_{CC}=5.0V±10%)

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Unit
Operating Current* ($\overline{RAS}$, $\overline{CS}$, Address Cycling @ t_{RC}=min)	KM41C4002A- 7	I_{CC1}	—	105	mA
	KM41C4002A- 8		—	95	mA
	KM41C4002A-10		—	85	mA
Standby Current ($\overline{RAS}$=$\overline{CS}$=V_{IH})		I_{CC2}	—	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{RAS}$ Cycling, $\overline{CS}$=V_{IH}, @ t_{RC}=min)	KM41C4002A- 7	I_{CC3}	—	105	mA
	KM41C4002A- 8		—	95	mA
	KM41C4002A-10		—	85	mA
Static Column Mode Current* ($\overline{RAS}$=$\overline{CS}$=V_{IL}, Address Cycling @t_{SC}=min)	KM41C4002A- 7	I_{CC4}	—	80	mA
	KM41C4002A- 8		—	70	mA
	KM41C4002A-10		—	60	mA
Standby Current ($\overline{RAS}$=$\overline{CS}$=$\overline{W}$≥V_{CC}-0.2V)		I_{CC5}	—	1	mA
$\overline{CS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CS}$ Cycling @ t_{RC}=min.)	KM41C4002A- 7	I_{CC6}	—	105	mA
	KM41C4002A- 8		—	95	mA
	KM41C4002A-10		—	85	mA
Standby Current ($\overline{RAS}$=V_{IH}, $\overline{CS}$=V_{IL}, D_{OUT}=Enable)		I_{CC7}	—	5	mA
Input Leakage Current (Any input 0≤V_{IN}≤6.5V, all other pins not under test=0 volts.)		I_{IL}	−10	10	μA
Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤5.5V)		I_{OL}	−10	10	μA
Output High Voltage Level (I_{OH}=−5mA)		V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL}=4.2mA)		V_{OL}	—	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} are dependent on output loading and cycle rates. Specified value are obtained with the output open. I_{CC} is specified as average current.I_{CC1}, I_{CC3}, I_{CC6}, Address can be changed maximum two times while $\overline{RAS}$=V_{IL}. I_{CC4}, Address can be changed maximum once while $\overline{CS}$=V_{IH}.

CAPACITANCE (T_A=25°C)

Item	Symbol	Min	Max	Unit
Input Capacitance (A_0-A_{10}, D)	C_{IN1}	—	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CS}$, $\overline{W}$)	C_{IN2}	—	7	pF
Output Capacitance (Q)	C_{OUT}	—	7	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC}=5.0V±10%, See notes 1,2)

Standard Operation	Symbol	KM41C4002A-7		KM41C4002A-8		KM41C4002A-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	130		150		180		ns	
Read-modify-write cycle time	t_{RWC}	155		175		210		ns	
Access time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	3,4,11
Access time from $\overline{CS}$	t_{CAC}		20		20		25	ns	3,4,5
Access time from column address	t_{AA}		35		40		50	ns	3,11
$\overline{CS}$ to output in Low-Z	t_{CLZ}	5		5		5		ns	3,12
Output buffer turn-off delay	t_{OFF}	0	15	0	15	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
$\overline{CS}$ hold time	t_{CSH}	70		80		100		ns	
$\overline{CS}$ pulse width	t_{CS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ to $\overline{CS}$ delay time	t_{RCD}	20	50	20	60	25	75	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	20	50	ns	11
$\overline{CS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		10		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		15		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		20		ns	
Column address hold referenced to $\overline{RAS}$	t_{AR}	55		60		75		ns	
Column Address to $\overline{RAS}$ lead time	t_{RAL}	35		40		50		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold referenced to $\overline{CS}$	t_{RCH}	0		0		0		ns	9
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	15		15		20		ns	
Write command hold referenced to $\overline{RAS}$	t_{WCR}	55		60		75		ns	6
Write command pulse width	t_{WP}	15		15		20		ns	

AC CHARACTERISTICS (Continued)

Standard Operation	Symbol	KM41C4002A-7		KM41C4002A-8		KM41C4002A-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		25		ns	
Write command to $\overline{CS}$ lead time	t_{CWL}	20		20		25		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	10
Data-in hold time	t_{DH}	15		15		20		ns	10
Data-in hold referenced to $\overline{RAS}$	t_{DHR}	55		60		75		ns	6
Refresh period (1024 cycles)	t_{REF}		16		16		16	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CS}$ to write enable delay time	t_{CWD}	20		20		25		ns	8
$\overline{RAS}$ to write enable delay time	t_{RWD}	70		80		100		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	35		40		50		ns	8
$\overline{CS}$ set-up time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{CSR}	10		10		10		ns	
$\overline{CS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{CHR}	20		30		30		ns	
$\overline{RAS}$ precharge to $\overline{CS}$ hold time	t_{RPC}	10		10		10		ns	
$\overline{CS}$ precharge ($\overline{C}$-B-$\overline{R}$ counter test)	t_{CPT}	35		40		50		ns	
Static column mode cycle time	t_{SC}	40		45		55		ns	
Static column mode read-write cycle time	t_{SRWC}	70		80		100		ns	
Access time from last write	t_{ALW}		65		75		95	ns	3,12
Output data hold time from column address	t_{AOH}	5		5		5		ns	
Output data enable time from $\overline{W}$	t_{OW}		45		50		70	ns	
Output data hold time from $\overline{W}$	t_{WOH}	0		0		0		ns	
$\overline{RAS}$ pulse width (static column mode)	t_{RASC}	70	100,000	80	100,000	100	100,000	ns	
$\overline{CS}$ pulse width (static column mode)	t_{CSC}	20	100,000	20	100,000	25	100,000	ns	
$\overline{CS}$ precharge time (static column mode)	t_{CP}	10		10		10		ns	
Write address hold time reference to $\overline{RAS}$	t_{AWR}	55		60		75		ns	6
Column address hold time referenced to $\overline{RAS}$ rise	t_{AH}	5		5		10		ns	
Last write to column address delay time	t_{LWAD}	20	30	20	35	25	45	ns	
Last write to column address hold time	t_{AHLW}	65		75		95		ns	
Write command inactive time	t_{WI}	10		10		10		ns	
Write command set-up time (Test mode In)	t_{WTS}	10		10		10		ns	
Write command hold time (Test mode In)	t_{WTH}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRP}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRH}	10		10		10		ns	

TEST MODE CYCLE

(Note. 13)

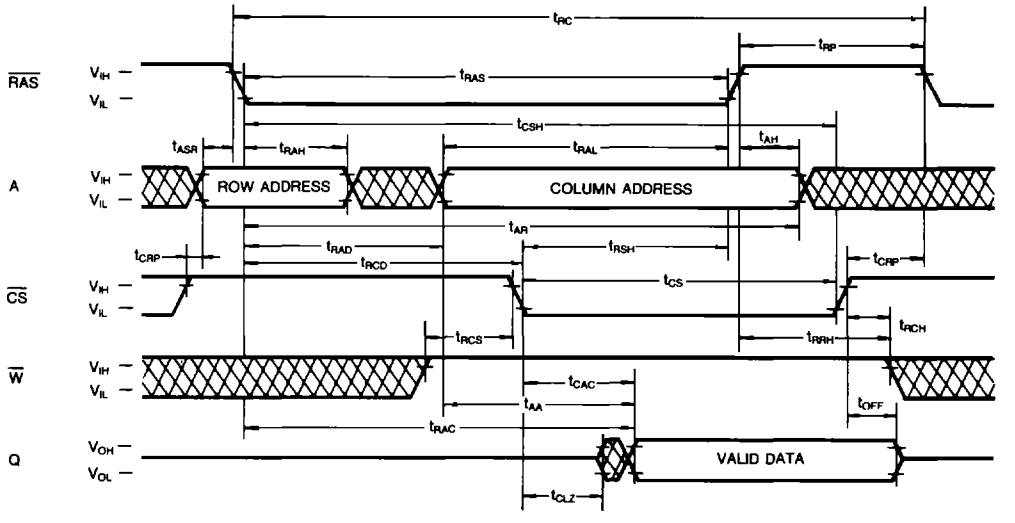
Standard Operation	Symbol	KM41C4002A-7		KM41C4002A-8		KM41C4002A-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	135		155		185		ns	
Read-modify-write cycle time	t_{RWC}	160		180		215		ns	
Access time from $\overline{RAS}$	t_{RAC}		75		85		105	ns	3,4,11
Access time from $\overline{CS}$	t_{CAC}		25		25		30	ns	3,4,5
Access time from column address	t_{AA}		40		45		55	ns	3,11
$\overline{RAS}$ pulse width	t_{RAS}	75	10,000	85	10,000	105	10,000	ns	
$\overline{CS}$ pulse width	t_{CS}	25	10,000	25	10,000	30	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	25		25		30		ns	
$\overline{CS}$ hold time	t_{CSH}	75		85		105		ns	
Column Address to $\overline{RAS}$ lead time	t_{RAL}	40		45		55		ns	
$\overline{CS}$ to write enable delay	t_{CWD}	25		25		30		ns	8
$\overline{RAS}$ to write enable delay	t_{RWD}	75		85		105		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	40		45		55		ns	8
Static column mode cycle time	t_{SC}	45		50		60		ns	
Static column mode read-modefy-write	t_{SRWC}	75		85		105		ns	
$\overline{RAS}$ pulse width (Static column mode)	t_{RASC}	75	100,000	85	100,000	105	100,000	ns	
Access time from last write	t_{ALW}		70		80		100	ns	3,12
$\overline{CS}$ pulse width (static column mode)	t_{CSC}	25	100,000	25	100,000	30	100,000	ns	

NOTES

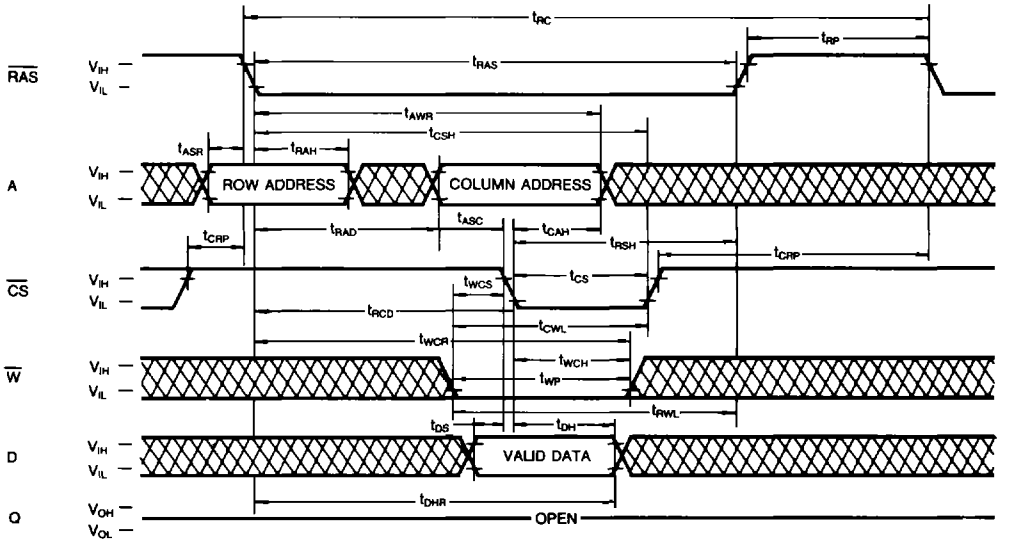
1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycle before proper device operation is achieved.
2. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$, and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF
4. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD(max)}$.
6. t_{AWR}, t_{WCR}, t_{DHR} are referenced to $t_{RAD(max)}$
7. This parameter defines the time at which the output achieves the open circuit condition and is not refernced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD(min)}$ and $t_{RWD} \geq t_{RWD(min)}$ and $t_{AWD} \geq t_{AWD(min)}$, then the cycle is a read-write cycle and the data out will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the $t_{RAD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit, then access time is controlled by t_{AA}.
12. Operation within the $t_{LWAD(max)}$ limit insures that $t_{ALW(max)}$ can be met. $t_{LWAD(max)}$ is specified as a reference point only. t_{LWAD} is greater than the specified $t_{LWAD(max)}$ limit, then access time is controlled by t_{AA}.
13. These specifications are applied in the test mode.

TIMING DIAGRAMS

READ CYCLE



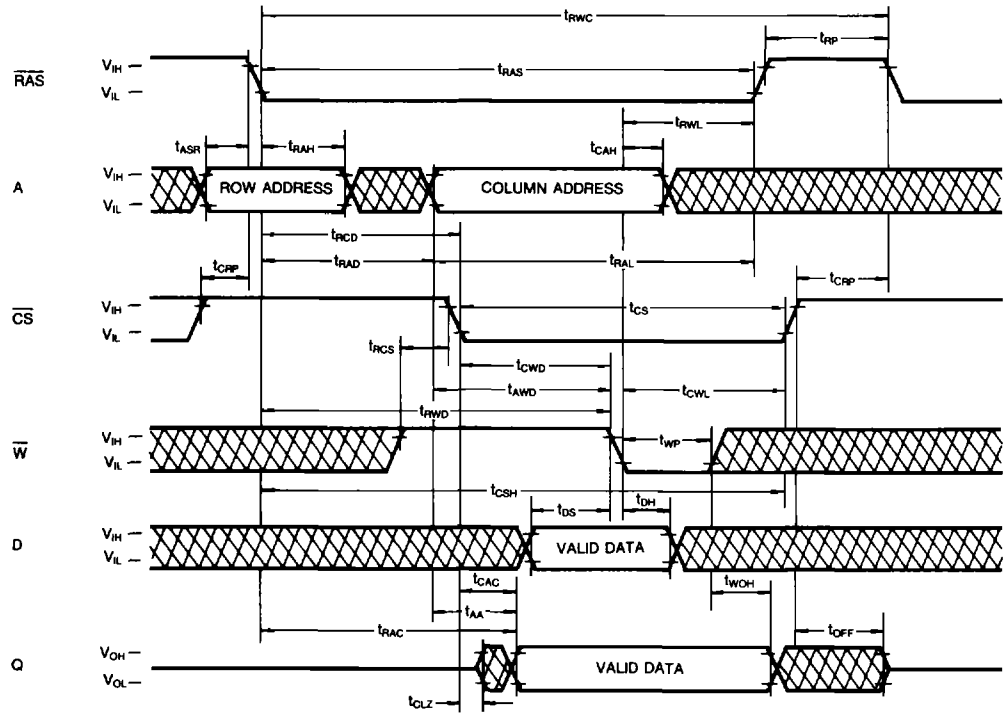
WRITE CYCLE (EARLY WRITE)



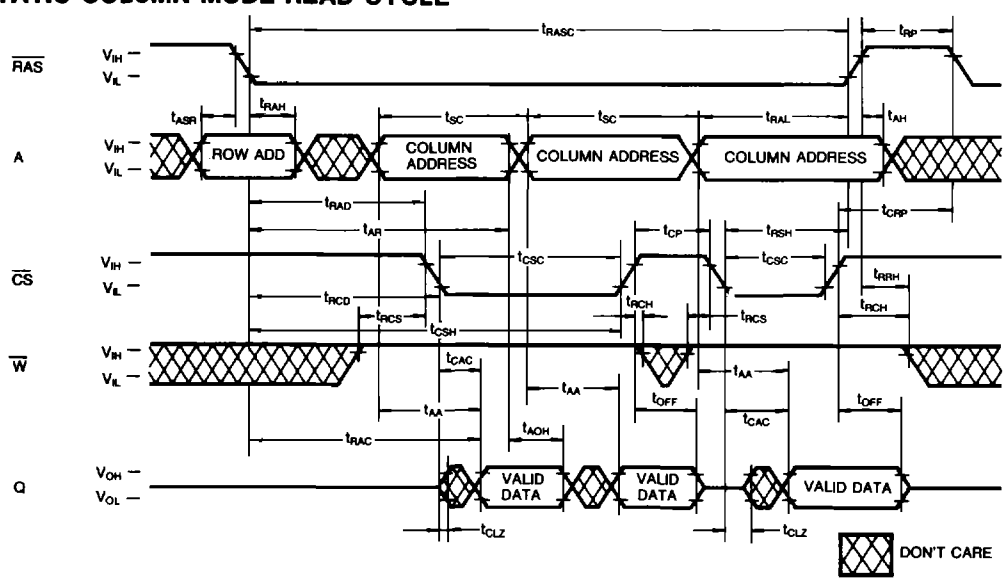
DON'T CARE

TIMING DIAGRAMS (Continued)

READ-WRITE/READ-MODIFY-WRITE CYCLE

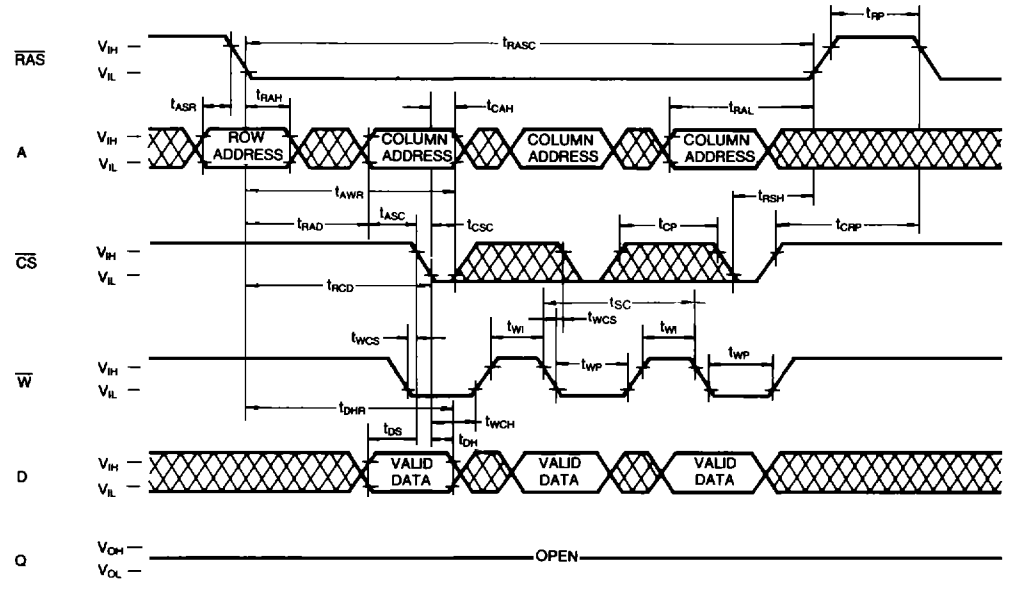


STATIC COLUMN MODE READ CYCLE

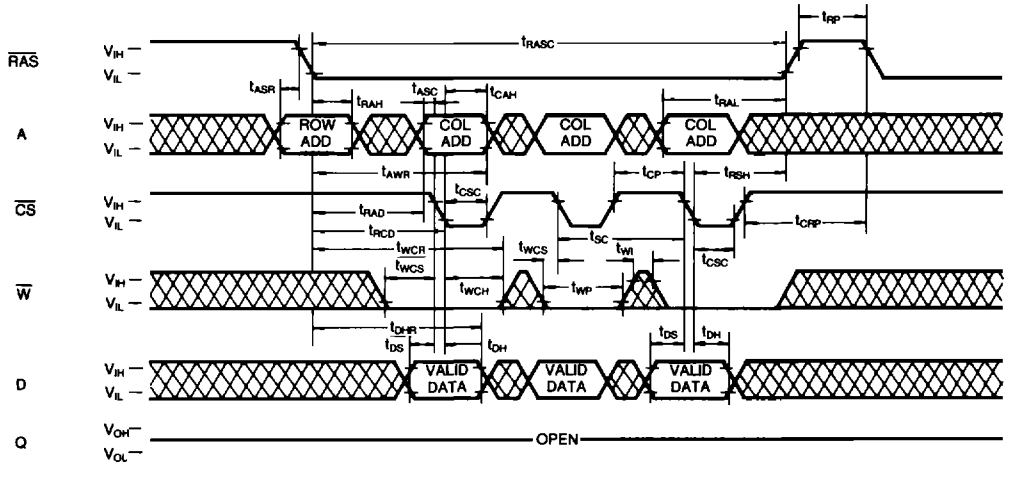


TIMING DIAGRAMS (Continued)

STATIC COLUMN MODE WRITE CYCLE ($\overline{W}$ CONTROLLED EARLY WRITE)



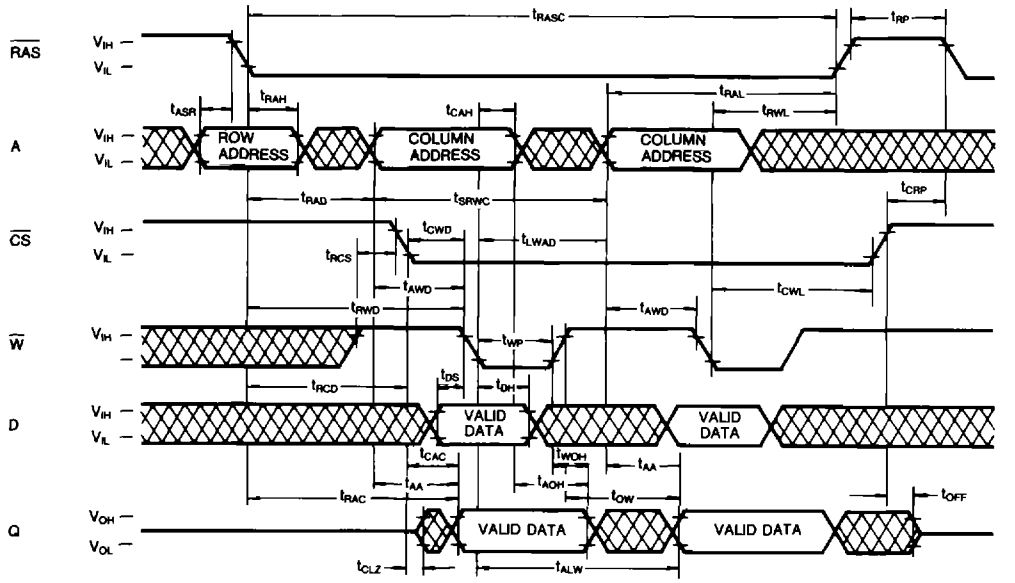
STATIC COLUMN MODE WRITE CYCLE ($\overline{CS}$ CONTROLLED EARLY WRITE)



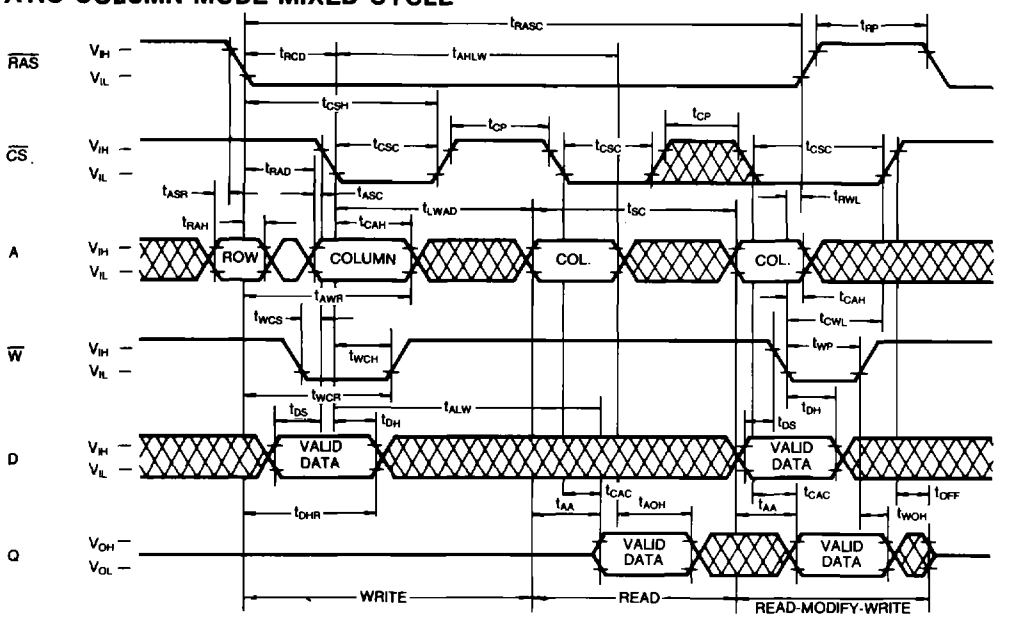
DON'T CARE

TIMING DIAGRAMS (Continued)

STATIC COLUMN MODE READ-WRITE CYCLE



STATIC COLUMN MODE MIXED CYCLE

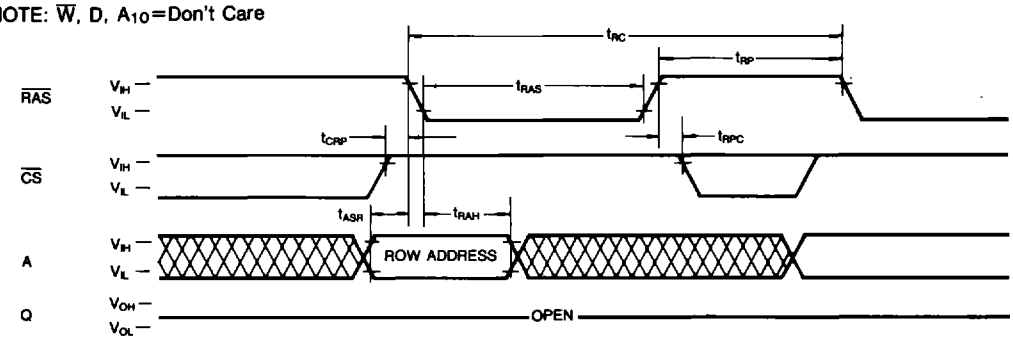


DONT'T CARE

TIMING DIAGRAMS (Continued)

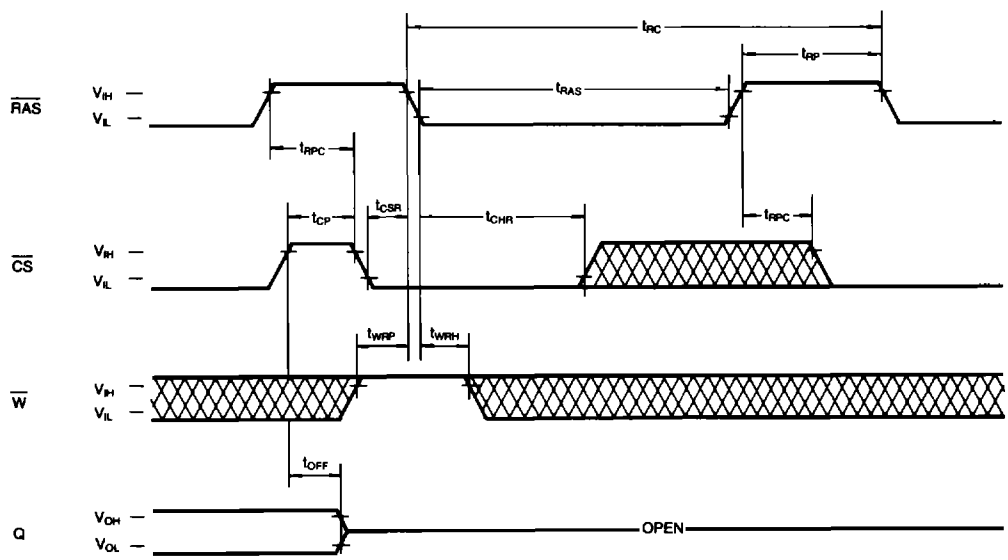
$\overline{RAS}$-ONLY REFRESH CYCLE

NOTE: $\overline{W}$, D, A_{10}=Don't Care



$\overline{CS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

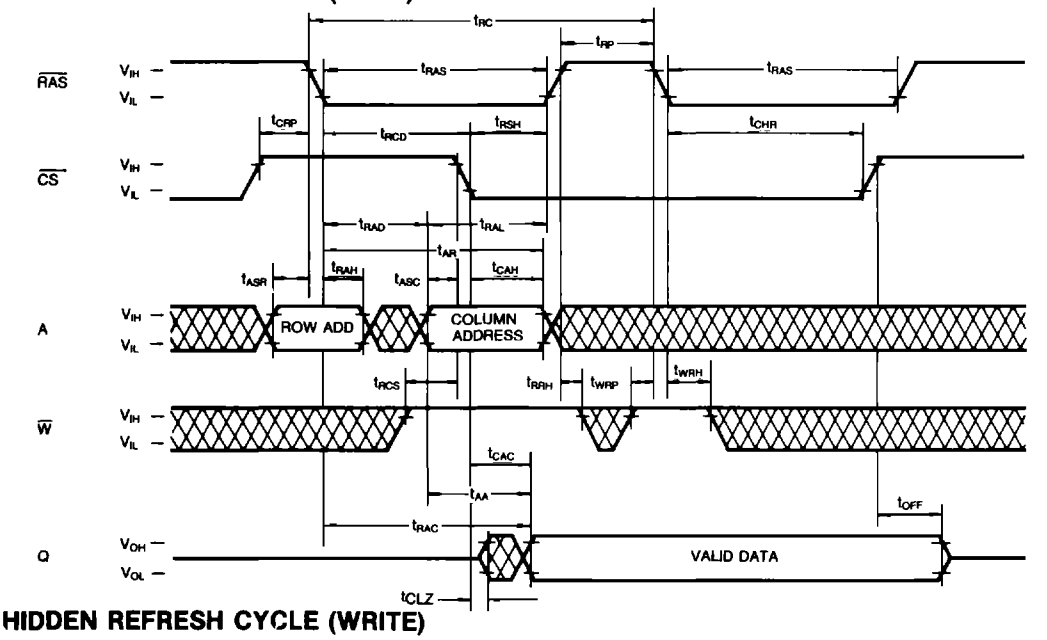
NOTE: Address=Don't Care



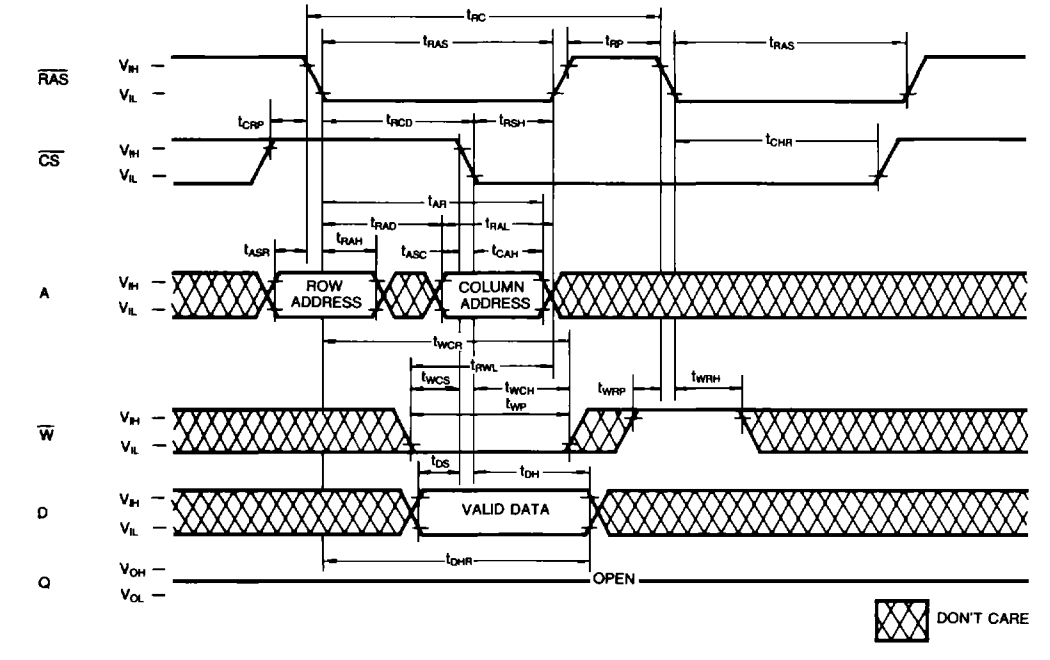
DON'T CARE

TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

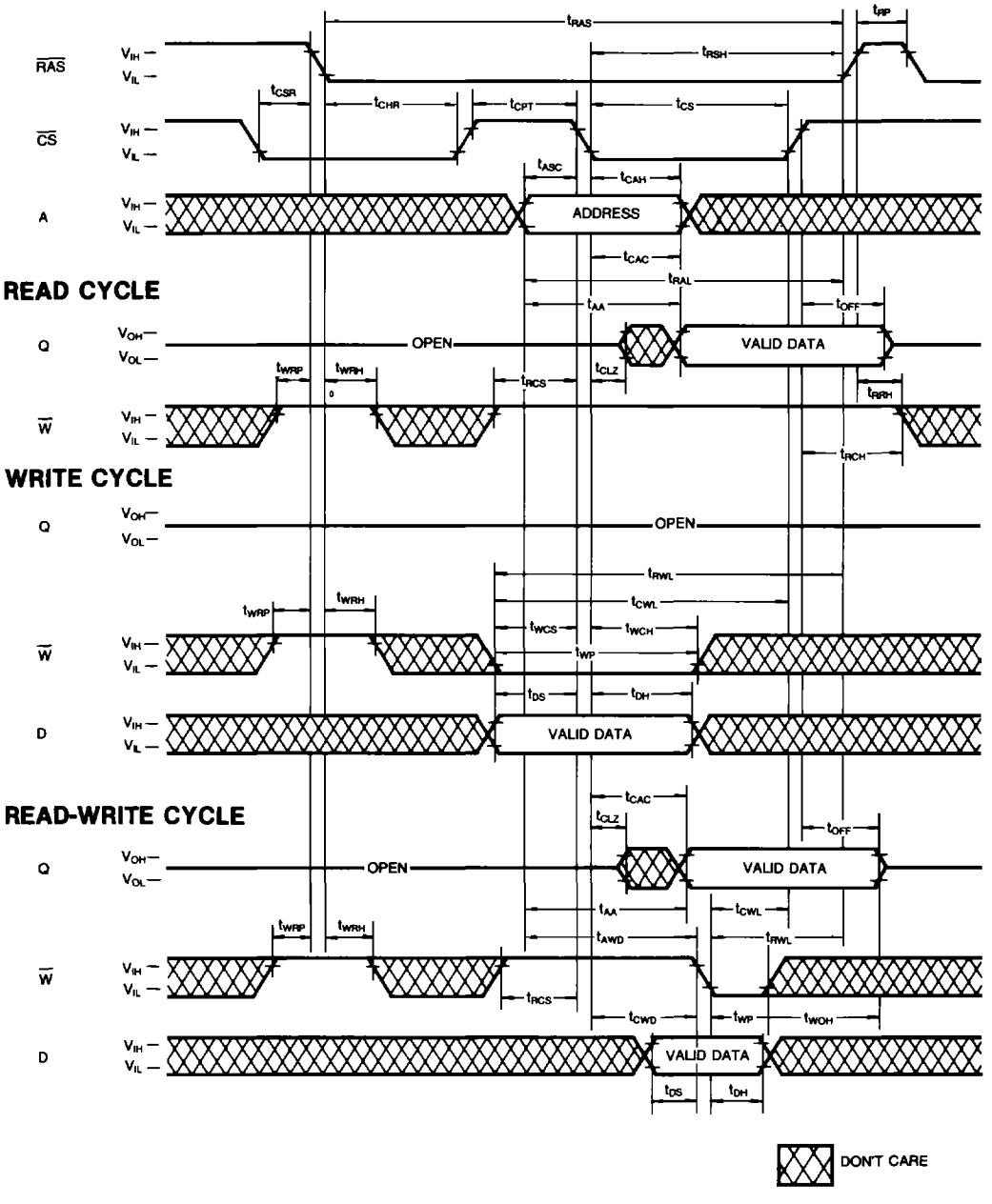


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

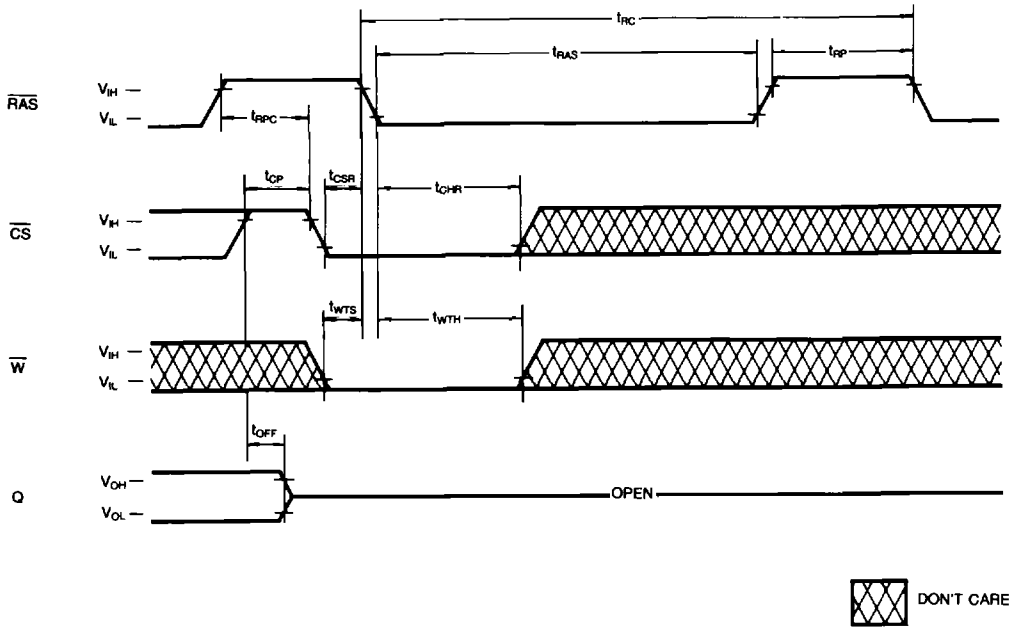
$\overline{CS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

NOTE: D, Address=Don't Care



TEST MODE DESCRIPTION

The KM41C4002A is the RAM organized 4,194,304 words by 1 bit, it is internally organized 524,288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. A_{10R}. A_{10C} and A_{0C} are not used. If, upon reading, all bits are equal (all "1"s or "0"s), the data output pin indicates a "1". If any of the bits differed, the data output pin would indicate a "0" In "Test Mode", the 4M DRAM can be tested as if it were a 512K DRAM. $\overline{W}$, $\overline{CS}$ Before $\overline{RAS}$ Cycle (Test Mode in Cycle) puts the device into "Test Mode". And "$\overline{CS}$ Before $\overline{RAS}$ Refresh Cycle" or "$\overline{RAS}$ only Refresh Cycle" puts it back into "Normal Mode". The "Test Mode" function reduces test time (1/8 in cases of N test pattern).

DEVICE OPERATIONS

Device Operation

The KM41C4002A contains 4,194,304 memory locations. Twenty-two address bits are required to address a particular memory location. Since the KM41C4002A has only 11 address input pins, time multiplexed addressing is used to input 11 row and 11 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the chip select input ($\overline{CS}$) and the valid row and column address inputs.

Operating of the KM41C4002A begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CS}$ remains high. Then the address on the 11 address input pins is changed from a row address to a column address and is strobed in by $\overline{CS}$. This is the beginning of any KM41C4002A cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CS}$ pulse widths are specified by t_{RAS}(min) and t_{CS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM41C4002A begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input($\overline{W}$) high during a $\overline{RAS}$/$\overline{CS}$ cycle. The access time is normally specified with respect to the falling edge of $\overline{RAS}$. But the access time also depends on the falling edge of $\overline{CS}$ and on the valid column address transition.

If $\overline{CS}$ goes low before t_{RCD}(max) and if the column address is valid before t_{RAD}(max) then the access time to valid data is specified by t_{RAC}(min). However, if $\overline{CS}$ goes low after t_{RCD}(max) or if the column address becomes valid after t_{RAD}(max), access is specified by t_{CAC} or t_{AA}. In order to achieve the minimum access time, t_{RAC}(min), it is necessary to meet both t_{RCD}(max) and t_{RAD}(max).

Write

The KM41C4002A can perform early write, late write and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$ and $\overline{CS}$. In any type of write cycle, Date-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before $\overline{CS}$. The data at the data input pin(D) is written into the addressed memory cell. Throughout the early write cycle the output remains in the Hi-Z state. This cycle is good for common I/O applications because the data-in and data-out pins may be tied together without bus contention.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CS}$ and meeting the data sheet read-modify-write cycle timing requirements. This cycle requires using a separate I/O to avoid bus contention.

Late Write: If $\overline{W}$ is brought low after $\overline{CS}$, a late write cycle will occur. The late write cycle is very similar to the read-modify-write cycle except that the timing parameters, t_{RWD}, t_{CWD} and t_{AWD}, are not necessarily met. The state of date-out is indeterminate since the output can be either Hi-Z or contain data depending on the timing conditions. This cycle requires a separate I/O to avoid bus contention.

Data Output

The KM41C4002A has a three-state output buffer which is controlled by $\overline{CS}$. Whenever $\overline{CS}$ is high (V_{IH}) the output is in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the output the output goes into the low impedance state in a time specified by t_{CLZ} after the falling edge of $\overline{CS}$. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC} and t_{AA} specify when the valid data will be present at the output. The valid data remains at the output until $\overline{CS}$ returns high. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM41C4002A operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Static Column Mode Read, Static Column Mode Read-Modify-Write.

Hi-Z Output Static: Early Write, $\overline{RAS}$-only Refresh, Static Column Mode Write, $\overline{CS}$-Before-$\overline{RAS}$ Refresh, $\overline{CS}$-only cycle.
Indeterminate Output State: Delayed Write.

DEVICE OPERATIONS (Continued)

Refresh

The data in the KM41C4002A is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 16 ms. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CS}$ remains high. This cycle must be repeated for each row.

$\overline{CS}$-before-$\overline{RAS}$ Refresh: The KM41C4002A has $\overline{CS}$-before-$\overline{RAS}$ on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CS}$ is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ goes low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CS}$ active time and cy^ling $\overline{RAS}$. The KM41C4002A hidden refresh cycle is actually a $\overline{CS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM41C4002A by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CS}$-before-$\overline{RAS}$ refresh is the preferred method.

Static Column Mode

Static Column Mode allows high speed read, write or read-modity-write random access to all the memory cells within a selected row. Operation within a selected row is similar to a static RAM. The read, write or readmodify-write cycles may be mixed in any order.

A Static Column mode read cycle starts as a normal cycle. Additional cells within the selected row are written by by applying a new column address while $\overline{W}=V_{IH}$ and $\overline{RAS}=V_{IL}$.

A Static Column mode write cycle starts as a normal cycle. Additional cells within the selected row are written by applying a new column address while $\overline{RAS}=V_{IL}$ and toggiling either $\overline{W}$ or $\overline{CS}$. The data is written into the cell trigered by the latter fallin edge of $\overline{W}$ or $\overline{CS}$.

$\overline{CS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CS}$-before-$\overline{RAS}$ refresh counter test cycle provides a convenient method of verifying the functionality of the $\overline{CS}$-before-$\overline{RAS}$ refresh activated circuitry.

After the $\overline{CS}$-before-$\overline{RAS}$ refresh operation, is $\overline{CS}$ goes high and then low again while RAS is held low, the read and write operations are enabled.

This is shown in the $\overline{CS}$-before-$\overline{RAS}$ counter test cycle timing diagram. A memory cell can be addressed with 11 row address bits and 11 column address bits defined as follows:

Row Address—Bits A_0 through A_9 are supplied by the on-chip refresh counter. The A_{10} bit is set high internally.

Column Address—Bits A_0 through A_{10} are strobed-in by the falling edge of $\overline{CS}$ as in a normal memory cycle.

Suggested $\overline{CS}$-before-$\overline{RAS}$ Counter Test Procedure

The $\overline{CS}$-before-$\overline{RAS}$ refresh counter test cycle timing is used in each of the following steps:

1. Initialize the internal refresh counter by performing 8 cycles.
2. Write a test pattern of "lows" into the memory cells at a single column address and 1024 row address. (The row addresses are supplied by the on-chip refresh counter).
3. Using read-modify-write cycles, read the "lows" written during step 2 and write "highs" into the same memory locations. Perform this step 512 times so that highs are written into the 512 memory cells.
4. Read the "highs" written during step 3.
5. Complement the test pattern and repeat steps 2, 3 and 4.

Power-up

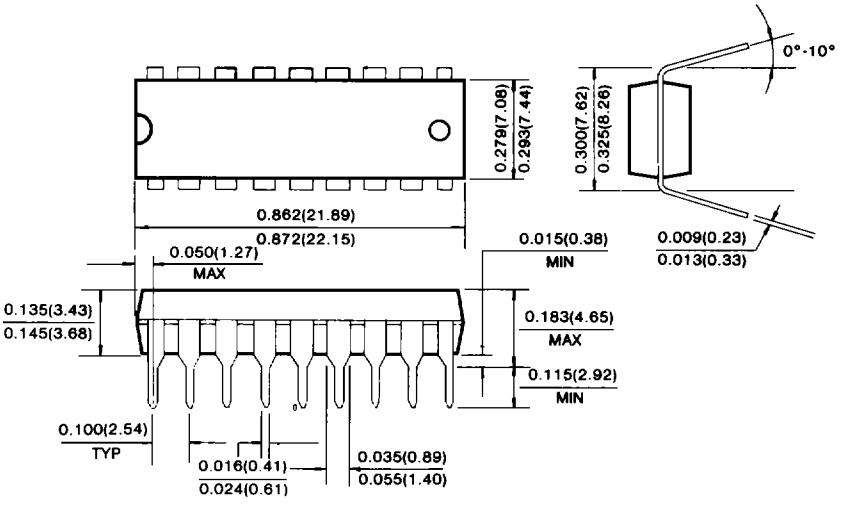
If $\overline{RAS}=V_{SS}$ during power-up, the KM41C4002A could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CS}$ track with V_{CC} during power-up or be held at a valid V_{IH} in order to minimize the power-up current.

An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.

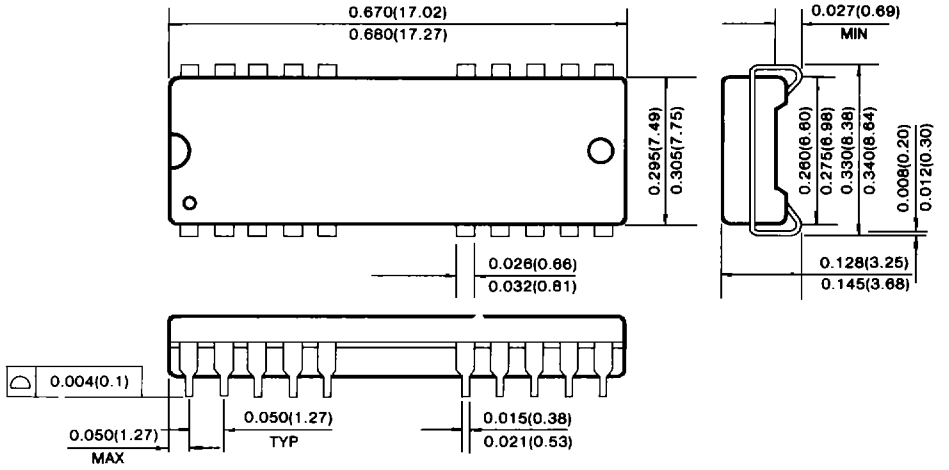
PACKAGE DIMENSIONS

18-LEAD PLASTIC DUAL IN-LINE PACKAGE

Unit: Inches (Millimeters)



20-LEAD PLASTIC SMALL OUT-LINE J-LEAD



PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE

Units: Inches (millimeters)