GENERAL DESCRIPTION

The M2004 variants -22, -32, -42, and -52 are VCSO (Voltage Controlled SAW Oscillator) based clock generator PLLs designed for clock frequency translation and jitter attenuation in a high-speed data communications system. The clock multiplication ratio and output divider ratio are pin selectable. External loop components allow the tailoring of PLL loop response. Based on the M2004-02, these device variants add the Hitless Switching with Phase Build-out (HS/PBO) feature. HS/PBO ensures that reference clock reselection does not disrupt the output clock. In addition, a fixed Narrow Loop Bandwidth feature (Fixed NBW) is included in the some of the device variants.

FEATURES

- **Pin-compatible with M2004-02/-12, these new product variants offer new functions**
- **Hitless Switching with Phase Build-out to ensure SONET/SDH MTIE and TDEV compliance during reference clock reselection**
- **Fixed Narrow Loop Bandwidth feature available**
- **Ideal for OC-48/192 data clock**
- **Integrated SAW (surface acoustic wave) delay line**
- **VCSO frequency from 300 to 700MHz ****
- **Low phase jitter of < 0.5ps rms, typical (12kHz to 20MHz or 50kHz to 80MHz)**
- **Pin-selectable configuration**
- **Reference clock inputs support differential LVDS, LVPECL, as well as single-ended LVCMOS, LVTTL**
- **Industrial temperature available**
- **Single 3.3V power supply**
- **Small 9 x 9 mm SMT (surface mount) package**

PIN ASSIGNMENT (9 x 9 mm SMT)

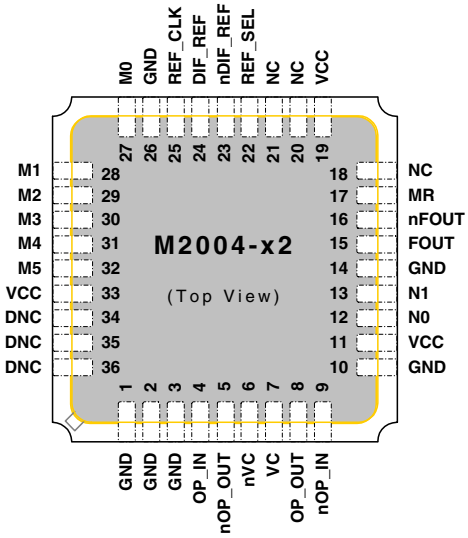

Figure 1: Pin Assignment

Example Input / Output Frequency Combinations

Input (MHz)	VCSO ** (MHz)	Output (MHz)	Application
19.44	622.08	77.76	OC-12 / 48 /192
77.76		311.04	
155.52		622.08	

Table 1: Example Input / Output Frequency Combinations

Device Variants and Corresponding Functions

Variant	Hitless Switching / Phase Build-out Triggered by		Fixed NBW
	Phase Transient	Mux Reselection	
M2004-02	no	no	no
M2004-12	✓ Yes	✓ Yes	no
M2004-22	no	no	✓ Yes
M2004-32	✓ Yes	✓ Yes	✓ Yes
M2004-42	no	✓ Yes	no
M2004-52	no	✓ Yes	✓ Yes

Table 2: Device Variants and Corresponding Functions

* This sheet covers only parts numbered M2004-22, -32, -42, -52.
See M2004-02/-12 Product Data Sheet for M2004-02 & M2004-12.

** Specify VCSO center frequency at time of order.

SIMPLIFIED BLOCK DIAGRAM

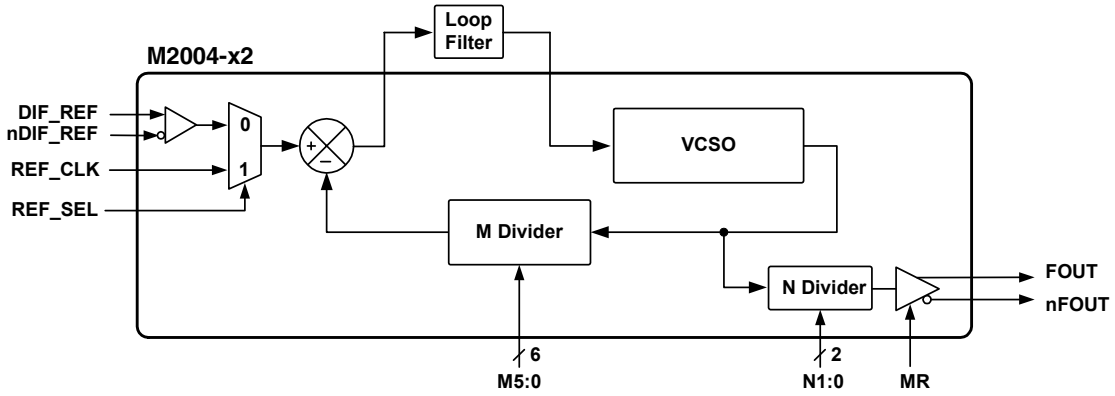

Figure 2: Simplified Block Diagram

PIN DESCRIPTIONS

Number	Name	I/O	Configuration	Description
1, 2, 3, 10, 14, 26	GND	Ground		Power supply ground connections.
4 9	OP_IN nOP_IN	Input		External loop filter connections. See Figure 4, External Loop Filter, on pg. 5.
5 8	nOP_OUT OP_OUT	Output		
6 7	nVC VC	Input		
11, 19, 33	VCC	Power		Power supply connection, connect to +3.3V.
12 13	N0 N1	Input	Internal pull-down resistor[1]	N divider (output divider) inputs N1:N0. LVCMOS/LVTTL. See Table 6, N Divider Pin Selection, on pg. 3.
15 16	FOUT nFOUT	Output	No internal terminator	Clock output pair. Differential LVPECL.
17	MR	Input	Internal pull-down resistor[1]	Reset: Logic 1 resets M and N dividers and forces FOUT to LOW and nFOUT to HIGH. Logic 0 enables the outputs. LVCMOS/LVTTL.
18 20 21	NC NC NC			No connection.
22	REF_SEL	Input	Internal pull-down resistor[1]	Reference clock input selection. LVCMOS/LVTTL. See Table 4, Reference Clock Input Selection, on pg. 3. REF_SEL triggers Hitless Switching (HS/PBO) when toggled.
23	nDIF_REF	Input	Internal pull-UP resistor[1]	Reference clock input pair. Differential LVPECL or LVDS.
24	DIF_REF		Internal pull-down resistor[1]	
25	REF_CLK	Input	Internal pull-down resistor[1]	Reference clock input. LVCMOS/LVTTL.
27 28 29 30 31	M0 M1 M2 M3 M4	Input	Internal pull-down resistor[1]	M divider (feedback divider) inputs M5:M0. See Table 5, M Divider Pin Selection, on pg. 3.
32	M5		Internal pull-UP resistor[1]	
34, 35, 36	DNC			Do Not Connect.

Table 3: Pin Descriptions

Note 1: For typical values of internal pull-down and pull-up resistors, see **DC Characteristics** on pg. 7.

DETAILED BLOCK DIAGRAM

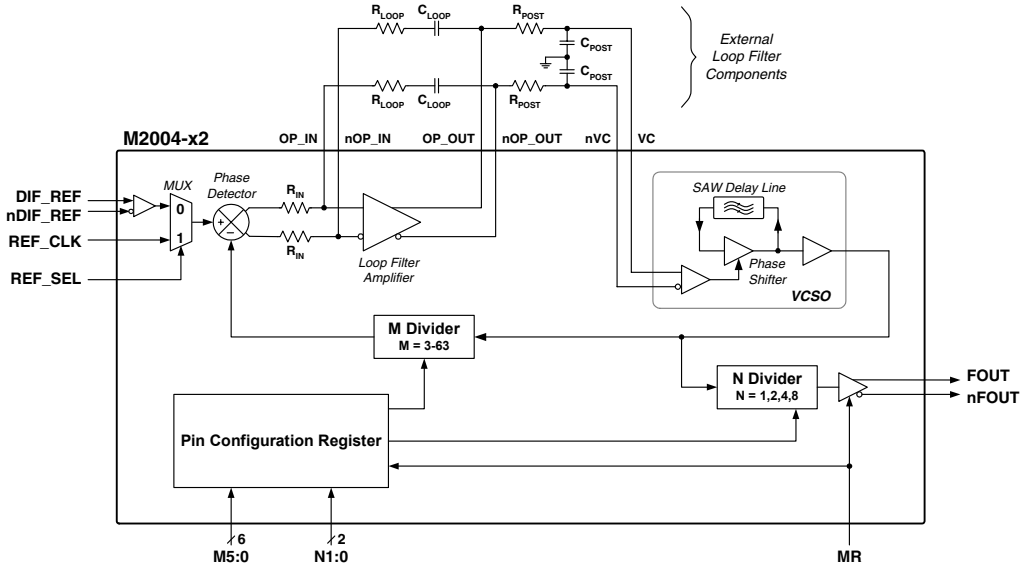

Figure 3: Detailed Block Diagram

PLL DIVIDER SELECTION TABLES

Reference Clock Input Selection

REF_SEL Pin Setting (Pin 22)	Reference Input Selection
0	DIF_REF, nDIF_REF
1	REF_CLK

Table 4: Reference Clock Input Selection

M Divider Pin Selection

M5:0 Pin Settings (Pins 32 - 27) M5 - M0	Definition	Sample Input Clock Freq (MHz) F_{VCSO}= 622.08[1], F_{VCSO}= 625.00[2]	
5[3] 4 3 2 1 0	Feedback Divider Value "M"		
0 0 0 0 1 1	M = 3 minimum		
0 0 0 1 0 0	M = 4	155.52	156.25
⋮			
0 0 1 0 0 0	M = 8	77.76	
⋮			
0 1 0 0 0 0	M = 16	38.80	
⋮			
0 1 1 0 0 1	M = 25		25.00
⋮			
1 0 0 0 0 0	M = 32	19.44	
⋮			
1 1 1 1 1 1	M = 63		

Table 5: M Divider Pin Selection

Note 1: F_{VCSO} = 622.08 MHz (e.g., M2004-22-622.0800)
Note 2: F_{VCSO} = 625.00 MHz (e.g., M2004-22-625.0000)
Note 3: M5 pin has a pull-up resister; M4-M0, pull-down.

N Divider Pin Selection

N1:0 Settings (Pin 13 and 12) N1	N0	N Divider Value	Sample Output Frequency (MHz) [1] (FOUT, nFOUT)
0	0	1	622.08
0	1	2	311.04
1	0	4	155.52
1	1	8	77.76

Table 6: N Divider Pin Selection

Note 1: F_{VCSO} = 622.08MHz (e.g., M2004-22-622.0800)

FUNCTIONAL DESCRIPTION

The M2004-x2 is a PLL (Phase Locked Loop) based clock generator that generates output clocks synchronized to one of two selectable input reference clocks. An internal high “Q” SAW delay line provides a low jitter clock signal.

The device can be pin-configured for feedback divider and output divider values. Output is LVPECL compatible. External loop filter component values set the PLL bandwidth to optimize jitter attenuation characteristics.

The M2004-x2 is ideal for clock jitter attenuation and frequency translation in 2.5 or 10 Gb optical network line card applications.

Added Features and Device Variants

Hitless Switching with Phase Build-out (HS/PBO) provides SONET/SDH MTIE and TDEV compliance during a reference clock reselection when using the internal mux (and also when using an external mux, in two device variants).

A fixed Narrow Loop Bandwidth feature (Fixed NBW) is included in some of the device variants.

All of the variants of the device are defined as follows:

- The M2004-02 is the base variant (it omits both HS/PBO and Fixed NBW).
- The M2004-12 includes HS/PBO triggered by either a phase transient or internal mux reselection.
- The M2004-22 includes HS/PBO – triggered by internal mux reselection only – and Fixed NBW.
- The M2004-32 includes HS/PBO – triggered by either a phase transient or internal mux reselection – and Fixed NBW.
- The M2004-42 includes HS/PBO triggered by internal mux reselection only.
- The M2004-52 includes HS/PBO – triggered by internal mux reselection only – and Fixed NBW.

Device Variants and Corresponding Functions

Variant	Hitless Switching / Phase Build-out Triggered by		Fixed NBW
	Phase Transient	Mux Reselection	
M2004-02	no	no	no
M2004-12	✓ **Yes**	✓ **Yes**	no
M2004-22	no	no	✓ **Yes**
M2004-32	✓ **Yes**	✓ **Yes**	✓ **Yes**
M2004-42	no	✓ **Yes**	no
M2004-52	no	✓ **Yes**	✓ **Yes**

Table 7: Device Variants and Corresponding Functions

Input Reference Clocks

An internal input MUX is provided for input reference clock selection. One input reference clock is selected from between a single-ended LVCMOS / LVTTL clock input or a differential LVPECL or LVDS clock input pair. The maximum input frequency is 175MHz.

PLL Operation

The M2004-x2 is a complete clock PLL. It uses a phase detector and configurable dividers to synchronize the output of the VCSO with the selected reference clock.

The “M Divider” divides the VCSO output frequency, feeding the result into the phase detector. The selected input reference clock is fed into the other input of the phase detector. The phase detector compares its two inputs. It then causes the VCSO to increase or decrease in speed as needed to phase- and frequency-lock the VCSO to the reference input.

The value of M directly affects closed loop bandwidth.

The M Divider

The relationship between the VCSO center frequency (Fvcso), the M divider, and the input reference frequency (Fref_clk) is:

$$Fvcso = Fref\_clk \times M$$

The product of M and the input frequency must be such that it falls within the “lock” range of the VCSO.

See APR in AC Characteristics on pg. 8.

N Divider and Outputs

The M2004-x2 provides one differential LVPECL output pair: FOUT, nFOUT. By using the N divider, the output frequency can be the VCSO center frequency (Fvcso) or 1/2, 1/4, or 1/8 Fvcso.

The N1 and N0 pins select the value for the N divider.

See Table 6, M Divider Pin Selection, on pg. 3.

When the N divider is included, the complete relationship for the output frequency (Fout) is defined as:

$$Fout = \frac{Fvcso}{N} = Fref\_clk \times \frac{M}{N}$$

Configuration of M and N Dividers

The M and N dividers can be set by pin configuration using the input pins M0 - M5, N0, and N1. The data on pins M5:0 and pins N1:0 is passed directly to the M and N dividers.

The divider configuration of the M2004-x2 is reset when the input pin MR is set HIGH. MR is set LOW for divider configuration to be operational.

Hitless Switching and Phase Build-out

A proprietary automatic Hitless Switching (HS) function is included in the M2004-22, M2004-32, M2004-42, and M2004-52. The HS function provides SONET/SDH MTIE and TDEV compliance during a reference clock reselection when using the internal mux. Two variants are additionally triggered by reference clock reselection when using an external mux (through detection of the resulting phase transient).* A Phase Build-out (PBO) function is also incorporated to absorb most of the phase change in the reference clock input.

The combined HS/PBO function is armed after the device locks to the input clock reference. Once armed, HS/PBO is triggered according to device variant as follows:

- In the M2004-22, M2004-42 and M2004-52, HS/PBO is only triggered by changing REF_SEL to switch the input reference clock.
- In the M2004-32, HS/PBO is triggered by either reselection of the input mux or by detection at the phase detector of an input phase transient beyond 4 ns.

Once triggered, the HS function narrows loop bandwidth to control MTIE during locking to the new input phase.** With proper configuration of the external loop filter, the output clocks will comply with MTIE and TDEV specifications for GR-253 (SONET) and ITU G.813 (SDH) during input reference clock changes.

The Phase Build-out (PBO) function enables the PLL to absorb most of the phase change of the input clock. The PBO function selects a new VCSO clock edge for the phase detector feedback clock, selecting the edge closest in phase to the new input clock phase. This reduces re-lock time, the generation of wander, and extra output clock cycles.

When the PLL locks to within 2 ns of the input clock phase, the PLL returns to normal loop bandwidth and the HS/PBO function is re-armed.

* Transient-triggered HS/PBO is not suitable for use with an unstable reference clock that would induce phase jitter beyond 2 ns at the phase detector (e.g., Stratum DPLL clock sources and unstable recovered network clocks intended for loop timing configuration). Therefore, all of the HS/PBO devices offer the internal mux-triggered HS/PBO capability.

** In the M2004-32 and M2004-52, the Fixed NBW function permanently enables narrow bandwidth, therefore PBO is the only actively-triggered function.

External Loop Filter

To provide stable PLL operation, and thereby a low jitter output clock, the M2004-x2 requires the use of an external loop filter components. These are connected to the provided filter pins (see Figure 4). Due to the differential signal path design, the implementation consists of two identical complementary RC filters as shown in Figure 4, below.

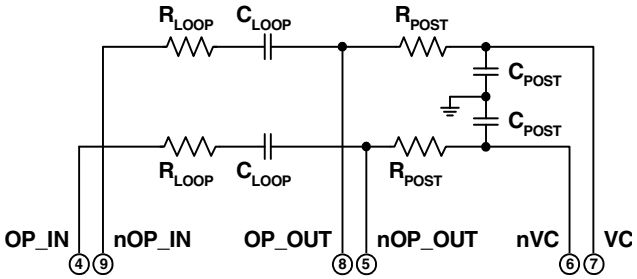

Figure 4: External Loop Filter

PLL bandwidth is affected by the "M" value as well as the VCSO frequency. See Table 8, External Loop Filter Component Values for M2004-42, on pg. 6.

In addition, loop bandwidth is affected by the Fixed Narrow Loop Bandwidth (Fixed NBW) feature. See Table 8, External Loop Filter Component Values for M2004-42, on pg. 6.

Fixed Narrow Loop Bandwidth (Fixed NBW) ***

A fixed Narrow Loop Bandwidth feature (Fixed NBW) is included in the M2004-22, M2004-32, and M2004-52. These device variants have a narrower loop bandwidth than the other variants. The internal resistor Rin is 2016 MΩ, increased from 16 kΩ. This lowers the loop bandwidth by a factor of 125 (2 / 0.016) and lowers the damping factor by a factor of 11.18 (the square root of 125), using the same loop components.

PLL Simulator Tool Available

A free PC software utility is available on the ICS website (www.icst.com). The M2000 Timing Modules PLL Simulator is a downloadable application that simulates PLL jitter and wander transfer characteristics. This enables the user to set appropriate external loop component values in a given application.

*** The M2004-02, M2004-12, and M2004-42 do not include Fixed NBW.

External Loop Filter Component Values for M2004-42[1]

VCSO Parameters: K_{VCO} = 800kHz/V, R_{IN} = 16kΩ, VCSO Bandwidth = 700kHz. See AC Characteristics on pg. 8 for PLL Loop Constants.

Device Configuration			Example External Loop Filter Component Values				Nominal Performance Using These Values		
F_{Ref} (MHz)	**F_{VCSO} (MHz)**	**M Divider Value**	**R loop**	**C loop**	**R post**	**C post**	**PLL Loop Bandwidth**	**Damping Factor**	**Passband Peaking (dB)**
19.44	622.08	32	13kΩ	0.47µF	33kΩ	220pF	3.8kHz	5.6	0.06
19.44	622.08	32	39kΩ	0.022µF	20kΩ	220pF	12.7kHz	7.7	0.03
19.44	622.08	32	2.2kΩ	10.0µF	22kΩ	3300pF	710Hz	4.4	0.10
155.52	622.08	4	3.9kΩ	0.47µF	39kΩ	100pF	11.0kHz	4.7	0.09
155.52	622.08	4	750Ω	10.0µF	7.5kΩ	1000pF	1.6kHz	4.2	0.10

Table 8: External Loop Filter Component Values for M2004-42

Note 1: K_{VCO} , VCSO Bandwidth, M Divider Value, and External Loop Filter Component Values determine Loop Bandwidth, Damping Factor, and Passband Peaking. For PLL Simulator software, go to www.icst.com.

External Loop Filter Component Values for M2004-22, M2004-32, and M2004-52[1]

VCSO Parameters: K_{VCO} = 800kHz/V, R_{IN} = 2016kΩ, VCSO Bandwidth = 700kHz. See AC Characteristics on pg. 8 for PLL Loop Constants.

Device Configuration			Example External Loop Filter Component Values				Nominal Performance Using These Values		
F_{Ref} (MHz)	**F_{VCSO} (MHz)**	**M Divider Value**	**R loop**	**C loop**	**R post**	**C post**	**PLL Loop Bandwidth**	**Damping Factor**	**Passband Peaking (dB)**
19.44	622.08	32	120kΩ	0.47µF	50kΩ	1000pF	265Hz	4.6	0.09
19.44	622.08	32	660kΩ	0.022µF	50kΩ	1000pF	1.83kHz	5.5	0.07
19.44	622.08	32	22kΩ	10.0µF	50kΩ	5000pF	47Hz	3.9	0.12
155.52	622.08	4	50kΩ	0.47µF	33kΩ	500pF	866Hz	5.4	0.07
155.52	622.08	4	27kΩ	2.0µF	50kΩ	500pF	500Hz	6.0	0.05
77.76	622.08	8	50Ω	1.0µF	33kΩ	500pF	414Hz	5.6	0.06

Table 9: External Loop Filter Component Values for M2004-22, M2004-32, and M2004-52

Note 1: K_{VCO} , VCSO Bandwidth, M Divider Value, and External Loop Filter Component Values determine Loop Bandwidth, Damping Factor, and Passband Peaking. For PLL Simulator software, go to www.icst.com.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Rating	Unit
V_I	Inputs	-0.5 to V_{CC} +0.5	V
V_O	Outputs	-0.5 to V_{CC} +0.5	V
V_{CC}	Power Supply Voltage	4.6	V
T_S	Storage Temperature	-45 to +100	°C

Table 10: Absolute Maximum Ratings

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in Recommended Conditions of Operation, DC Characteristics, or AC Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

RECOMMENDED CONDITIONS OF OPERATION

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Positive Supply Voltage		3.135	3.3	3.465	V
T_A	Ambient Operating Temperature	Commercial	0		+70	°C
		Industrial	-40		+85	°C

Table 11: Recommended Conditions of Operation

ELECTRICAL SPECIFICATIONS

DC Characteristics

Unless stated otherwise, V_{CC} = 3.3V ±5%, T_A = 0 °C to +70 °C (commercial), F_{VCSO} = F_{OUT} = 622-675MHz, Outputs terminated with 50Ω to V_{CC} - 2V
T_A = -40 °C to +85 °C (industrial)

	Symbol	Parameter		Min	Typ	Max	Unit	Conditions
Power Supply	V_{CC}	Positive Supply Voltage		3.135	3.3	3.465	V	
	I_{CC}	Power Supply Current			162		mA	
Differential Input: LVDS / LVPECL	V_{P-P}	Peak to Peak Input Voltage [1]	DIF_REF, nDIF_REF	0.15			V	
	V_{CMR}	Common Mode Input [1]		0.5		V_{cc} - 0.85	V	
LVCMOS / LVTTL Input	V_{IH}	Input High Voltage	REF_CLK, REF_SEL, MR, N0:N1, M0:M5	2		V_{cc} + 0.3	V	
	V_{IL}	Input Low Voltage		-0.3		1.3	V	
Inputs with Pull-down	I_{IH}	Input High Current	DIF_REF, REF_CLK, REF_SEL, MR, N0:N1, M0:M4			150	µA	V_{CC} = V_{IN} = 3.456V
	I_{IL}	Input Low Current		-5			µA	
	$R_{pulldown}$	Internal Pull-down Resistor			51		kΩ	
Inputs with Pull-up	I_{IH}	Input High Current	nDIF_REF, M5			5	µA	V_{CC} = 3.456V V_{IN} = 0 V
	I_{IL}	Input Low Current		-150			µA	
	R_{pullup}	Internal Pull-up Resistor			51		kΩ	
All Inputs	C_{IN}	Input Capacitance	All Inputs			4	pF	
Differential Outputs	V_{OH}	Output High Voltage	FOUT, nFOUT	V_{cc} - 1.4		V_{cc} - 1.0	V	
	V_{OL}	Output Low Voltage		V_{cc} - 2.0		V_{cc} - 1.7	V	
	V_{P-P}	Peak to Peak Output Voltage [2]		0.4		0.85	V	

Table 12: DC Characteristics

Note 1: Single-ended measurement. See Figure 6, Differential Input Level on pg. 9.
Note 2: Single-ended measurement. See Figure 5, Input and Output Rise and Fall Time on pg. 9.

ELECTRICAL SPECIFICATIONS (CONTINUED)

AC Characteristics

Unless stated otherwise, V_{CC} = 3.3V ±5%, T_A = 0 °C to +70 °C (commercial), F_{VCSO} = F_{OUT} = 622-675MHz, Outputs terminated with 50Ω to V_{CC} - 2V
T_A = -40 °C to +85 °C (industrial)

	Symbol	Parameter		Min	Typ	Max	Unit	Conditions
	F_{IN}	Input Frequency	DIF_REF, nDIF_REF, REF_CLK	1		175	MHz	
	F_{OUT}	Output Frequency	FOUT, nFOUT	38		700	MHz	
	APR	VCSO Pull-Range	Commercial	±120	±200		ppm	
			Industrial	±50	±150		ppm	
PLL Loop Constants [1]	K_{VCO}	VCO Gain			800		kHz/V	
	R_{IN}	Internal Loop Resistor	M2004-42		16		kΩ	
			M2004-22, M2004-32, M2004-52		2016		kΩ	
	BW_{VCSO}	VCSO Bandwidth			700		kHz	
Phase Noise and Jitter	Φn	Single Side Band Phase Noise @622.08MHz	1kHz Offset		-72		dBc/Hz	
			10kHz Offset		-94		dBc/Hz	
			100kHz Offset		-123		dBc/Hz	
	J(t)	Jitter (rms)	12kHz to 20MHz		0.5		ps	
			50kHz to 80MHz		0.5		ps	
	odc	Output Duty Cycle [2]	N = 2, 4, or 8	45	50	55	%	
			N = 1	40	50	60	%	
	t_R	Output Rise Time [2] for FOUT, nFOUT	F_{OUT} =155.52MHz N = 4 (N1:0 = 10)	350	450	550	ps	20% to 80%
			F_{OUT} =311.04MHz N = 2 (N1:0 = 01)	325	425	500	ps	
			F_{OUT} =622.08MHz N = 1 (N1:0 = 00)	200	275	350	ps	
	t_F	Output Fall Time [2] for FOUT, nFOUT	F_{OUT} =155.52MHz N = 4 (N1:0 = 10)	350	450	550	ps	20% to 80%
			F_{OUT} =311.04MHz N = 2 (N1:0 = 01)	325	425	500	ps	
			F_{OUT} =622.08MHz N = 1 (N1:0 = 00)	200	275	350	ps	
	t_{LOCK}	PLL Lock Time				100	ms	
	MTIE	Mean Time Interval Error [3]	M2004-22, M2004-32, M2004-42, M2004-52		Compliant with GR-253-CORE			

Table 13: AC Characteristics

Note 1: Parameters needed for PLL Simulator software; see Tables 8 and 9, External Loop Filter Component Values, on pg. 6.
Note 2: See Parameter Measurement Information on pg. 9.
Note 3: Requires proper loop filter settings. Consult factory.

PARAMETER MEASUREMENT INFORMATION

Input and Output Rise and Fall Time

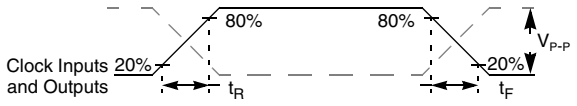

Figure 5: Input and Output Rise and Fall Time

Differential Input Level

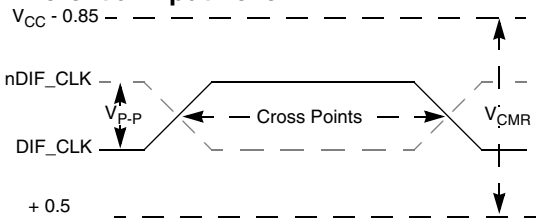

Figure 6: Differential Input Level

Output Duty Cycle

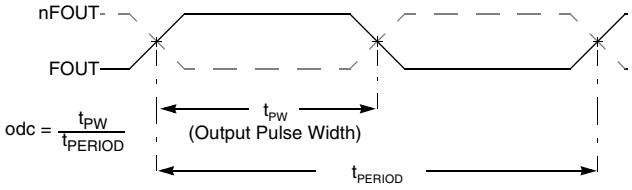

Figure 7: Output Duty Cycle

DEVICE PACKAGE - 9 x 9mm CERAMIC LEADLESS CHIP CARRIER

Mechanical Dimensions:

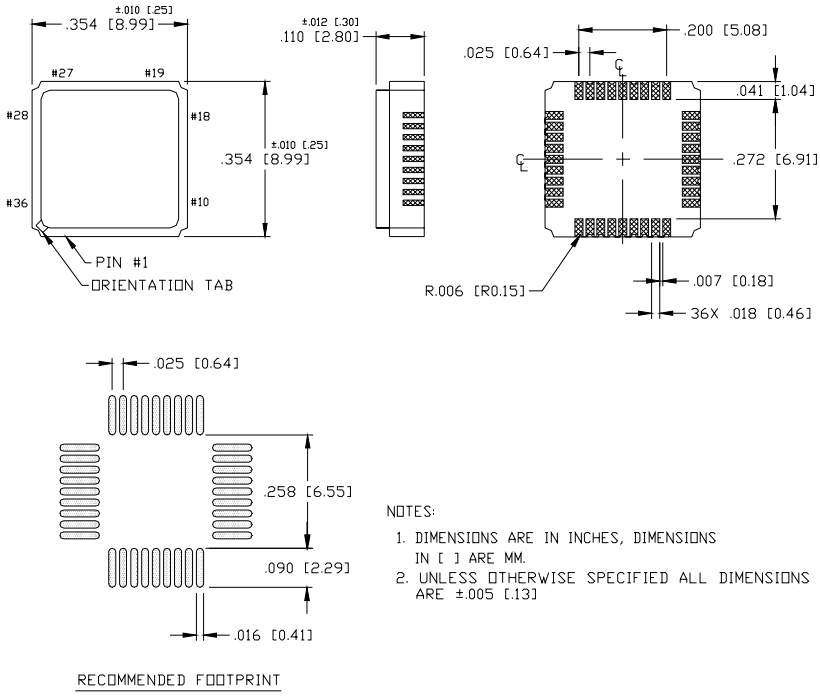

Figure 8: Device Package - 9 x 9mm Ceramic Leadless Chip Carrier

ORDERING INFORMATION

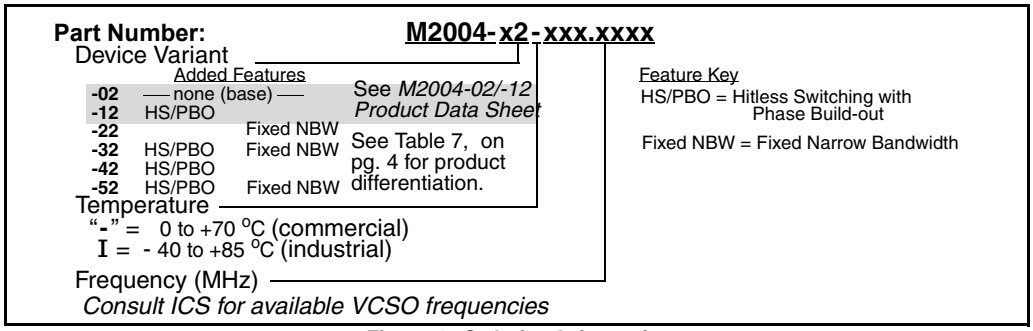

Figure 9: Ordering Information

Example Part Numbers

VCSO Freq (MHz)	Temperature	Part Number
622.08	commercial	**M2004-22-622.0800** or **M2004-32-622.0800** or **M2004-42-622.0800** or **M2004-52-622.0800**
	industrial	**M2004-22I622.0800** or **M2004-32I622.0800** or **M2004-42I622.0800** or **M2004-52I622.0800**

Table 14: Example Part Numbers

Consult ICS for the availability of other VCSO frequencies.