



M27V102

1 Mbit (64Kb x16) Low Voltage UV EPROM and OTP EPROM

NOT FOR NEW DESIGN

- **M27V102 is replaced by the M27W102**
- **LOW VOLTAGE READ OPERATION:**
3V to 3.6V
- **ACCESS TIME:** 90ns
- **LOW POWER CONSUMPTION:**
 - Active Current 15mA at 5MHz
 - Standby Current 20 μ A
- **PROGRAMMING VOLTAGE:** 12.75V \pm 0.25V
- **PROGRAMMING TIME:** 100 μ s/word
- **ELECTRONIC SIGNATURE**
 - Manufacturer Code: 20h
 - Device Code: 8Ch

DESCRIPTION

The M27V102 is a low voltage 1 Mbit EPROM offered in the two ranges UV (ultra violet erase) and OTP (one time programmable). It is ideally suited for microprocessor systems requiring large data or program storage and is organized as 65,536 words by 16 bits.

The M27V102 operates in the read mode with a supply voltage as low as 3V. The decrease in operating power allows either a reduction of the size of the battery or an increase in the time between battery recharges.

The FDIP40W (window ceramic frit-seal package) has a transparent lid which allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

For application where the content is programmed only one time and erasure is not required, the M27V102 is offered in PDIP40, PLCC32 and TSOP40 (10 x 14 mm) packages.

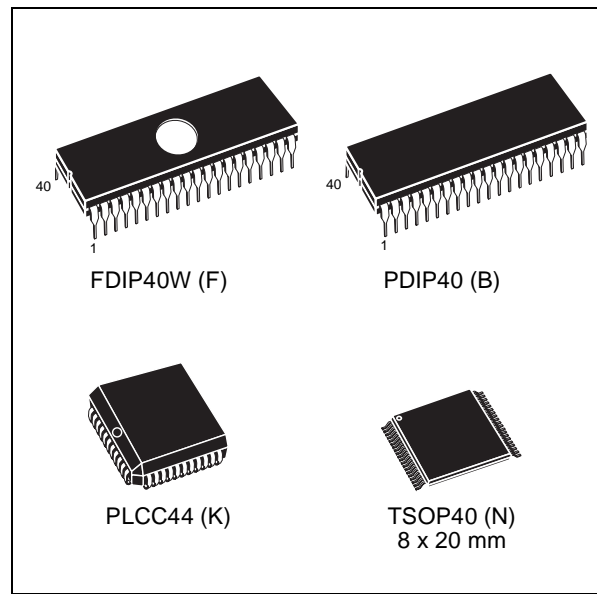
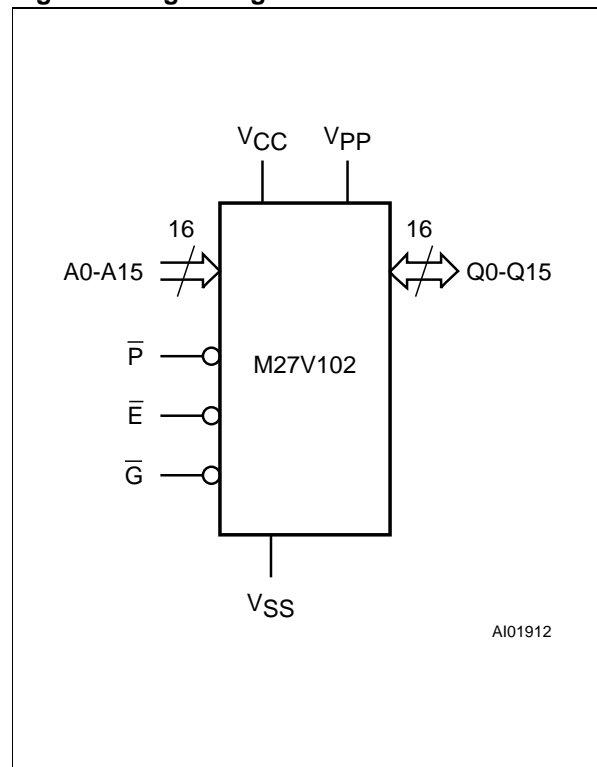


Figure 1. Logic Diagram



M27V102

Figure 2A. DIP Connections

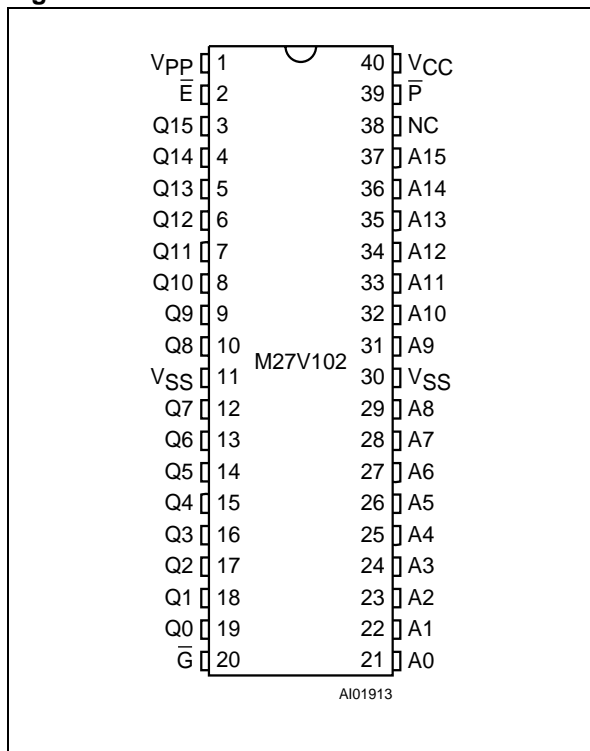


Figure 2B. LCC Connections

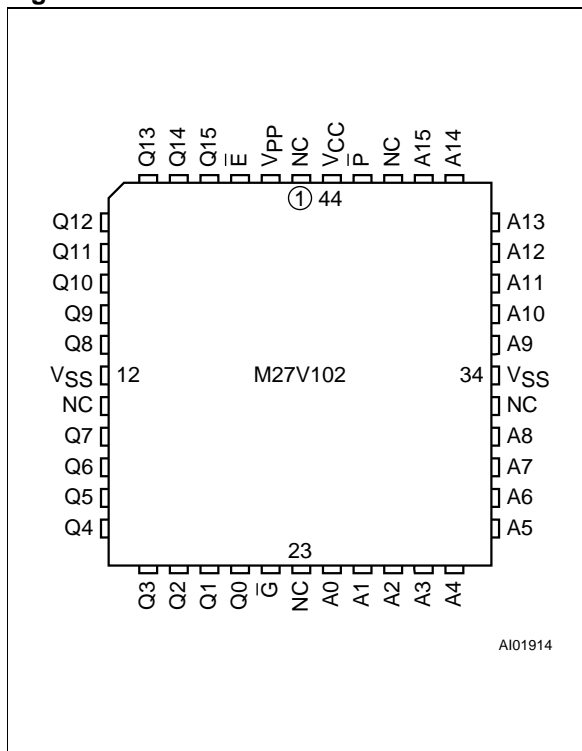


Figure 2C. TSOP Connections

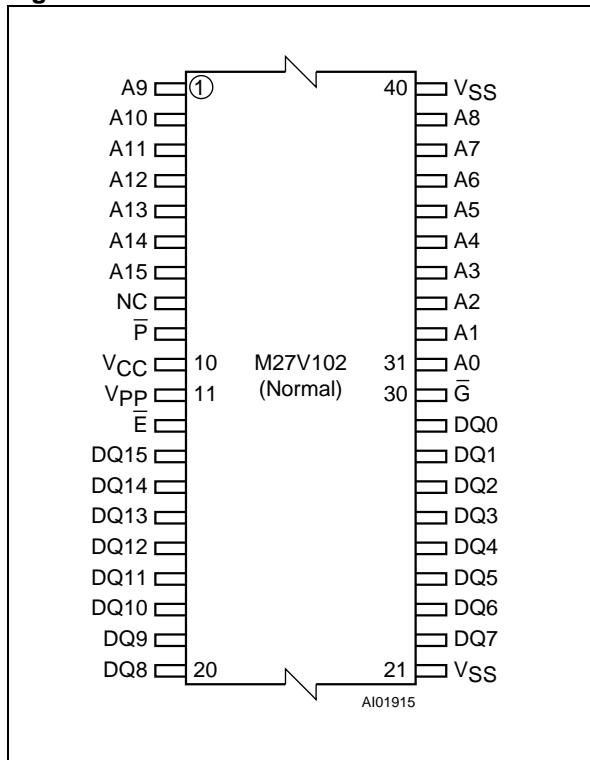


Table 1. Signal Names

| | |
|-----------|--------------------------|
| A0-A15 | Address Inputs |
| Q0-Q15 | Data Outputs |
| \bar{E} | Chip Enable |
| \bar{G} | Output Enable |
| \bar{P} | Program |
| V_{PP} | Program Supply |
| V_{CC} | Supply Voltage |
| V_{SS} | Ground |
| NC | Not Connected Internally |

Table 2. Absolute Maximum Ratings (1)

| Symbol | Parameter | Value | Unit |
|-------------------------|----------------------------------------------|------------|------|
| T_A | Ambient Operating Temperature ⁽³⁾ | -40 to 125 | °C |
| T_{BIAS} | Temperature Under Bias | -50 to 125 | °C |
| T_{STG} | Storage Temperature | -65 to 150 | °C |
| V_{IO} ⁽²⁾ | Input or Output Voltage (except A9) | -2 to 7 | V |
| V_{CC} | Supply Voltage | -2 to 7 | V |
| V_{A9} ⁽²⁾ | A9 Voltage | -2 to 13.5 | V |
| V_{PP} | Program Supply Voltage | -2 to 14 | V |

Note: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

2. Minimum DC voltage on Input or Output is -0.5V with possible undershoot to -2.0V for a period less than 20ns. Maximum DC voltage on Output is $V_{CC} + 0.5V$ with possible overshoot to $V_{CC} + 2V$ for a period less than 20ns.

3. Depends on range.

Table 3. Operating Modes

| Mode | \bar{E} | \bar{G} | \bar{P} | A9 | V_{PP} | Q15-Q0 |
|----------------------|-----------|-----------|----------------|----------|----------------------|-------------|
| Read | V_{IL} | V_{IL} | V_{IH} | X | V_{CC} or V_{SS} | Data Out |
| Output Disable | V_{IL} | V_{IH} | X | X | V_{CC} or V_{SS} | Hi-Z |
| Program | V_{IL} | X | V_{IL} Pulse | X | V_{PP} | Data In |
| Verify | V_{IL} | V_{IL} | V_{IH} | X | V_{PP} | Data Output |
| Program Inhibit | V_{IH} | X | X | X | V_{PP} | Hi-Z |
| Standby | V_{IH} | X | X | X | V_{CC} or V_{SS} | Hi-Z |
| Electronic Signature | V_{IL} | V_{IL} | V_{IH} | V_{ID} | V_{CC} | Codes |

Note: X = V_{IH} or V_{IL} , $V_{ID} = 12V \pm 0.5V$.

Table 4. Electronic Signature

| Identifier | A0 | Q7 | Q6 | Q5 | Q4 | Q3 | Q2 | Q1 | Q0 | Hex Data |
|---------------------|----------|----|----|----|----|----|----|----|----|----------|
| Manufacturer's Code | V_{IL} | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 20h |
| Device Code | V_{IH} | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 8Ch |

Note: Outputs Q15-Q8 are set to '0'.

Table 5. AC Measurement Conditions

| | High Speed | Standard |
|---------------------------------------|------------|--------------|
| Input Rise and Fall Times | ≤ 10ns | ≤ 20ns |
| Input Pulse Voltages | 0 to 3V | 0.4V to 2.4V |
| Input and Output Timing Ref. Voltages | 1.5V | 0.8V and 2V |

Figure 3. AC Testing Input Output Waveform

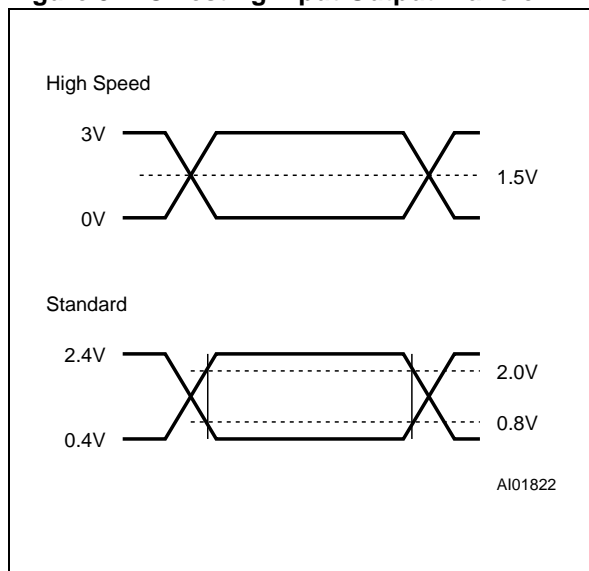


Figure 4. AC Testing Load Circuit

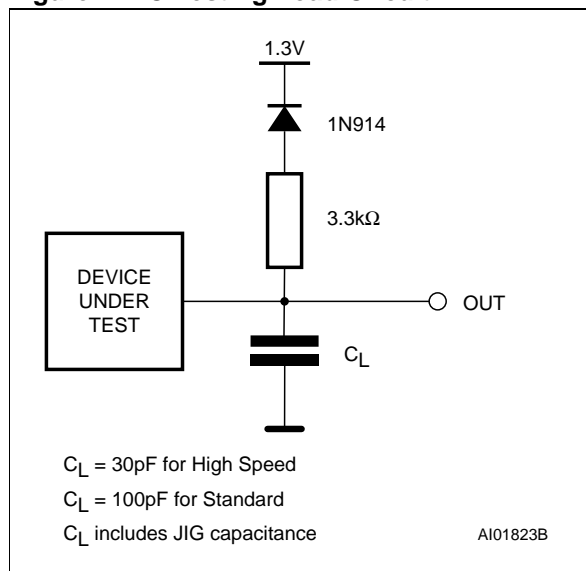


Table 6. Capacitance ⁽¹⁾ (T_A = 25 °C, f = 1 MHz)

| Symbol | Parameter | Test Condition | Min | Max | Unit |
|------------------|--------------------|-----------------------|-----|-----|------|
| C _{IN} | Input Capacitance | V _{IN} = 0V | | 6 | pF |
| C _{OUT} | Output Capacitance | V _{OUT} = 0V | | 12 | pF |

Note: Sampled only, not 100% tested.

DEVICE OPERATION

The operating modes of the M27V102 are listed in the Operating Modes table. A single power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A9 for Electronic Signature.

Read Mode

The M27V102 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable (\bar{E}) is the power control and should be used for device selection. Output Enable (\bar{G}) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the ad-

resses are stable, the address access time (t_{AVQV}) is equal to the delay from \bar{E} to output (t_{ELQV}). Data is available at the output after a delay of t_{OE} from the falling edge of \bar{G} , assuming that \bar{E} has been low and the addresses have been stable for at least t_{AVQV}-t_{GLQV}.

Standby Mode

The M27V102 has a standby mode which reduces the active current from 15mA to 20μA with low voltage operation V_{CC} ≤ 3.6V, see Read Mode DC Characteristics table for details. The M27V102 is placed in the standby mode by applying a TTL high signal to the \bar{E} input. When in the standby mode, the outputs are in a high impedance state, independent of the \bar{G} input.

Table 7. Read Mode DC Characteristics (1)

(TA = 0 to 70 °C or -40 to 85 °C; VCC = 3.3V ± 10%; VPP = VCC)

| Symbol | Parameter | Test Condition | Min | Max | Unit |
|---------------------|-------------------------------|--------------------------------------------------------------------------------------|------------------------|---------------------|------|
| ILI | Input Leakage Current | $0V \leq V_{IN} \leq V_{CC}$ | | ±10 | μA |
| ILO | Output Leakage Current | $0V \leq V_{OUT} \leq V_{CC}$ | | ±10 | μA |
| ICC | Supply Current | $\bar{E} = V_{IL}, \bar{G} = V_{IL}, I_{OUT} = 0mA,$ $f = 5MHz, V_{CC} \leq 3.6V$ | | 15 | mA |
| ICC1 | Supply Current (Standby) TTL | $\bar{E} = V_{IH}$ | | 1 | mA |
| ICC2 | Supply Current (Standby) CMOS | $\bar{E} > V_{CC} - 0.2V, V_{CC} \leq 3.6V$ | | 20 | μA |
| I _{PP} | Program Current | $V_{PP} = V_{CC}$ | | 10 | μA |
| V _{IL} | Input Low Voltage | | -0.3 | 0.8 | V |
| V _{IH} (2) | Input High Voltage | | 2 | V _{CC} + 1 | V |
| V _{OL} | Output Low Voltage | $I_{OL} = 2.1mA$ | | 0.4 | V |
| V _{OH} | Output High Voltage TTL | $I_{OH} = -400\mu A$ | 2.4 | | V |
| | Output High Voltage CMOS | $I_{OH} = -100\mu A$ | V _{CC} - 0.7V | | V |

Note: 1. VCC must be applied simultaneously with or before VPP and removed simultaneously or after VPP.

2. Maximum DC voltage on Output is VCC + 0.5V.

Table 8A. Read Mode AC Characteristics (1)

(TA = 0 to 70 °C or -40 to 85 °C; VCC = 3.3V ± 10%; VPP = VCC)

| Symbol | Alt | Parameter | Test Condition | M27V102 | | | | Unit |
|-----------------------|------------------|-----------------------------------------|--------------------------------------|---------|-----|------|-----|------|
| | | | | -90 (3) | | -100 | | |
| | | | | Min | Max | Min | Max | |
| t _{AVQV} | t _{ACC} | Address Valid to Output Valid | $\bar{E} = V_{IL}, \bar{G} = V_{IL}$ | | 90 | | 100 | ns |
| t _{ELQV} | t _{CE} | Chip Enable Low to Output Valid | $\bar{G} = V_{IL}$ | | 90 | | 100 | ns |
| t _{GLQV} | t _{OE} | Output Enable Low to Output Valid | $\bar{E} = V_{IL}$ | | 45 | | 50 | ns |
| t _{EHQZ} (2) | t _{DF} | Chip Enable High to Output Hi-Z | $\bar{G} = V_{IL}$ | 0 | 30 | 0 | 30 | ns |
| t _{GHQZ} (2) | t _{DF} | Output Enable High to Output Hi-Z | $\bar{E} = V_{IL}$ | 0 | 30 | 0 | 30 | ns |
| t _{AXQX} | t _{OH} | Address Transition to Output Transition | $\bar{E} = V_{IL}, \bar{G} = V_{IL}$ | 0 | | 0 | | ns |

Note: 1. VCC must be applied simultaneously with or before VPP and removed simultaneously or after VPP.

2. Sampled only, not 100% tested.

3. Speed obtained with High Speed AC measurement conditions.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, this product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:

- the lowest possible memory power dissipation,
- complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, \bar{E} should be decoded and used as the primary device selecting function, while \bar{G} should be made a common connection to all devices in the array and connected to the READ line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

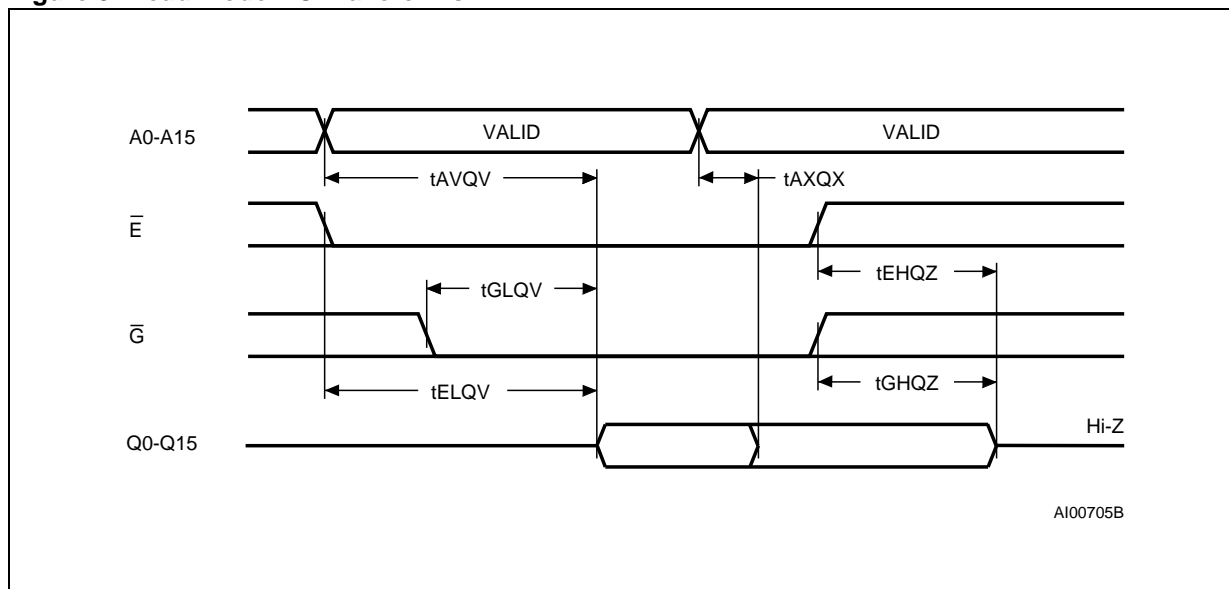
Table 8B. Read Mode AC Characteristics (1)

($T_A = 0$ to $70\text{ }^\circ\text{C}$ or -40 to $85\text{ }^\circ\text{C}$; $V_{CC} = 3.3\text{V} \pm 10\%$; $V_{PP} = V_{CC}$)

| Symbol | Alt | Parameter | Test Condition | M27V102 | | | | | | Unit |
|------------------|-----------|-----------------------------------------|--------------------------------------|---------|-----|------|-----|------|-----|------|
| | | | | -120 | | -150 | | -200 | | |
| | | | | Min | Max | Min | Max | Min | Max | |
| t_{AVQV} | t_{ACC} | Address Valid to Output Valid | $\bar{E} = V_{IL}, \bar{G} = V_{IL}$ | | 120 | | 150 | | 200 | ns |
| t_{ELQV} | t_{CE} | Chip Enable Low to Output Valid | $\bar{G} = V_{IL}$ | | 120 | | 150 | | 200 | ns |
| t_{GLQV} | t_{OE} | Output Enable Low to Output Valid | $\bar{E} = V_{IL}$ | | 50 | | 60 | | 90 | ns |
| $t_{EHQZ}^{(2)}$ | t_{DF} | Chip Enable High to Output Hi-Z | $\bar{G} = V_{IL}$ | 0 | 40 | 0 | 50 | 0 | 70 | ns |
| $t_{GHQZ}^{(2)}$ | t_{DF} | Output Enable High to Output Hi-Z | $\bar{E} = V_{IL}$ | 0 | 40 | 0 | 50 | 0 | 70 | ns |
| t_{AXQX} | t_{OH} | Address Transition to Output Transition | $\bar{E} = V_{IL}, \bar{G} = V_{IL}$ | 0 | | 0 | | 0 | | ns |

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP} .
 2. Sampled only, not 100% tested.

Figure 5. Read Mode AC Waveforms



System Considerations

The power switching characteristics of Advanced CMOS EPROMs require careful decoupling of the devices. The supply current, I_{CC} , has three segments that are of interest to the system designer: the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of \bar{E} . The magnitude of transient current peaks is dependent on the capacitive and inductive loading of the device at the output. The associated transient voltage peaks can be suppressed by complying with the two line

output control and by properly selected decoupling capacitors. It is recommended that a $0.1\mu\text{F}$ ceramic capacitor be used on every device between V_{CC} and V_{SS} . This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a $4.7\mu\text{F}$ bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for every eight devices. The bulk capacitor should be located near the power supply connection point. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

Table 9. Programming Mode AC Characteristics ⁽¹⁾
 ($T_A = 25\text{ }^\circ\text{C}$; $V_{CC} = 6.25\text{V} \pm 0.25\text{V}$; $V_{PP} = 12.75\text{V} \pm 0.25\text{V}$)

| Symbol | Parameter | Test Condition | Min | Max | Unit |
|----------|-------------------------|-----------------------------|------|----------------|---------------|
| I_{LI} | Input Leakage Current | $0 \leq V_{IN} \leq V_{IH}$ | | ± 10 | μA |
| I_{CC} | Supply Current | | | 50 | mA |
| I_{PP} | Program Current | $\bar{E} = V_{IL}$ | | 50 | mA |
| V_{IL} | Input Low Voltage | | -0.3 | 0.8 | V |
| V_{IH} | Input High Voltage | | 2 | $V_{CC} + 0.5$ | V |
| V_{OL} | Output Low Voltage | $I_{OL} = 2.1\text{mA}$ | | 0.4 | V |
| V_{OH} | Output High Voltage TTL | $I_{OH} = -400\mu\text{A}$ | 2.4 | | V |
| V_{ID} | A9 Voltage | | 11.5 | 12.5 | V |

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP} .

Table 10. Programming Mode AC Characteristics ⁽¹⁾
 ($T_A = 25\text{ }^\circ\text{C}$; $V_{CC} = 6.25\text{V} \pm 0.25\text{V}$; $V_{PP} = 12.75\text{V} \pm 0.25\text{V}$)

| Symbol | Alt | Parameter | Test Condition | Min | Max | Unit |
|------------------|-----------|------------------------------------------|----------------|-----|-----|---------------|
| t_{AVPL} | t_{AS} | Address Valid to Program Low | | 2 | | μs |
| t_{QVPL} | t_{DS} | Input Valid to Program Low | | 2 | | μs |
| t_{VPHPL} | t_{VPS} | V_{PP} High to Program Low | | 2 | | μs |
| t_{VCHPL} | t_{VCS} | V_{CC} High to Program Low | | 2 | | μs |
| t_{ELPL} | t_{CES} | Chip Enable Low to Program Low | | 2 | | μs |
| t_{PLPH} | t_{PW} | Program Pulse Width | | 95 | 105 | μs |
| t_{PHQX} | t_{DH} | Program High to Input Transition | | 2 | | μs |
| t_{QXGL} | t_{OES} | Input Transition to Output Enable Low | | 2 | | μs |
| t_{GLQV} | t_{OE} | Output Enable Low to Output Valid | | | 100 | ns |
| $t_{GHQZ}^{(2)}$ | t_{DFP} | Output Enable High to Output Hi-Z | | 0 | 130 | ns |
| t_{GHAX} | t_{AH} | Output Enable High to Address Transition | | 0 | | ns |

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP} .

2. Sampled only, not 100% tested.

Programming

The M27V102 has been designed to be fully compatible with the M27C1024 and has the same electronic signature. As a result the M27V102 can be programmed as the M27C1024 on the same programming equipments applying 12.75V on V_{PP} and 6.25V on V_{CC} by the use of the same PRES-TO II algorithm. When delivered (and after each '1's erasure for UV EPROM), all bits of the M27V102 are in the '1' state. Data is introduced by selectively programming '0's into the desired bit locations.

Although only '0's will be programmed, both '1's and '0's can be present in the data word. The only way to change a '0' to a '1' is by die exposure to ultraviolet light (UV EPROM). The M27V102 is in the programming mode when V_{PP} input is at 12.75V, \bar{E} is at V_{IL} and \bar{P} is pulsed to V_{IL} . The data to be programmed is applied to 16 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. V_{CC} is specified to be $6.25\text{V} \pm 0.25\text{V}$.

Figure 6. Programming and Verify Modes AC Waveforms

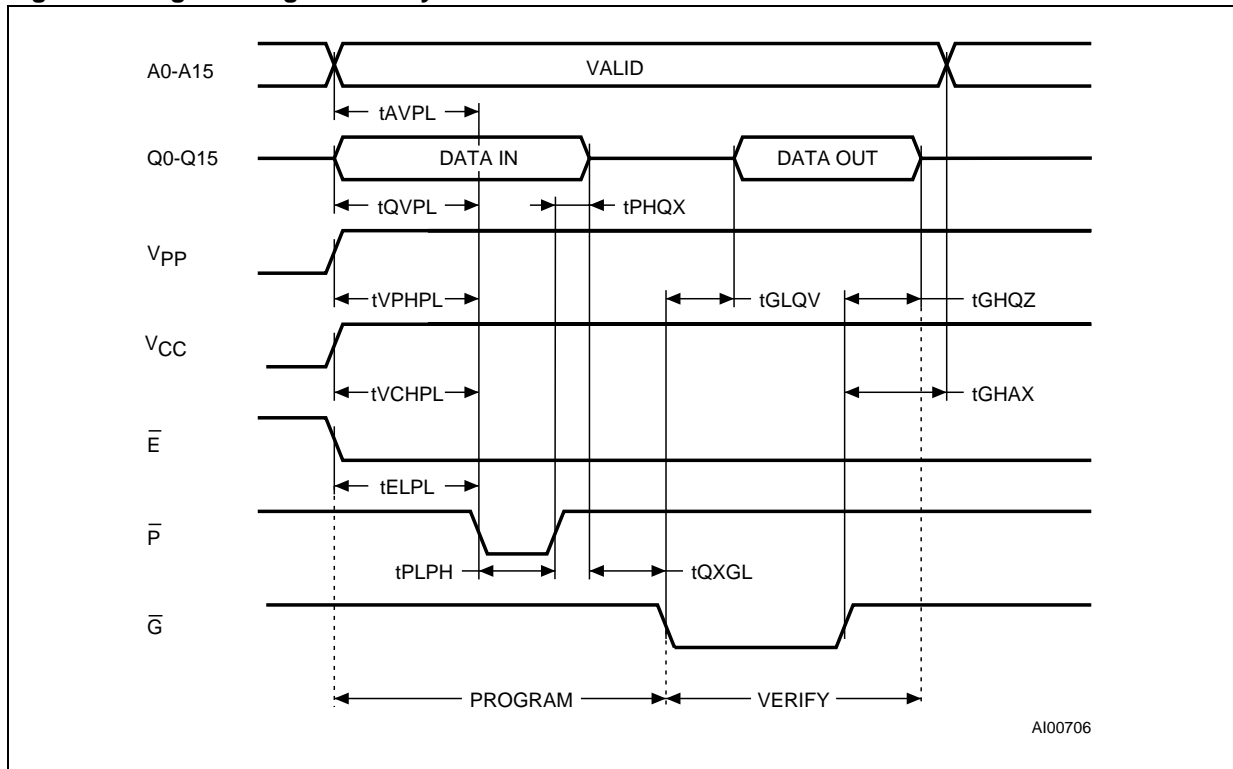
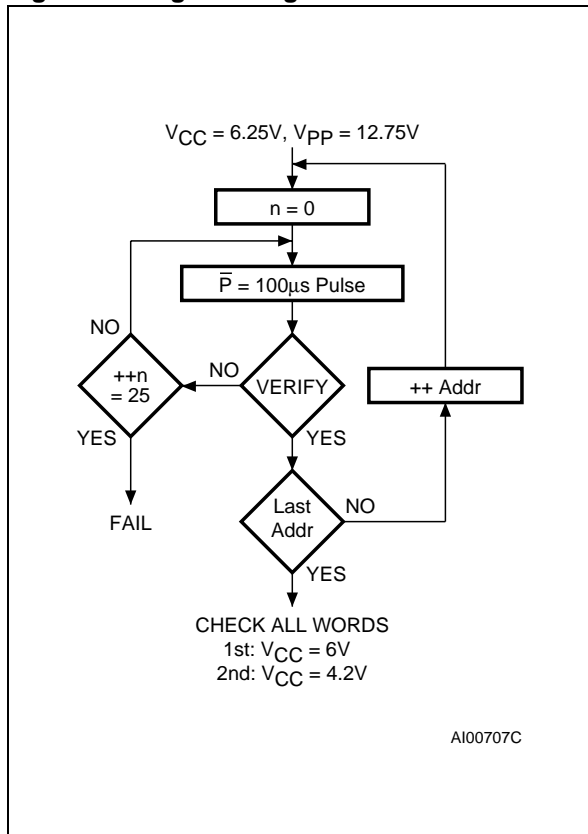


Figure 7. Programming Flowchart



PRESTO II Programming Algorithm

PRESTO II Programming Algorithm allows programming of the whole array with a guaranteed margin, in a typical time of 6.5 seconds. Programming with PRESTO II consists of applying a sequence of 100µs program pulses to each word until a correct verify occurs (see Figure 7). During programming and verify operation, a MARGIN MODE circuit is automatically activated in order to guarantee that each cell is programmed with enough margin. No overprogram pulse is applied since the verify in MARGIN MODE at V_{CC} much higher than 3.6V provides necessary margin to each programmed cell.

Program Inhibit

Programming of multiple M27V102s in parallel with different data is also easily accomplished. Except for E̅, all like inputs including G̅ of the parallel M27V102 may be common. A TTL low level pulse applied to a M27V102's P̅ input, with E̅ low and V_{PP} at 12.75V, will program that M27V102. A high level E̅ input inhibits the other M27V102s from being programmed.

Program Verify

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with E̅ and G̅ at V_{IL}, P̅ at V_{IH}, V_{PP} at 12.75V and V_{CC} at 6.25V.



Electronic Signature

The Electronic Signature (ES) mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. The ES mode is functional in the $25^{\circ}\text{C} \pm 5^{\circ}\text{C}$ ambient temperature range that is required when programming the M27V102. To activate the ES mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M27V102 with $V_{PP} = V_{CC} = 5\text{V}$. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH} . All other address lines must be held at V_{IL} during Electronic Signature mode. Byte 0 ($A0 = V_{IL}$) represents the manufacturer code and byte 1 ($A0 = V_{IH}$) the device identifier code. For the STMicroelectronics M27V102, these two identifier bytes are given in Table 4 and can be read-out on outputs Q7 to Q0. Note that the M27V102 and M27C1024 have the same identifier bytes.

ERASURE OPERATION (applies to UV EPROM)

The erasure characteristics of the M27V102 is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 Å range. Research shows that constant exposure to room level fluorescent lighting could erase a typical M27V102 in about 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M27V102 is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M27V102 window to prevent unintentional erasure. The recommended erasure procedure for the M27V102 is exposure to short wave ultraviolet light which has wavelength 2537 Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2 . The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with $12000\mu\text{W/cm}^2$ power rating. The M27V102 should be placed within 2.5 cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

M27V102

Table 11. Ordering Information Scheme

| | | | | | |
|----------------------------------------------------------------------------------------------------------------|---------|-----|---|---|----|
| Example: | M27V102 | -90 | K | 1 | TR |
| Device Type M27 | | | | | |
| Supply Voltage V = 3.3V ±10% | | | | | |
| Device Function 102 = 1 Mbit (64Kb x16) | | | | | |
| Speed -90 ⁽¹⁾ = 90 ns -100 = 100 ns -120 = 120 ns -150 = 150 ns -200 = 200 ns | | | | | |
| Package F = FDIP40W B = PDIP40 K = PLCC44 N = TSOP40: 10 x 14 mm | | | | | |
| Temperature Range 1 = 0 to 70 °C 6 = -40 to 85 °C | | | | | |
| Options TR = Tape & Reel Packing | | | | | |

Note: 1. High Speed, see AC Characteristics section for further information.

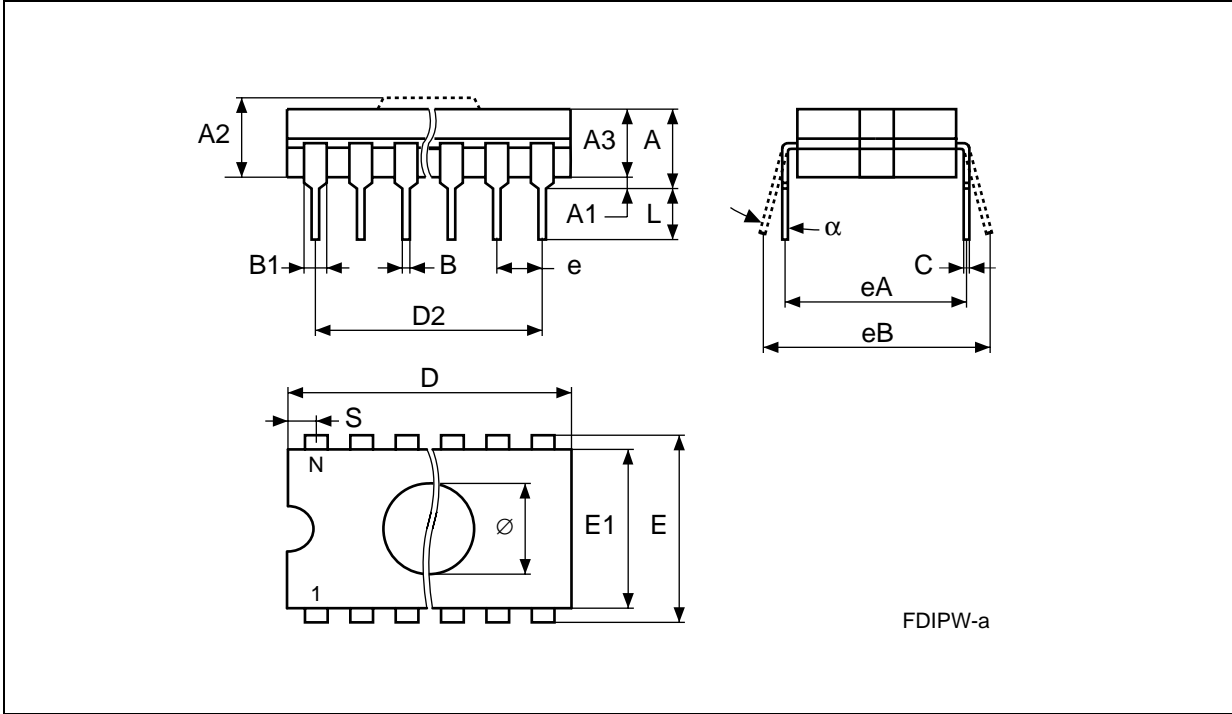
M27V102 is replaced by the M27W102

For a list of available options (Speed, Package, etc...) or for further information on any aspect of this device, please contact the STMicroelectronics Sales Office nearest to you.

Table 12. FDIP40W - 40 pin Ceramic Frit-seal DIP with window, Package Mechanical Data

| Symb | mm | | | inches | | |
|------|-------|-------|-------|--------|-------|-------|
| | Typ | Min | Max | Typ | Min | Max |
| A | | | 5.72 | | | 0.225 |
| A1 | | 0.51 | 1.40 | | 0.020 | 0.055 |
| A2 | | 3.91 | 4.57 | | 0.154 | 0.180 |
| A3 | | 3.89 | 4.50 | | 0.153 | 0.177 |
| B | | 0.41 | 0.56 | | 0.016 | 0.022 |
| B1 | 1.45 | - | - | 0.057 | - | - |
| C | | 0.23 | 0.30 | | 0.009 | 0.012 |
| D | | 51.79 | 52.60 | | 2.039 | 2.071 |
| D2 | 48.26 | - | - | 1.900 | - | - |
| E | 15.24 | - | - | 0.600 | - | - |
| E1 | | 13.06 | 13.36 | | 0.514 | 0.526 |
| e | 2.54 | - | - | 0.100 | - | - |
| eA | 14.99 | - | - | 0.590 | - | - |
| eB | | 16.18 | 18.03 | | 0.637 | 0.710 |
| L | | 3.18 | | | 0.125 | |
| S | | 1.52 | 2.49 | | 0.060 | 0.098 |
| ∅ | 7.62 | - | - | 0.300 | - | - |
| α | | 4° | 11° | | 4° | 11° |
| N | | 40 | | | 40 | |

Figure 8. FDIP40W - 40 pin Ceramic Frit-seal DIP with window, Package Outline

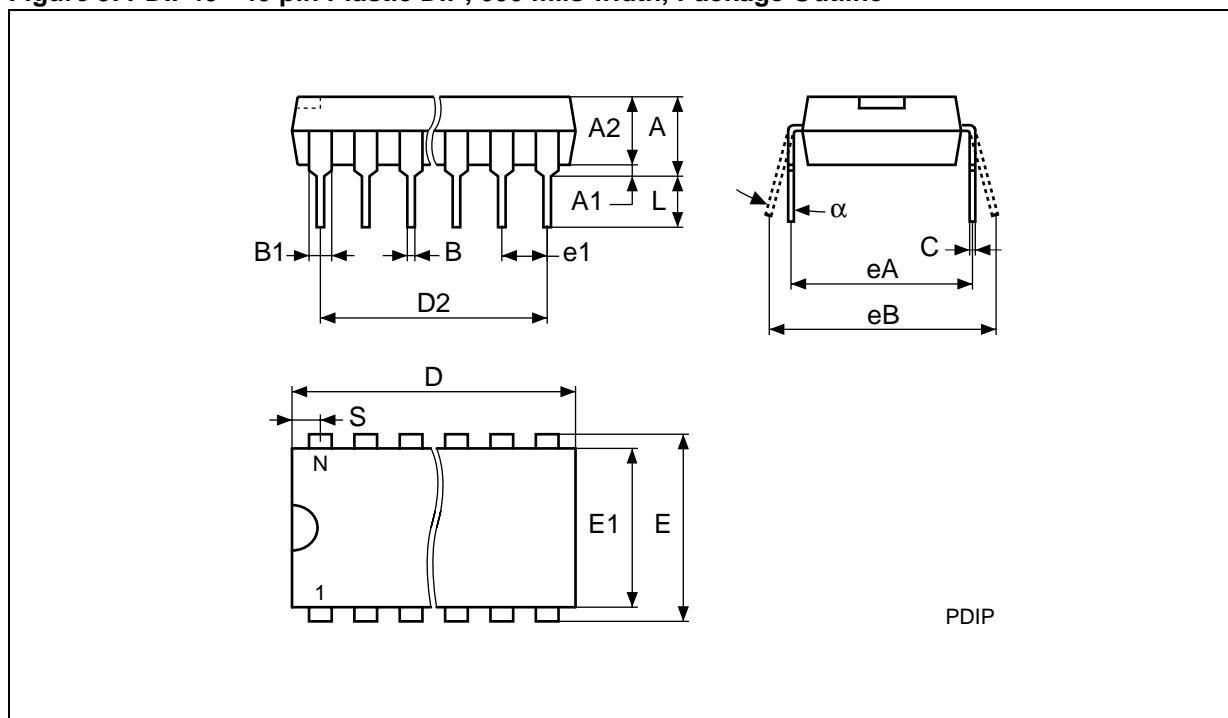


Drawing is not to scale.

Table 13. PDIP40 - 40 pin Plastic DIP, 600 mils width, Package Mechanical Data

| Symb | mm | | | inches | | |
|----------|-------|-------|-------|--------|-------|-------|
| | Typ | Min | Max | Typ | Min | Max |
| A | 4.45 | – | – | 0.175 | – | – |
| A1 | 0.64 | 0.38 | – | 0.025 | 0.015 | – |
| A2 | | 3.56 | 3.91 | | 0.140 | 0.154 |
| B | | 0.38 | 0.53 | | 0.015 | 0.021 |
| B1 | | 1.14 | 1.78 | | 0.045 | 0.070 |
| C | | 0.20 | 0.31 | | 0.008 | 0.012 |
| D | | 51.78 | 52.58 | | 2.039 | 2.070 |
| D2 | 48.26 | – | – | 1.900 | – | – |
| E | | 14.80 | 16.26 | | 0.583 | 0.640 |
| E1 | | 13.46 | 13.99 | | 0.530 | 0.551 |
| e1 | 2.54 | – | – | 0.100 | – | – |
| eA | 15.24 | – | – | 0.600 | – | – |
| eB | | 15.24 | 17.78 | | 0.600 | 0.700 |
| L | | 3.05 | 3.81 | | 0.120 | 0.150 |
| S | | 1.52 | 2.29 | | 0.060 | 0.090 |
| α | | 0° | 15° | | 0° | 15° |
| N | | 40 | | | 40 | |

Figure 9. PDIP40 - 40 pin Plastic DIP, 600 mils width, Package Outline

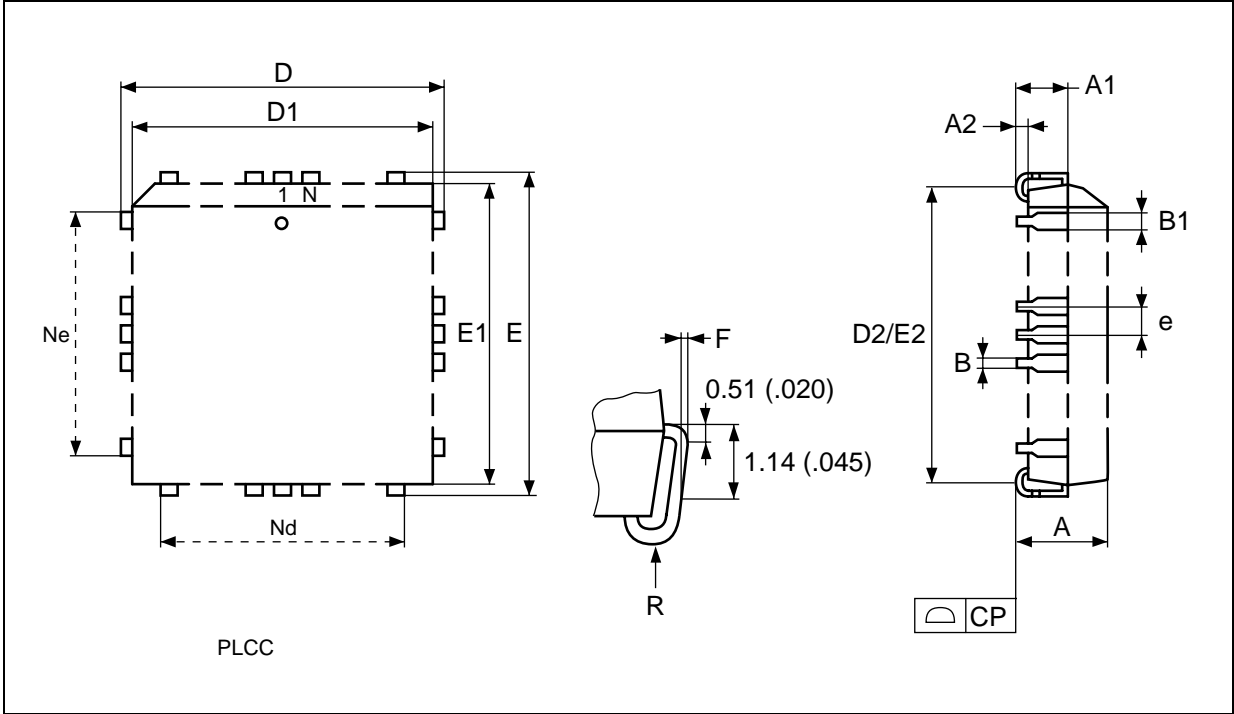


Drawing is not to scale.

Table 14. PLCC44 - 44 lead Plastic Leaded Chip Carrier, Package Mechanical Data

| Symb | mm | | | inches | | |
|------|------|-------|-------|--------|-------|-------|
| | Typ | Min | Max | Typ | Min | Max |
| A | | 4.20 | 4.70 | | 0.165 | 0.185 |
| A1 | | 2.29 | 3.04 | | 0.090 | 0.120 |
| A2 | | - | 0.51 | | - | 0.020 |
| B | | 0.33 | 0.53 | | 0.013 | 0.021 |
| B1 | | 0.66 | 0.81 | | 0.026 | 0.032 |
| D | | 17.40 | 17.65 | | 0.685 | 0.695 |
| D1 | | 16.51 | 16.66 | | 0.650 | 0.656 |
| D2 | | 14.99 | 16.00 | | 0.590 | 0.630 |
| E | | 17.40 | 17.65 | | 0.685 | 0.695 |
| E1 | | 16.51 | 16.66 | | 0.650 | 0.656 |
| E2 | | 14.99 | 16.00 | | 0.590 | 0.630 |
| e | 1.27 | - | - | 0.050 | - | - |
| F | | 0.00 | 0.25 | | 0.000 | 0.010 |
| R | 0.89 | - | - | 0.035 | - | - |
| N | 44 | | | 44 | | |
| CP | | | 0.10 | | | 0.004 |

Figure 10. PLCC44 - 44 lead Plastic Leaded Chip Carrier, Package Outline

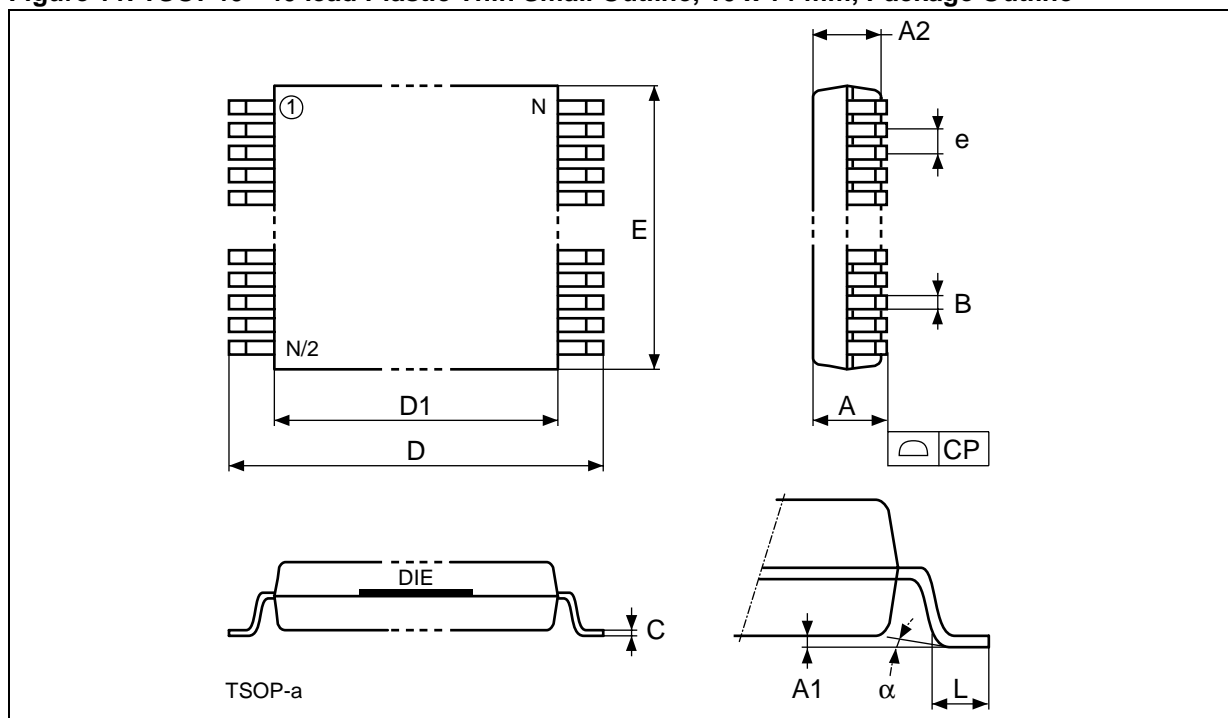


Drawing is not to scale.

Table 15. TSOP40 - 40 lead Plastic Thin Small Outline, 10 x 14 mm, Package Mechanical Data

| Symb | mm | | | inches | | |
|----------|------|-------|-------|--------|-------|-------|
| | Typ | Min | Max | Typ | Min | Max |
| A | | | 1.20 | | | 0.047 |
| A1 | | 0.05 | 0.15 | | 0.002 | 0.006 |
| A2 | | 0.95 | 1.05 | | 0.037 | 0.041 |
| B | | 0.17 | 0.27 | | 0.007 | 0.011 |
| C | | 0.10 | 0.21 | | 0.004 | 0.008 |
| D | | 13.80 | 14.20 | | 0.543 | 0.559 |
| D1 | | 12.30 | 12.50 | | 0.484 | 0.492 |
| E | | 9.90 | 10.10 | | 0.390 | 0.398 |
| e | 0.50 | - | - | 0.020 | - | - |
| L | | 0.50 | 0.70 | | 0.020 | 0.028 |
| α | | 0° | 5° | | 0° | 5° |
| N | 40 | | | 40 | | |
| CP | | | 0.10 | | | 0.004 |

Figure 11. TSOP40 - 40 lead Plastic Thin Small Outline, 10 x 14 mm, Package Outline



Drawing is not to scale.

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