



82424 CACHE AND DRAM CONTROLLER (CDC)

- Supports 25 MHz/33 MHz/50 MHz Intel486™ SX, Intel487™ SX, Intel486 DX, Intel486 DX2, OverDrive™ for Intel486 and OverDrive for DX2 Processors
- Fully Synchronous, 25 MHz/33 MHz PCI Bus Capable of Supporting Bus Masters
- Supports OverDrive Upgrade Socket, Including OverDrive for DX2 in Write-Back Mode
- Programmable Attribute Map for First 1-Mbyte of Main Memory
- Posted Write Buffers for Improved Performance
- Integrated DRAM Controller
 - 2-Mbyte to 160-Mbyte Main Memory using 70 ns Fast Page Mode SIMM Memory
 - Decoupled Refresh Cycles to Reduce DRAM Access Latency
 - Burst Mode PCI Accesses to DRAM Supported at the Rate of x-3-3-3-3
- Integrated Cache Controller
 - Write-Through and Write-Back Cache Options
 - 64 KB, 128 KB, 256 KB and 512 KB Cache Sizes using Standard SRAMs
 - Burst Line Fill of 2-1-1-1 from Secondary Cache at 25 MHz and 33 MHz and 3-1-1-1 at 50 MHz
 - Zero Wait State Write to L2 Cache for a Cache Write Hit
 - Main Memory Posting at Zero Wait States, Enabling Optimum Write-Through Cache Performance
 - Concurrent Cache Line Replacement from Secondary Cache in Write-Back Mode
- PCI Bridge
 - Translates CPU Cycles into PCI Bus Cycles
 - Translates Back-to-Back Sequential Memory Write Cycles Into PCI Burst Cycles
 - Separate PCI-to-Main Memory Port Allows Concurrent/Independent CPU and PCI Bus Operations
 - Integrated Snoop Filter

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The 82424 Cache DRAM Controller (CDC) integrates the cache and main memory DRAM control functions and provides the address paths and bus control for transfers between the Host (CPU/cache), main memory, and the Peripheral Component Interconnect (PCI) Bus. The Dual-ported architecture permits concurrent operations on the Host and PCI Buses. The cache controller supports both write-through and write-back cache policies and cache sizes from 64 Kbytes to 512 Kbytes. The cache memory can be implemented using standard asynchronous SRAMs. The dual-ported main memory DRAM controller interfaces DRAM to the Host Bus and the PCI Bus. The CDC supports a two-way interleaved DRAM organization for optimum performance. Up to eight single sided SIMMs or four dual sided SIMMs provide a maximum of 160 Mbytes of main memory. The CDC is intended to be used with the 82423 Data Path Unit (DPU). The DPU provides 32-bit data paths between the Host, main memory, and the PCI. Together, these two components provide a full function dual-port data path connection to main memory and form a Host/PCI Bridge.

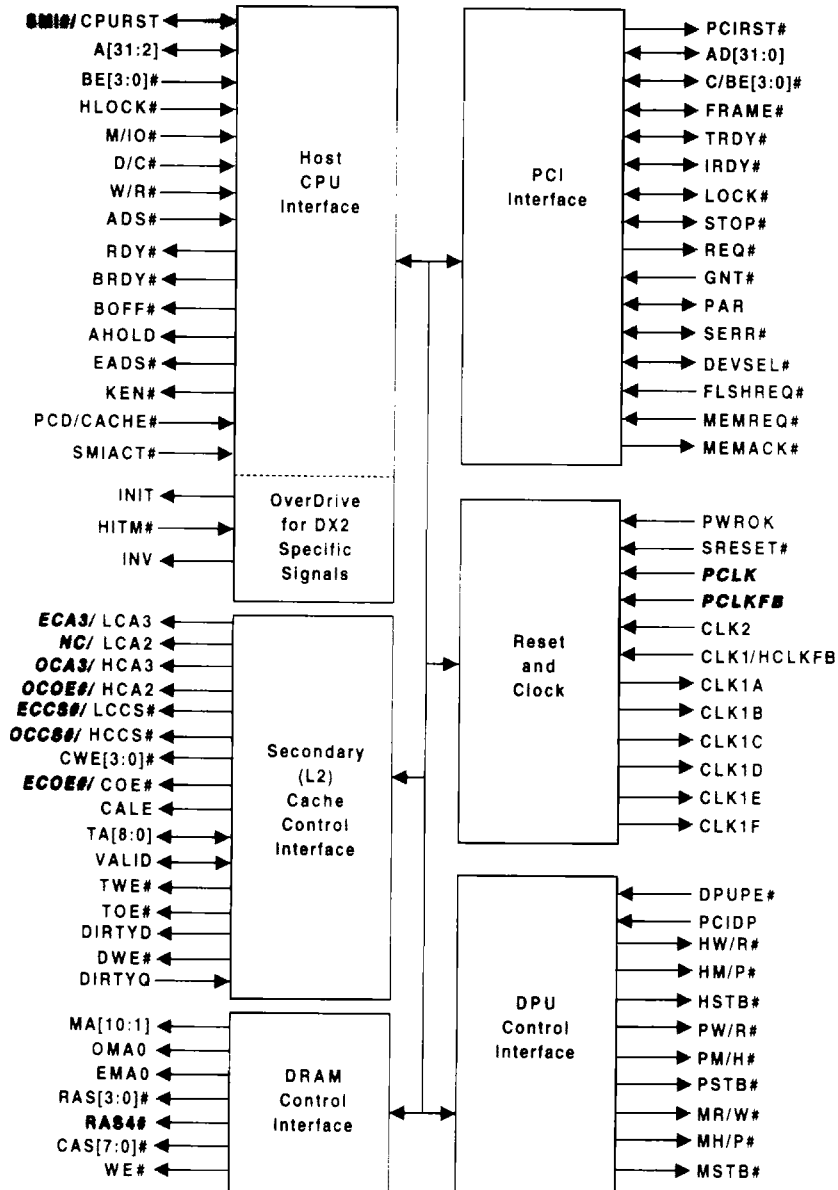
This data sheet describes the 82424TX, 82424ZX and 82424ZX-50 components. All normal text describes the functionality for all three components. All features that exist on the 82424ZX and 82424ZX-50 are shaded as shown below.

This is an example of what the shaded sections that apply only to 82424ZX and 82424ZX-50 components look like.

All features that exist only on the 82424ZX-50 are shaded as shown below.

This is an example of what the shaded sections that apply only to the 82424ZX-50 component look like.

Simplified CDC Block Diagram



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