HM67M1864 Series (Target Spec.)

ADE-203-226(Z)
Rev. 0
Mar.31,1994
Product Preview

64K × 18 Bits Synchronous Fast Static RAM With Burst Counter and Self-Timed Write

Description

The HM67B1864 is a 1,179,648 bit density high performance synchronous static random access memory organized as 64k×18 bit. This SRAM is designed to support high performance secondary cache for the PowerPC™ and 680XX based systems.

This SRAM integrates input registers and a 2-bit counter to support linear burst sequence. All sysnchronous inputs including all addresses, all data inputs, a chip enable ($\overline{CE}$), burst control inputs ($\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$), and two write enables ($\overline{LW}$, $\overline{UW}$) are registered and controlled by rising edge of external clock input (CLK).

Address Status Processor ($\overline{ADSP}$) or Address Status Controller ($\overline{ADSC}$) can initiate the burst operation. Burst Address Advance ($\overline{ADV}$) controls continued burst addresses generated internally. Asynchronous Output Enable ($\overline{OE}$) enables all data outputs, which are also asynchronous.

Address, input data and write control are registered to support self-timed write function. Two write enables allow individual byte (upper and/or lower byte) write.

The HM67B1864 operates from +3.3V power supply, and all inputs and outputs are LVTTL compatible.

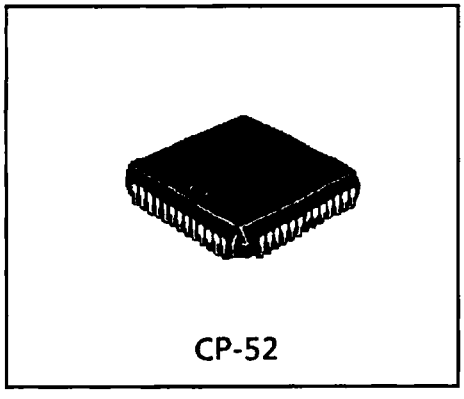
Features

- Single 3.3V Power Supply (LV-TTL)
- Fast Access Times: 9 / 12 ns(max)
- Byte writeable via Dual Write Enables
- Internal Input Registers
  (Address, Data, Control)
- Internal Self-Timed Write Cycle
- $\overline{ADSP}$, $\overline{ADSC}$, and $\overline{ADV}$ burst Control Pins
  (linear burst sequence)
- Three-state outputs Controlled by
  Asynchronous Output Enable
- Common data inputs and data outputs
- High board density 52-Lead PLCC package

Ordering Information

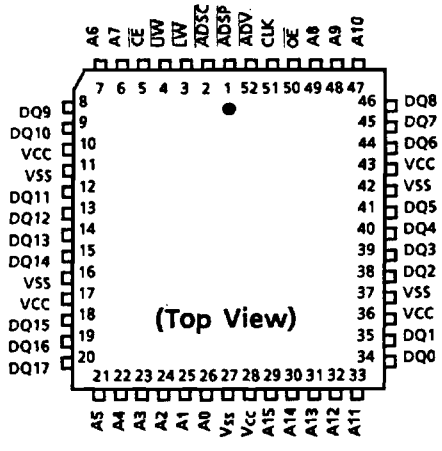
Type No.	Access Time	CPU Clock Rate	Package
HM67M1864CP-9	9ns	66MHZ	PLCC 52pin
HM67M1864CP-12	12ns	50MHZ	(CP-52)

Package Outline



CP-52

Pin Assignment



Pin Descriptions

Pin name	Function
A0-A15	Address Input
CLK	Clock
$\overline{ADV}$	Burst Address Advance
$\overline{LW}$	Lower Byte Write Enable
$\overline{UW}$	Upper Byte Write Enable
$\overline{ADSC}$	Controller Address Status
$\overline{ADSP}$	Processor Address Status
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
D_{Q0}-D_{Q17}	Data Input/Output
V_{CC}	3.3V Power Supply
V_{SS}	Ground

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All power supply and ground pins must be connected for proper operation of the device.

This document contains information on a new product.

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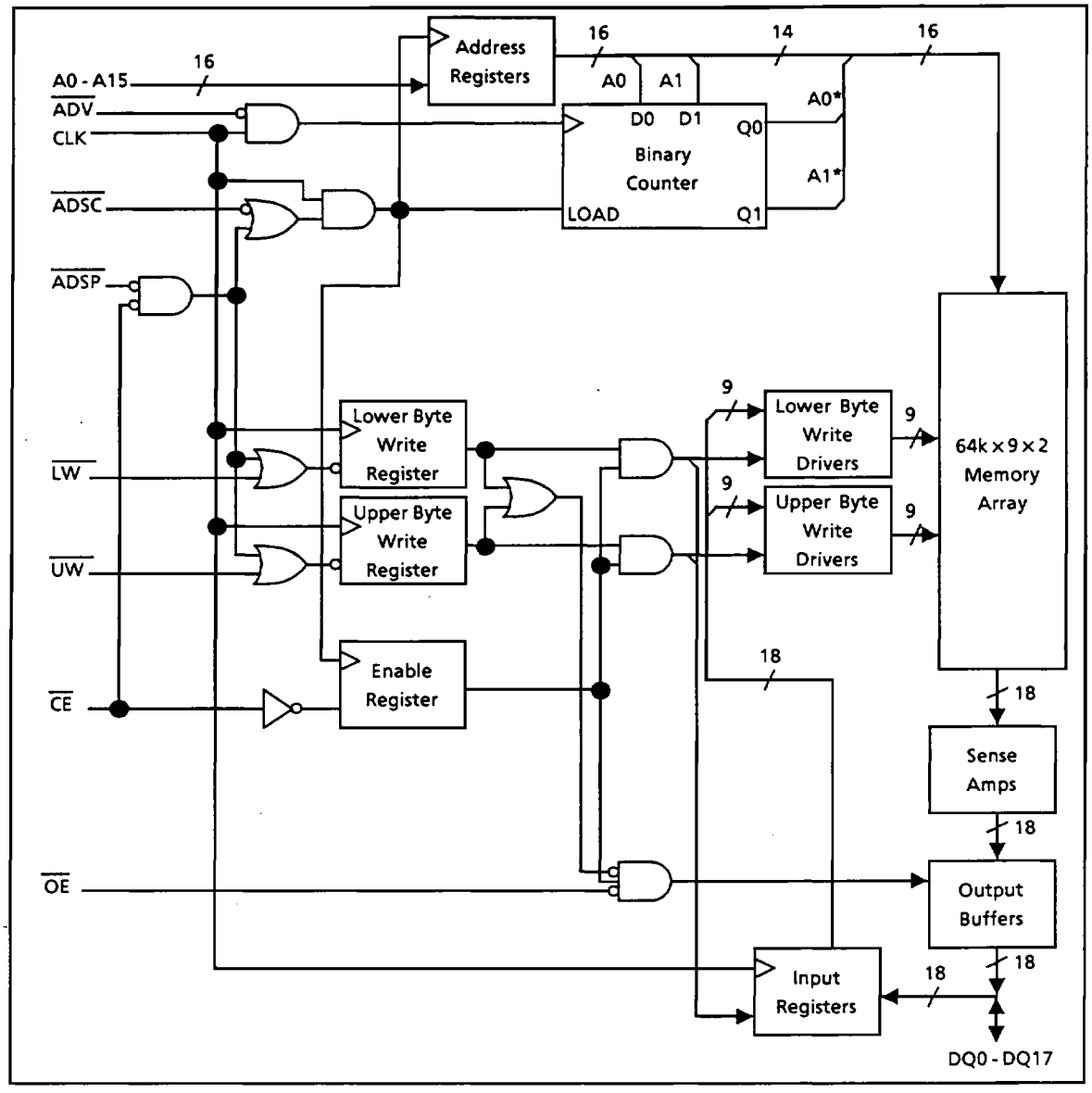
Hitachi semiconductor

Block Diagram

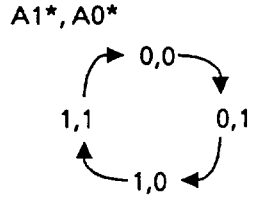


NOTE : The functional block diagram illustrates simplified device operation. See truth table, pin descriptions adn timing diagrams for detailed information.

Burst Sequence Table

External Address	A14 – A2	A1	A0
1st Burst Address	A14 – A2	A0⊕A1	$\overline{A0}$
2nd Burst Address	A14 – A2	$\overline{A1}$	A0
3rd Burst Address	A14 – A2	$\overline{A0 \oplus A1}$	$\overline{A0}$

Note : The burst wraps around to its initial state upon completion.



Seuence Diagram
(linear burst sequence)

Signal Description

Pin Name	Function
A0 – A15	Synchronous Address Inputs : These inputs are registered and must meet the setup and hold times around the rising edge of CLK.
$\overline{LW}$ $\overline{UW}$	Synchronous Byte Write Enables : These active LOW inputs allow individual bytes to be written and must meet the setup and hold times around the rising edge of CLK. A byte write enable is LOW for a WRITE cycle and HIGH for a READ cycle. $\overline{LW}$ controls DQ0-DQ8 (the lower bits), while $\overline{UW}$ controls DQ9-DQ17 (the upper bits).
CLK	Clock : This signal latches the address, data, chip enables, byte write enables and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
$\overline{CE}$	Synchronous Chip Enable : This active LOW input is used to enable the device and conditions internal use of $\overline{ADSP}$. This input is sampled only when a new external address is loaded.
$\overline{OE}$	Output Enable : This active LOW asynchronous input enables the data I/O output drivers.
$\overline{ADV}$	Synchronous Address Advance : This active LOW input is used to advance the internal burst counter, controlling burst access after the external address is loaded. A HIGH on this pin effectively causes wait states to be generated (no address advance). This pin must be HIGH at the rising edge of the first clock after an $\overline{ADSP}$ cycle is initiated if a WRITE cycle is desired (to ensure use of correct address).
$\overline{ADSP}$	Synchronous Address Status Processor : This active LOW input interrupts any ongoning burst, causing a new external address to be latched. A READ is perfomed using the new address, independent of the byte write enables and $\overline{ADSC}$ but dependent upon $\overline{CE}$. $\overline{ADSP}$ is ignored if $\overline{CE}$ is HIGH.
$\overline{ADSC}$	Synchronous Address Status Controller : This active LOW input interrupts any ongoing burst and causes a new external address to be latched. A READ or WRITE is performed using the new address if all chip enables are active.
D_{Q0}-D_{Q17}	Input/Output data pins

Synchronous Truth Table

$\overline{CE}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{UW}$ or $\overline{LW}$	CLK	Address Used	Operation
H	X	L	X	X	L-H	N/A	Deselected
L	L	X	X	X	L-H	Extemal Address	Read Cycle, Begin Burst
L	H	L	X	L	L-H	Extemal Address	Write Cycle, Begin Burst
L	H	L	X	H	L-H	Extemal Address	Read Cycle, Begin Burst
X	H	H	L	L	L-H	Next Address	Write Cycle, Continue Burst
X	H	H	L	H	L-H	Next Address	Read Cycle, Continue Burst
X	H	H	H	L	L-H	Current Address	Write Cycle, Suspend Burst
X	H	H	H	H	L-H	Current Address	Read Cycle, Suspend Burst
H	X	H	L	L	L-H	Next Address	Write Cycle, Continue Burst
H	X	H	L	H	L-H	Next Address	Read Cycle, Continue Burst
H	X	H	H	L	L-H	Current Address	Write Cycle, Suspend Burst
H	X	H	H	H	L-H	Current Address	Read Cycle, Suspend Burst

Notes:

1. X means don't care.
2. All inputs except $\overline{OE}$ must meet setup and hold times for the low-to-high transitions of clock(CLK).
3. Wait status are inserted by suspending burst.

Asynchronous Truth Table

Operation	$\overline{OE}$	I/O Status
Read	L	Data Out
Read	H	High-Z
Write	X	High-Z-Data in
Deselected	X	High-Z

Notes:

1. X means High or Low.
2. For a write operation following a read operation. $\overline{OE}$ must be high before the input data required setup time and held high through the input data hold time.

Absolute Maximum Ratings

Items	Symbol	Rating	Unit
Supply voltage	Vcc	-0.5 to +4.6	V
Voltage on any pins relative to Vss	V_T	-0.5 to Vcc + 0.5	V
Power dissipation	P_T	1.0	W
Operating temperature range	T_{opr}	0 to +70	°C
Storage temperature range (with bias)	$T_{Tstg(bias)}$	-10 to + 85	°C
Storage temperature range	T_{stg}	-55 to + 125	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Items	Symbol	min	max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	3.0	3.6	V
Supply Voltage to Vss	Vss	0.0	0.0	V
Input High Voltage	V_{IH}	2.2	$V_{CC}+0.5$	V
Input Low Voltage	V_{IL}	-0.5[1)]	0.8	V

Note: 1) -2.0V for undershoot pulse width $\leqq t_{KHKH}$ min / 2.

DC and Operating Characteristics (V_{CC} = 3.3V ± 0.3V, Ta = 0 to 70°C, unless otherwise noted)

Items	Symbol	Test conditions	min	max	Unit
Input Leakage Current	I_{LI}	$V_{IN} = V_{SS}$ to V_{CC}	–	±2.0	μA
Output Leakage Current	I_{LO}	$\overline{OE} = V_{IH}$	–	±2.0	μA
Supply Current	I_{CC}	Iout = 0mA, all inputs = V_{IH} or V_{IL}, cycle time ≥ t_{KHKH} min.	–	190	mA
Standby Current	I_{SB}	$\overline{CE} = V_{IH}$, other inputs = V_{IH} or V_{IL}, cycle time ≥ t_{KHKH} min.	–	TBD	mA
Output Low Voltage	V_{OL}	I_{OL} = 8mA	–	0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4mA	2.4	–	V

Capacitance (f = 1.0MHz, Ta = 25°C)

Items	Symbol	min	max	Unit
Input Capacitance	Cin	–	5	pF
Input / Output Capacitance	$C_{I/O}$	–	8	pF

Note: This parameter is sampled and not 100% tested.

AC Characteristics

(Vcc = 3.3V ± 0.3V, VSS = 0V, Ta = 0 to +70°C, unless otherwise noted)

Items	Symbol		-9		-12		Unit	Notes
	Standard	Alternate	min	max	min	max		
Cycle Time	t_{KHKH}	t_{CYC}	15	–	20	–	ns	
Clock Access Time	t_{KHQV}	t_{ACK}	–	9	–	12	ns	1
Output Enable to Output valid	t_{GLQV}	t_{OE}	–	5	–	6	ns	5
Clock High to Output Active	t_{KHQX1}	t_{CLZ}	4	–	4	–	ns	
Clock High to Output Change	t_{KHQX2}	t_{COH}	3	–	3	–	ns	
Output Enable to Output Active	t_{GLQZ}	t_{OLZ}	0	–	0	–	nS	
Output Disable to Q High-Z	t_{GHQZ}	t_{OHZ}	2	6	2	6	ns	2
Clock High to Q High-Z	t_{KHQZ}	t_{CHZ}	–	6	–	6	ns	
Clock High Pulse Width	t_{KHKL}	t_{CH}	5	–	5	–	ns	
Clock Low Pulse Width	t_{KLKH}	t_{CL}	5	–	5	–	ns	
Setup Times:			2.5	–	2.5	–	ns	3,4
Address	t_{AVKH}	t_{SA}						
Address Status	t_{ADSVKH}	t_{SADS}						
Input Data	t_{DVKH}	t_{SD}						
Byte Write	t_{WVKH}	t_{SW}						
Address Advance	t_{ADVVKH}	t_{SADV}						
Chip Enable	t_{EVKH}	t_{SCE}						
Hold Times:			0.5	–	0.5	–	ns	3,4
Address	t_{KHAX}	t_{HA}						
Address Status	t_{KHADSX}	t_{HADS}						
Input Data	t_{KHDX}	t_{HD}						
Byte Write	t_{KHWX}	t_{HW}						
Address Advance	t_{KHADVX}	t_{HADV}						
Chip Enable	t_{KHEX}	t_{HCE}						

NOTES

1. Maximum access times are guaranteed for all possible i486™ external bus cycles.
2. Transition is measured ±200mV from steady-state voltage with load of Figure B. This parameter is sampled.
3. A READ cycle is defined by byte write enables all HIGH or $\overline{ADSP}$ LOW for the required setup and hold times. A WRITE cycle is defined by at last one byte write enable LOW and $\overline{ADSP}$ HIGH for the required setup and hold times.
4. This is a synchronous device. All address must meet the specified setup and hold times for all rising edges of CLK when either $\overline{ADSP}$ or $\overline{ADSC}$ is LOW and chip enabled. All other Synchronous inputs must meet the setup and hold times with stable logic levels for all rising egdes of clock(CLK) when chip is enabled. Chip enable must be valid at each rising edge of CLK(when either $\overline{ADSP}$ or $\overline{ADSC}$ is LOW) to remain enabled
5. $\overline{OE}$ is a High or Low when a byte write enable is sampled LOW.

AC Test Conditions

Input Timing Measurement Reference Level.....1.5V Output Timing Reference Level.....1.5V

Input Pulse Levels.....0 to 3.0V Output Load....See Figure A unless otherwise noted

Input Rise/Fall Time.....2ns

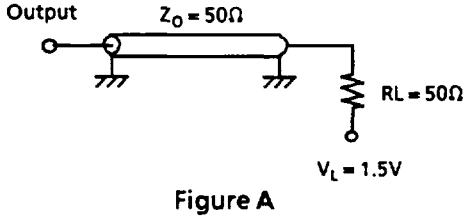


Figure A

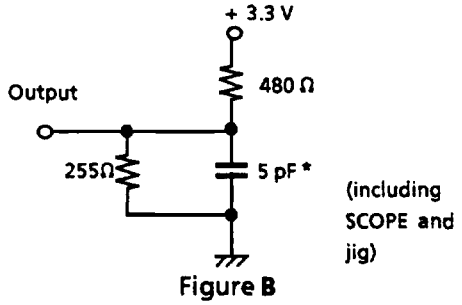
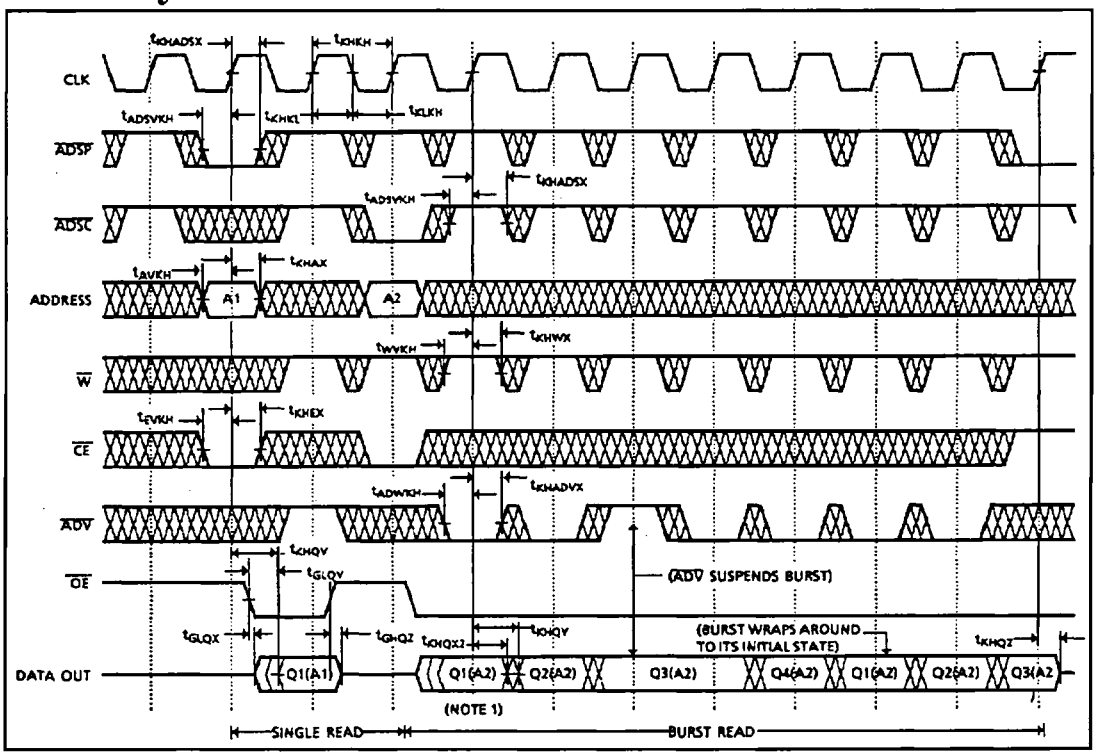


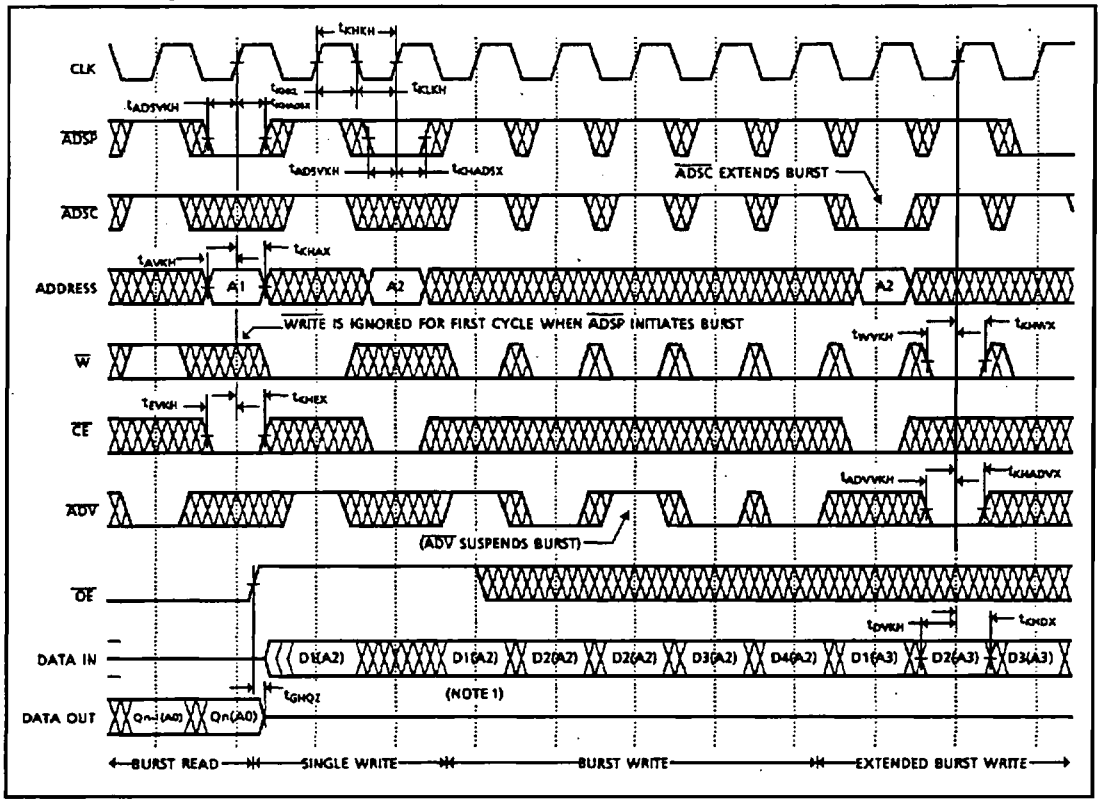
Figure B

Read Cycles

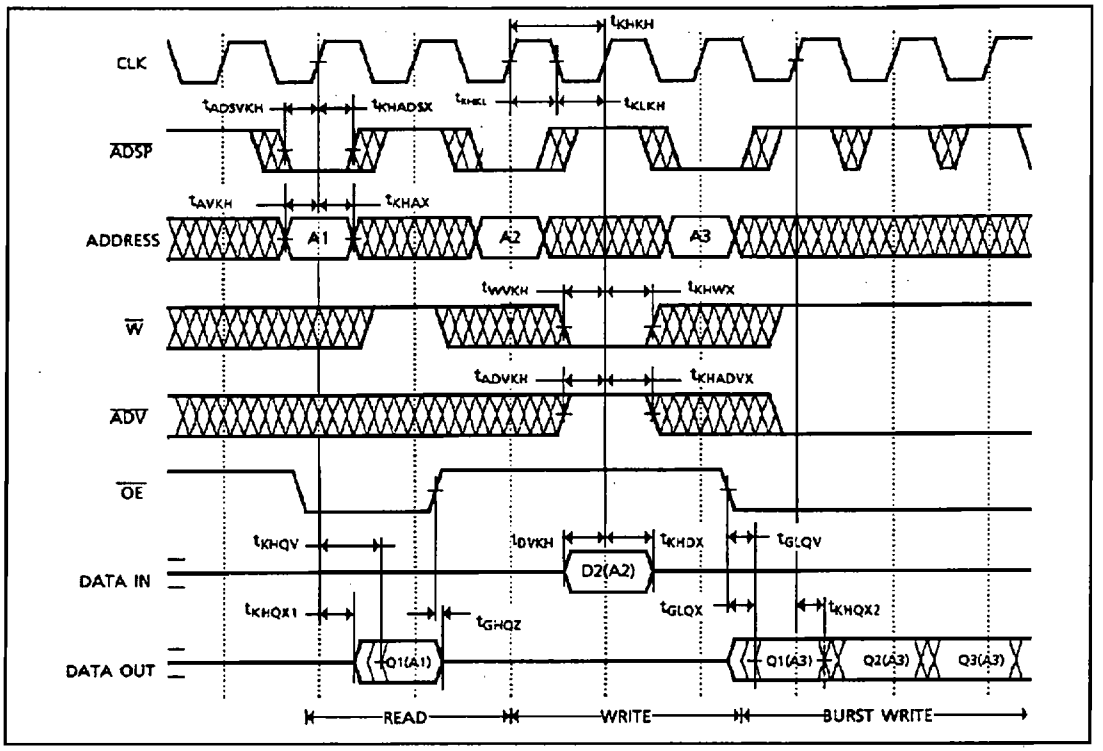


Note: 1. Q1(A2) represents the first outputs data from the base address A2; Q2(A2) represents the next outputs data in the burst sequence with A2 as the base address.

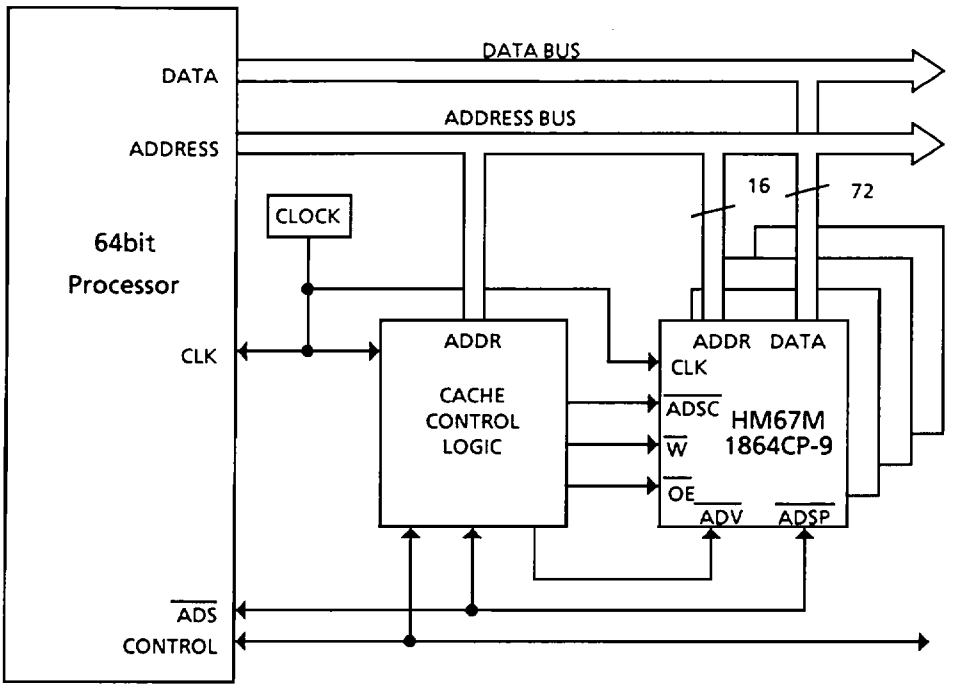
Write Cycles



Combination Read / Write Cycles



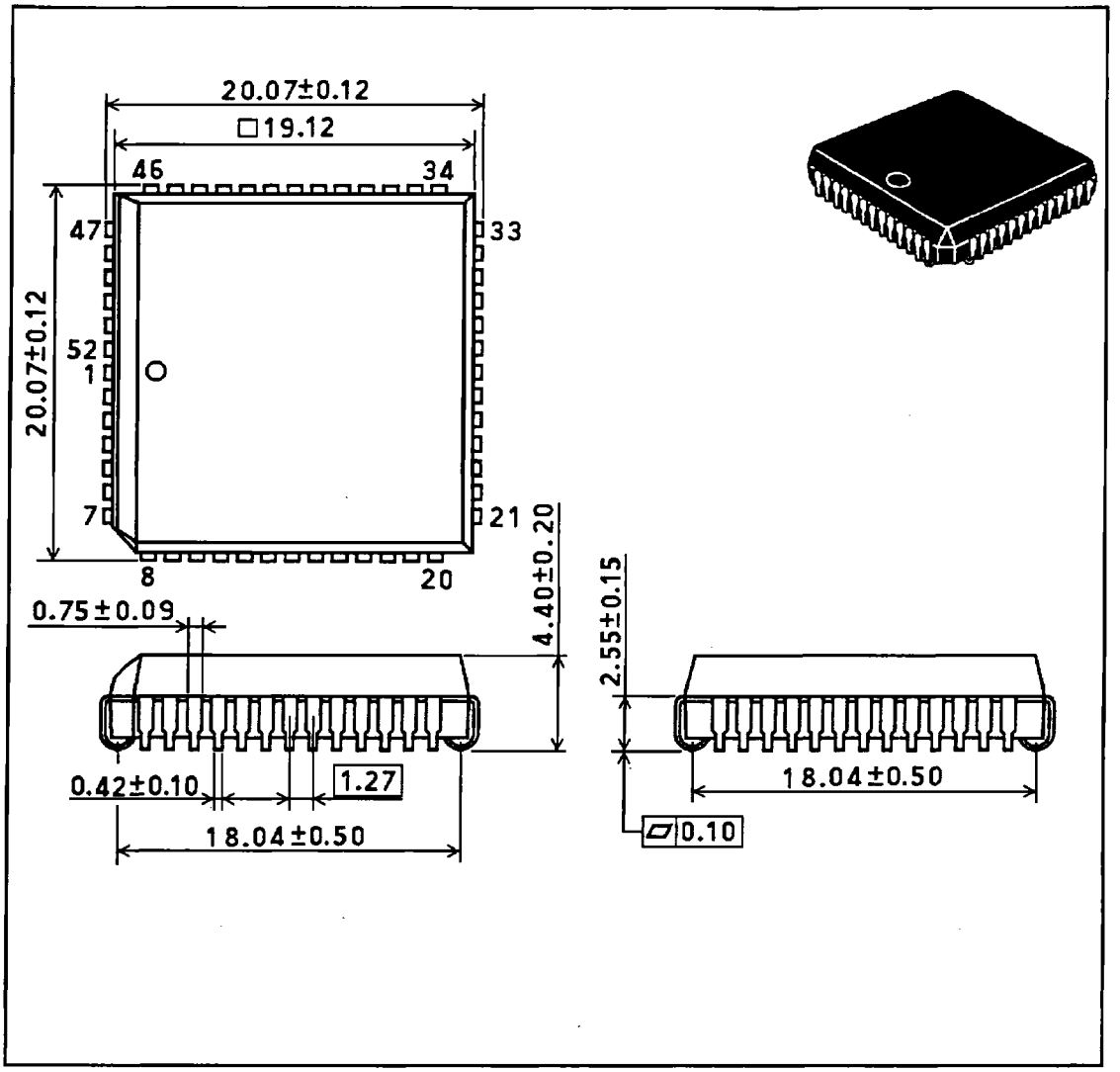
Application Examples



256K Byte Secondary Cache With Burst for 66MHz Processor
Using Four HM67M1864CP-9 Synchronous SRAM

Package Dimensions

●CP-52 Unit: mm



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Semiconductor & I.C. Division
San Francisco Center
2000 Sierra Point Parkway
Brisbane, CA 94005-1819
(415) 589-8300
Fax: (415) 583-4207

Engineering Facility
Hitachi Micro Systems, Inc.
179 East Tasman Drive
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