1M x 4 Bit CMOS Dynamic RAM with Extended Data Out

DESCRIPTION

This is a family of 1,048,576 x 4 bit Extended Data Out CMOS DRAMs. Extended Data Out offers high speed random access of memory cells within the same row. Power supply voltage(+5.0V or +3.3V), access time (-5, -6, -7 or -8), power consumption (Normal or Low power) and package type(SOJ or TSOP-II) are optional features of this family.

All of this family have $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh and Hidden refresh capabilities.

This 1Mx4 Extended Data Out DRAM family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability.

It may be used as main memory unit for microcomputer, personal computer and portable machines.

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FEATURES

- Part Identification
  - KM44C1004C/CL (5V)
  - KM44V1004C/CL (3.3V)

- Active Power Dissipation

Unit : mW

Speed	3.3V	5V
-5	-	468
-6	220	413
-7	200	358
-8	180	303

- Refresh cycles

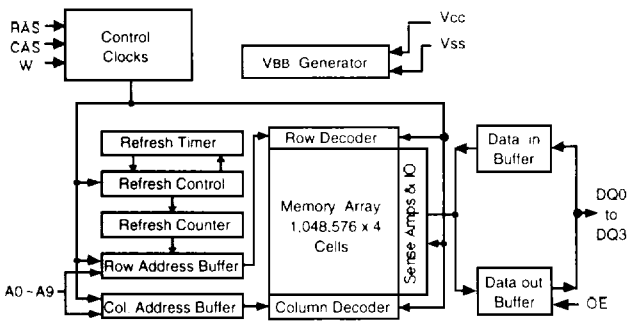
	Vcc	Refresh cycle	Refresh Period	
			Normal	L
C1004C	5V	1K	16ms	128ms
V1004C	3.3V			

- Performance range:

Speed	tRAC	tCAC	tRC	tPC	Remark
-5	50ns	15ns	90ns	35ns	5V Only
-6	60ns	15ns	110ns	40ns	5V/3.3V
-7	70ns	20ns	130ns	45ns	5V/3.3V
-8	80ns	20ns	150ns	50ns	5V/3.3V

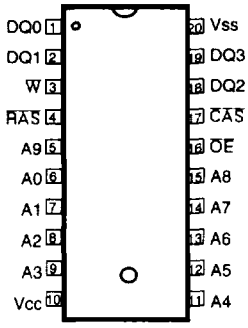
- Extended Data Out operation
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- Self-refresh capability (3.3V,L-ver only)
- TTL(5V)/LVTTL(3.3V) compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC standard pinout
- Available in plastic SOJ ,DIP ,ZIP and TSOP(II) packages
- Single +5V±10% power supply (5V product)
- Single +3.3V±0.3V power supply (3.3V product)

FUNCTIONAL BLOCK DIAGRAM

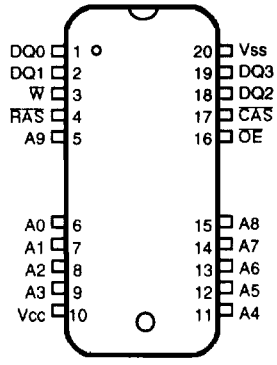


PIN CONFIGURATION (Top Views)

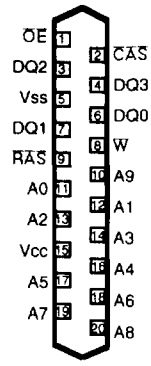
• KM44C/V1004CP



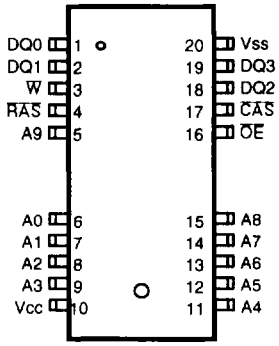
• KM44C/V1004CJ



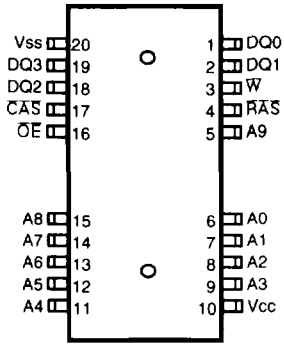
• KM44C/V1004CZ



• KM44C/V1004CT



• KM44C/V1004CTR



Pin Name	Pin Function
A0 - A9	Address Inputs
DQ0 -3	Data In/Out
V_{SS}	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Outputs Enable
V_{CC}	Power(+5.0V)
	Power(+3.3V)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Units
		3.3V	5V	
Voltage on any pin relative to V_{SS}	V_{IN},V_{OUT}	-0.5 to +4.6	-1.0 to +7.0	V
Voltage on V_{CC} supply relative to Vss	V_{CC}	-0.5 to +4.6	-1.0 to +7.0	V
Storage Temperature	Tstg	-55 to +150	-55 to +150	°C
Power Dissipation	P_D	600	600	W
Short Circuit Output Current	I_{OS}	50	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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RECOMMENDED OPERATING CONDITIONS (Voltages referenced to Vss, T_A= 0 to 70 °C)

Parameter	Symbol	3.3V			5V			Unit
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage	V_{CC}	3.0	3.3	3.6	4.5	5.0	5.5	V
Ground	Vss	0	0	0	0	0	0	V
Input High Voltage	V_{IH}	2.0	-	Vcc+0.3*1	2.4	-	Vcc+1.0*1	V
Input Low Voltage	V_{IL}	-0.3*2	-	0.8	-1.0*2	-	0.8	V

*1 : Vcc+1.3V/15ns(3.3V),Vcc+2.0V/20ns(5V), Pulse width is measured at Vcc

*2 : -1.3V/15ns(3.3V), -2.0V/20ns(5V),Pulse width is measured atVss

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

	Parameter	Symbol	Min	Max	Units
3.3V	Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.3V, all other pins not under test=0V)	$I_{I(L)}$	-5	5	μA
	Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤Vcc)	$I_{O(L)}$	-5	5	μA
	Output High Voltage Level (I_{OH}=-2mA)	V_{OH}	2.4	-	V
	Output Low Voltage Level (I_{OL}=2mA)	V_{OL}	-	0.4	V
5V	Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.5V, (Any input 0≤V_{IN}≤Vcc+0.5V, all other pins not under test=0V)	$I_{I(L)}$	-5	5	μA
	Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤Vcc)	$I_{O(L)}$	-5	5	μA
	Output High Voltage Level (I_{OH}=-5mA)	V_{OH}	2.4	-	V
	Output Low Voltage Level (I_{OL}=4.2mA)	V_{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Symbol	Power	Speed	Max		Units
			KM44V1004C	KM44C1004C	
I_{CC1}	Don't care	-5	-	85	mA
		-6	60	75	mA
		-7	55	65	mA
		-8	50	55	mA
I_{CC2}	Don't care	Don't care	1	2	mA
I_{CC3}	Don't care	-5	-	85	mA
		-6	60	75	mA
		-7	55	65	mA
		-8	50	55	mA
I_{CC4}	Don't care	-5	-	85	mA
		-6	60	75	mA
		-7	55	65	mA
		-8	50	55	mA
I_{CC5}	Normal	Don't care	0.5	1	mA
	L		100	200	µA
I_{CC6}	Don't care	-5	-	85	mA
		-6	60	75	mA
		-7	55	65	mA
		-8	50	55	mA
I_{CC7}	L	Don't care	200	300	µA
I_{CCS}	L	Don't care	150	-	µA

I_{CC1}* : Operating current ($\overline{RAS}$, $\overline{CAS}$, Address cycling @tRC=min.)

I_{CC2} : Standby current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3}* : $\overline{RAS}$-only refresh current ($\overline{CAS}$=V_{IH}, $\overline{RAS}$, Address cycling @tRC=min.)

I_{CC4}* : EDO Mode current ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address cycling @tPC=min.)

I_{CC5} : Standby current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{CC}-0.2V)

I_{CC6}* : $\overline{CAS}$-before-$\overline{RAS}$ Refresh current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

I_{CC7} : Battery back-up current, Average power supply current, Battery back-up mode

Input high voltage(V_{IH})=Vcc-0.2V, Input low voltage(V_{IL})=0.2V, $\overline{CAS}$= 0.2V

DQ0~3 = Don't care, T_{RC}=125µs, T_{RAS}=T_{RAS} min~300 ns

I_{CCS} : Self refresh current

$\overline{RAS}$=$\overline{CAS}$=V_{IL}, $\overline{W}$=$\overline{OE}$=A0 ~ A9 = V_{CC}-0.2V or 0.2V,

DQ0 ~ DQ3= V_{CC}-0.2V, 0.2V or open

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1} , I_{CC3} and I_{CC6}, address can be changed maximum two times while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one hyper page cycle.

CAPACITANCE (T_A=25°C, Vcc=5V or 3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance [A0 ~ A9]	C_{IN1}	-	5	pF
Input capacitance [$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$]	C_{IN2}	-	7	pF
Output Capacitance [DQ0 ~ DQ3]	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, See note 1,2)

Test condition (5V device) : Vcc=5.0V±10%, V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.0/0.8V
Test condition (3.3V device) : Vcc=3.3V±0.3V, V_{ih}/V_{il}=2.0/0.8V, V_{oh}/V_{ol}=2.0/0.8V

Parameter	Symbol	-5 *1		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	84		104		124		144		ns	
Read-modify-write cycle time	tRWC	116		140		165		190		ns	
Access time from $\overline{RAS}$	tRAC		50		60		70		80	ns	3,4,10
Access time from $\overline{CAS}$	tCAC		13		15		20		20	ns	3,4,5
Access time from column address	tAA		25		30		35		40	ns	3,10
$\overline{CAS}$ to output in Low-Z	tCLZ	3		3		3		3		ns	3
Output buffer turn-off delay from $\overline{CAS}$	tCEZ	3	13	3	15	3	20	3	20	ns	7,13
Transition time (rise and fall)	tT	2	50	2	50	2	50	2	50	ns	2
$\overline{RAS}$ precharge time	tRP	30		40		50		60		ns	
$\overline{RAS}$ pulse width	tRAS	50	10K	60	10K	70	10K	80	10K	ns	
$\overline{RAS}$ hold time	tRSH	13		15		20		20		ns	
$\overline{CAS}$ hold time	tCSH	40		50		60		70		ns	
$\overline{CAS}$ pulse width	tCAS	8	10K	10	10K	15	10K	20	10K	ns	11
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	33	20	43	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	tRAD	15	25	15	30	15	35	15	40	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		5		ns	
Row address set-up time	tASR	0		0		0		0		ns	
Row address hold time	tRAH	10		10		10		10		ns	
Column address set-up time	tASC	0		0		0		0		ns	
Column address hold time	tCAH	8		10		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	tAR	35		42		52		57		ns	17
Column address to $\overline{RAS}$ lead time	tRAL	25		30		35		40		ns	
Read command set-up time	tRCS	0		0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		0		ns	8
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		0		ns	8
Write command hold time	tWCH	10		10		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	tWCR	37		42		52		57		ns	17
Write command pulse width	tWP	10		10		15		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	13		15		20		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	8		10		15		20		ns	

Note) *1 : 5V only

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, See note 1,2)

Parameter	Symbol	-5*1		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Data set-up time	tDS	0		0		0		0		ns	9
Data hold time	tDH	8		10		15		15		ns	9
Data hold time referenced to $\overline{RAS}$	tDHR	35		42		52		57		ns	17
Refresh period(Normal)	tREF		16		16		16		16	ms	
Refresh period(L-ver)	tREF		128		128		128		128	ms	
Write command set-up time	tWCS	0		0		0		0		ns	7
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	30		34		44		44		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	67		79		89		99		ns	7
Column address to $\overline{W}$ delay time	tAWD	42		49		59		64		ns	7
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	45		54		64		69		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	5		5		5		5		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		15		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		5		ns	
$\overline{CAS}$ precharge time($\overline{CBR}$ counter test cycle)	tCPT	20		20		25		30		ns	
Access time from $\overline{CAS}$ precharge	tCPA		28		35		40		45	ns	3
Hyper Page mode cycle time	tHPC	20		25		30		35		ns	15
Hyper Page mode read-modify-write cycle time	tHPRWC	47		56		71		81		ns	
$\overline{CAS}$ precharge time (Hyper page cycle)	tCP	8		10		10		10		ns	
$\overline{RAS}$ pulse width (Hyper page cycle)	tRASP	50	200K	60	200K	70	200K	80	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	30		35		40		45		ns	
$\overline{OE}$ access time	tOEA		13		15		20		20	ns	
$\overline{OE}$ to data delay	tOED	13		15		20		20		ns	
Out put buffer turn off delay time from $\overline{OE}$	tOEZ	3	13	3	15	3	20	3	20	ns	6,13
$\overline{OE}$ to output in low-Z	tOLZ	3		3		3		3		ns	
$\overline{OE}$ command hold time	tOEH	13		15		20		20		ns	
Output data hold time	tDOH	5		5		5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	tREZ	3	13	3	15	3	20	3	20	ns	6,13
Output buffer turn off delay from $\overline{W}$	tWEZ	3	13	3	15	3	20	3	20	ns	6,13
$\overline{W}$ to data delay	tWED	15		15		20		20		ns	
$\overline{OE}$ to $\overline{CAS}$ hold time	tOCH	5		5		5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	tCHO	5		5		5		5		ns	
$\overline{OE}$ precharge time	tOEP	5		5		5		5		ns	
$\overline{W}$ pulse width (hyper page cycle)	tWPE	5		5		5		5		ns	
$\overline{RAS}$ pulse width($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		100		100		µs	16
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	90		110		130		150		ns	16
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	-50		-50		-50		-50		ns	16

Note) *1 : 5V only

TEST MODE CYCLE

(Note. 11)

Parameter	Symbol	-5*1		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	89		109		129		149		ns	
Read-modify-write cycle time	tRWC	121		145		170		195		ns	
Access time from $\overline{RAS}$	tRAC		55		65		75		85	ns	3,4,10
Access time from $\overline{CAS}$	tCAC		18		20		25		25	ns	3,4,5
Access time from column address	tAA		30		35		40		45	ns	3,10
$\overline{RAS}$ pulse width	tRAS	55	10K	65	10K	75	10K	85	10K	ns	
$\overline{CAS}$ pulse width	tCAS	13	10K	15	10K	20	10K	25	10K	ns	
$\overline{RAS}$ hold time	tRSH	18		20		25		25		ns	
$\overline{CAS}$ hold time	tCSH	45		55		65		75		ns	
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		45		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	35		39		49		49		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	72		84		94		104		ns	7
Column address to $\overline{W}$ delay time	tAWD	47		54		64		69		ns	7
Hyper Page mode cycle time	tHPC	25		30		35		40		ns	15
Hyper page mode read-modify-write cycle time	tPRWC	52		61		76		86		ns	
$\overline{RAS}$ pulse width (Hyper page cycle)	tRASP	55	200K	65	200K	75	200K	85	200K	ns	
Access time form $\overline{CAS}$ precharge	tCPA		33		40		45		50	ns	3
$\overline{OE}$ access time	tOEA		18		20		25		25	ns	
$\overline{OE}$ to data delay	tOED	18		20		25		25		ns	
$\overline{OE}$ command hold time	tOEH	18		20		25		25		ns	

Note) *1 : 5V only

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 2ns for all inputs.
3. Measured with a load equivalent to 2 TTL(5V)/1 TTL(3.3V) loads and 100pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD≥ tRCD(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
7. tWCS, tRWD, tCWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If tWCS≥ tWCS(min), the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD≥ tCWD(min), tRWD≥ tRWD(min) and tAWD≥ tAWD(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either tRCH or tRRH must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-modify write cycles.
10. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
11. These specifications are applied in the test mode.
12. In test mode read cycle, the value of tRAC, tAA, tCAC is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
13. tCEZ(max),tREZ(max),tOEZ(max) and tWEZ(max) define the time at which the output achives the open circuit condition and are not referenced to output voltage level.
14. If $\overline{RAS}$ goes high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes high before $\overline{RAS}$ high going, the open circuit condition of the output is achieved by $\overline{RAS}$ high going.
15. tASC≥6ns, Assume tT=2.0ns.
16. 1024 cycles of burst refresh must be executed within 16ms before and after self refresh,in order to meet refresh specification.(3.3V L-Ver.)
17. tAR , tWCR ,tDHR are referenced to tRAD(max).