MSC2312B-xxYS9/KS9

1,048,576-Word by 9-Bit DRAM Module: Fast Page Mode

DESCRIPTION

The OKI MSC2312B-xxYS9/KS9 is a fully decoded 1,048,576-word x 9-bit CMOS Dynamic Random Access Memory Module composed of nine 1-Mb DRAMs in SOJ (MSM511000B) packages mounted with nine 0.2 µF decoupling capacitors on a 30-pin glass epoxy single-inline package. This module is generally used for memory expansion in parity applications such as workstations.

FEATURES

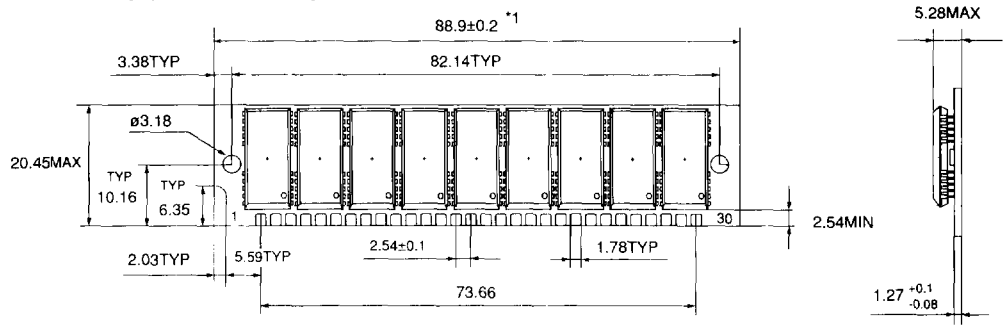
- 1-Meg x 9-bit organization
  - MSC2312B-xxYS9: Socket insertable module
  - MSC2312B-xxKS9: Pin through-hole module
- Single +5 V supply ±10 % tolerance
- Access times: 60, 70, 80, 100 ns
- Input: TTL compatible
- Output: TTL compatible, three-state
- Refresh: 512 cycles/8 ms
- $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{CAS}$-before-$\overline{RAS}$ hidden refresh, $\overline{RAS}$-only refresh capability

Family Organization

Part Number	Access Time (Max)			Cycle Time (Min)	Power Dissipation (Max)	
	t_{RAC}	t_{AA}	t_{CAC}		Operating	Standby
MSC2312B-60YS9/KS9	60 ns	30 ns	15 ns	120 ns	4455 mW	49.5 mW (MOS level)
MSC2312B-70YS9/KS9	70 ns	35 ns	20 ns	130 ns	3960 mW	
MSC2312B-80YS9/KS9	80 ns	40 ns	20 ns	150 ns	3465 mW	
MSC2312B-10YS9/KS9	100 ns	50 ns	25 ns	190 ns	2970 mW	

PIN CONFIGURATION

MSC2312B-xxYS9



*1 The common size difference of the board width, 12.5 mm of its height, is specified as ±0.2. The value above 12.5 mm is specified as ±0.5.

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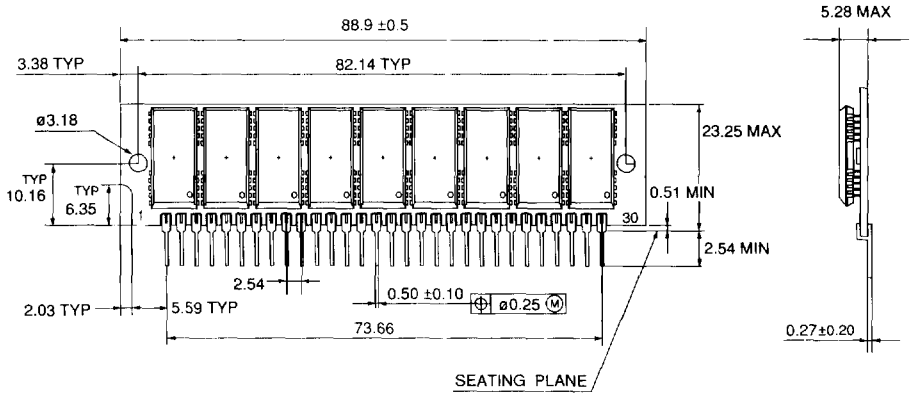
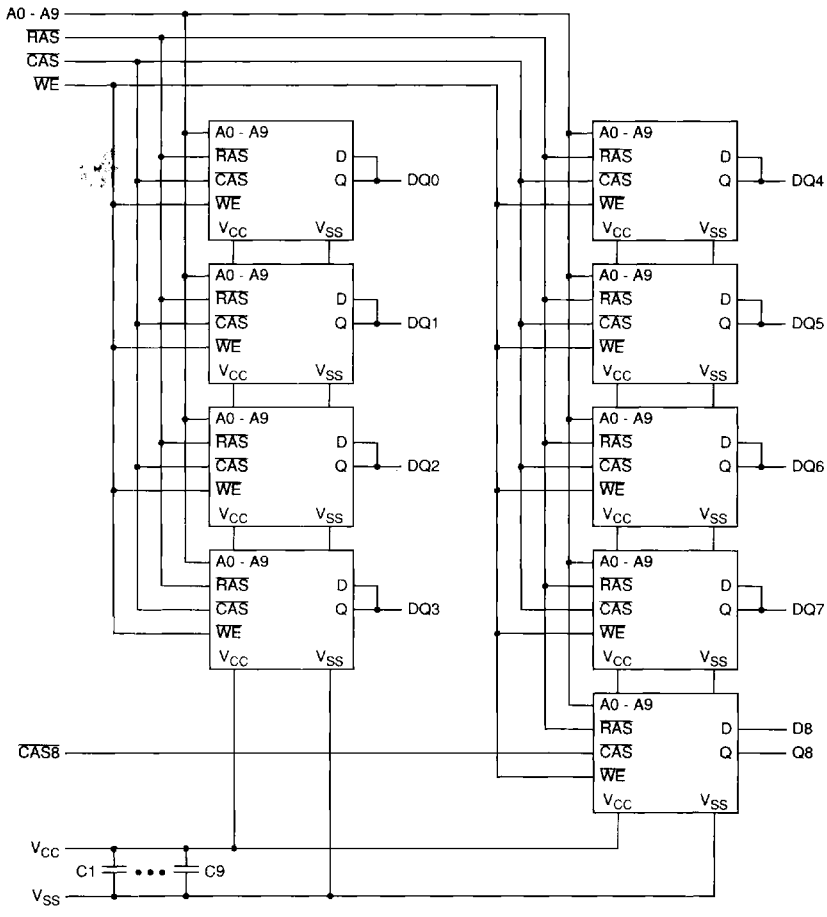


Pin Configuration

Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name
1	V_{CC}	11	A4	21	$\overline{WE}$
2	$\overline{CAS}$	12	A5	22	V_{SS}
3	DQ0	13	DQ3	23	DQ6
4	A0	14	A6	24	N.C.
5	A1	15	A7	25	DQ7
6	DQ1	16	DQ4	26	Q8
7	A2	17	A8	27	$\overline{RAS}$
8	A3	18	A9	28	$\overline{CAS8}$
9	V_{SS}	19	N.C.	29	D8
10	DQ2	20	DQ5	30	V_{CC}

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings [1]

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-1.0 ~ +7.0	V
Voltage V_{CC} supply relative to V_{SS}	V_{CC}	-1.0 ~ +7.0	V
Short circuit output current	I_{OS}	50	mA
Power dissipation	P_D	9	W
Operating temperature	T_{OPR}	0 ~ +70	°C
Storage temperature	T_{STG}	-40 ~ +125	°C

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions (T_a = 0 ~+70°C)

Parameter	Symbol	Rated Value			Unit
		Min	Typ	Max	
Power supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input high voltage	V_{IH}	2.4	-	6.5	V
Input low voltage	V_{IL}	-1.0	-	0.8	V

Capacitance (T_a = 25°C, f = 1 MHz) [1]

Parameter	Symbol	Typ	Max	Unit
Input capacitance (A0 ~ A9)	C_{IN1}	-	81	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	-	83	pF
I/O capacitance (DQ0 ~ DQ7)	C_{DQ}	-	23	pF
Input capacitance ($\overline{CAS8}$)	C_{IN3}	-	27	pF
Input capacitance (D8)	C_{IN4}	-	16	pF
Output capacitance (Q8)	C_{OUT}	-	17	pF

1. Capacitance measured with Boonton Meter.

DC Characteristics (V_{CC} = 5 V ±10%, T_a = 0°C ~ +70°C)

Parameter	Symbol	Condition		60 ns Min	60 ns Max	70 ns Min	70 ns Max	80 ns Min	80 ns Max	100 ns Min	100 ns Max	Unit	Note
Input leakage current	I_{LI}	0 V ≤ V_I ≤ 6.5 V; All other pins not under test = 0 V		-90	90	-90	90	-90	90	-90	90	µA	
Output leakage current	I_{LO}	D_{OUT} disable 0 V ≤ V_O ≤ 5.5 V		-10	10	-10	10	-10	10	-10	10	µA	
Output high voltage	V_{OH}	I_{OH} = -5.0 mA		2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output low voltage	V_{OL}	I_{OL} = 4.2 mA		0	0.4	0	0.4	0	0.4	0	0.4	V	
Average power supply current (Operating)	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = min.		-	810	-	720	-	630	-	540	mA	[1] [2]
Power supply current (Standby)	I_{CC2}	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IH} D_{OUT} = Hi-Z	TTL	-	18	-	18	-	18	-	18	mA	
			MOS	-	9	-	9	-	9	-	9	mA	
Average power supply current ($\overline{RAS}$-only refresh)	I_{CC3}	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = min.		-	810	-	720	-	630	-	540	mA	[1] [2]
Average power supply current ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	I_{CC6}	$\overline{RAS}$ cycling, $\overline{CAS}$-before-$\overline{RAS}$, t_{RC} = min.		-	810	-	720	-	630	-	540	mA	[1]
Average power supply current (Fast Page Mode)	I_{CC7}	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling, t_{PC} = min.		-	720	-	630	-	540	-	495	mA	[1] [3]

1. I_{CC} depends on output loading and cycle rates. Specified values are obtained with the output open.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

AC Characteristics (V_{CC} = 5 V ±10%, T_a = 0°C ~ +70°C) [1] [2] [3]

Parameter	Symbol	60 ns		70 ns		80 ns		100 ns		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	120	-	130	-	150	-	190	-	ns	
Fast Page Mode cycle time	t_{PC}	40	-	45	-	50	-	55	-	ns	
Access time from $\overline{RAS}$	t_{RAC}	-	60	-	70	-	80	-	100	ns	[4] [5] [6]
Access time for $\overline{CAS}$	t_{CAC}	-	15	-	20	-	20	-	25	ns	[4] [5]
Access time from column address	t_{AA}	-	30	-	35	-	40	-	50	ns	[4] [6]
Access time from $\overline{CAS}$ precharge	t_{CPA}	-	35	-	40	-	45	-	50	ns	[4]
Output low impedance time from $\overline{CAS}$	t_{CLZ}	0	-	0	-	0	-	0	-	ns	
Output buffer turn-off delay time	t_{OFF}	0	20	0	20	0	20	0	20	ns	[7]
Transition time	t_T	3	50	3	50	3	50	3	50	ns	[3]
Refresh period	t_{REF}	-	8	-	8	-	8	-	8	ms	
$\overline{RAS}$ precharge time	t_{RP}	50	-	50	-	60	-	80	-	ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10K	70	10K	80	10K	100	10K	ns	
$\overline{RAS}$ pulse width (Fast Page Mode)	t_{RASP}	60	100K	70	100K	80	100K	100	100K	ns	
$\overline{RAS}$ hold time	t_{RSH}	15	-	20	-	20	-	25	-	ns	
$\overline{CAS}$ precharge time (Fast Page Mode)	t_{CP}	10	-	10	-	10	-	10	-	ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10K	20	10K	20	10K	25	10K	ns	
$\overline{CAS}$ hold time	t_{CSH}	60	-	70	-	80	-	100	-	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	-	5	-	5	-	5	-	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	25	75	ns	[5]
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	20	50	ns	[6]
Row address set-up time	t_{ASR}	0	-	0	-	0	-	0	-	ns	
Row address hold time	t_{RAH}	10	-	10	-	10	-	15	-	ns	
Column address set-up time	t_{ASC}	0	-	0	-	0	-	0	-	ns	
Column address hold time	t_{CAH}	15	-	15	-	15	-	20	-	ns	
Column address hold time from $\overline{RAS}$	t_{AR}	50	-	55	-	60	-	75	-	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30	-	35	-	40	-	50	-	ns	
Read command set-up time	t_{RCS}	0	-	0	-	0	-	0	-	ns	
Read command hold time	t_{RCH}	0	-	0	-	0	-	0	-	ns	[8]
Read command hold time reference to $\overline{RAS}$	t_{RRH}	0	-	0	-	0	-	0	-	ns	[8]
Write command set-up time	t_{WCS}	0	-	0	-	0	-	0	-	ns	
Write command hold time	t_{WCH}	10	-	15	-	15	-	20	-	ns	
Write command hold time from $\overline{RAS}$	t_{WCR}	50	-	55	-	60	-	75	-	ns	
Write command pulse width	t_{WP}	10	-	15	-	15	-	20	-	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15	-	20	-	20	-	25	-	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	15	-	20	-	20	-	25	-	ns	
Data-in set-up time	t_{DS}	0	-	0	-	0	-	0	-	ns	
Data-in hold time	t_{DH}	15	-	15	-	15	-	20	-	ns	

AC Characteristics (V_{CC} = 5 V ±10%, T_a = 0°C ~ +70°C) [1] [2] [3] (Continued)

Parameter	Symbol	60 ns		70 ns		80 ns		100 ns		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Data-in hold time from $\overline{RAS}$	t_{DHR}	50	-	55	-	60	-	75	-	ns	
$\overline{CAS}$ active delay from $\overline{RAS}$ precharge	t_{RPC}	10	-	10	-	10	-	10	-	ns	
$\overline{RAS}$ to $\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$)	t_{CSR}	10	-	10	-	10	-	10	-	ns	
$\overline{RAS}$ to $\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$)	t_{CHR}	30	-	30	-	30	-	30	-	ns	
$\overline{CAS}$ precharge time (Refresh counter test)	t_{CPT}	40	-	40	-	40	-	50	-	ns	

1. A start-up delay of 100 µs is required after power-up followed by a minimum of eight initialization cycles ($\overline{RAS}$-only refresh or $\overline{CAS}$-before-$\overline{RAS}$ refresh) before proper device operation is achieved. When using the internal refresh counter, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles is required.
2. AC measurements assume t_T = 5 ns.
3. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring input timing signals. Transition times are measured between V_{IH} and V_{IL}.
4. Measured with a load circuit equivalent to 2 TTL + 100 pF.
5. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max.) limit, access time is controlled by t_{CAC}.
6. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, access time is controlled by t_{AA}.
7. t_{OFF} (max.) defines the time at which the output achieves an open circuit condition and is not referenced to output voltage levels.
8. t_{RCH} or t_{RRH} must be satisfied for a read cycle.

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See ADDENDUM B for AC Timing Waveforms