CHAPTER 9: ELECTRICAL DATA

9.1 Maximum Ratings

Ambient Operating Temperature: 0° C to + 70° C
Storage Temperature: 65° C to + 150° C
Supply Voltage to Ground Potential: -0.5 V to + 7.0 V
Applied Input Voltage: -0.5 V to + 7.0 V

Stresses above those listed may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

9.2 DC Specifications

TA = 0° C to 70° C, VDD = 5V +/- 5%, VSS = 0V

Symbol	Parameter	Min	Max	Unit	Condition	Notes
Voh	Output High Voltage	2.4		V	Ioh = 400 uA	
Vol	Output Low Voltage		0.4	V	Iol = 24 mA	1,2
Vol	Output Low Voltage		0.4	V	Iol = 8 mA	3
Vol	Output Low Voltage		0.4	V	Iol = 4 mA	4
Vol	Output Low Voltage		0.4	V	Iol = 2 mA	5
Vih	Input High Voltage	2	VCC+0.5	V	TTL	6
Vil	Input Low Voltage	-0.5	0.8	V	TTL	6
Vis	Schmitt Input Voltage	2.4	VCC+0.5	V	Schmitt	6
Vic	CMOS Input Voltage	3.8	VCC+0.5	V	CMOS	6
ILI	Input Leakage Current	-10	10	uA		
OLI	Output Leakage Current	-10	10	uA		
ICC	Operating Supply Current typical normal operation typical power down	 180 80		 mA mA		
CI	Input Capacitance		8	pF		
CO	Output Capacitance		8	pF		
CIO	I/O Capacitance		8	pF		

Notes: Other than ISA bus interface and Monitor interface, there is no DC requirements on the outputs. The other interfaces only have AC requirements.

1. Output Current (Iol) Capabilities:
   24mA: SD[15:0],CINTn, M16, ZEROWSn, IO16n, IOCHRDY, (all the ISA output pins).
2. Open Drain Outputs:
   24mA: IOCHRDY, CINTn, IO16n, M16n, ZEROWSn (ISA)
3. 8mA: HSYNC, VSYNC, RASLn, CASLn/WELn, MA[7:0], CASHIn/WEHIn/MA[8], RASHn/MA[9], PCLK, P[15:0], PAR, REQn, SD[31:16], LBSELn, C/BE[3:0],FRAMEn, IRDYn, TRDYn, DEVSELn, STOPn, LOCKn
4. 4mA: P[23:16], SRCK, SRD, WEAn/CASAn, WEBn/CASBn, WECn/CASCn, WEDn/CASDn, WEEn/CASEn, WEFn/CASFn, WEGn/CASGn, WEHn/CASHn,BLANKn
5. 2mA: CSEL[3]/EEPCS, CSEL[2]/EEPSK, CSEL[1]/EEPWD, CSEL[0]/EEPRD, ROMENLn, VDVALID, MDMXn, ARDn, AWRn, BD[7:0], DACWRn, DACRDn, ARS[3:0], MD[63:0]
6. Input Structures:
   TTL: All inputs
   TTL w/pull-ups: ESYNC, EPDATA, EPCLK

9.3 AC Specifications

All AC Timing Diagrams are strictly to show relative timing from one signal to the next. These diagrams are not necessarily logically correct or complete. For better understanding of logical cycles for ISA, VL and PCI bus, please refer to the respective specifications.

The AC values in here are preliminary **design** values.

9.3.1 ISA Bus Timing

ISA Memory Read/Write Timing

No	Symbol	Parameter	Min (ns)	Max (ns)	Load (pF)	Notes
	tBCLK	*ISA Bus Clock Period*	*80*			1
ISA1	tALE	ALE Active to Inactive	40			
ISA2	tLAS	LA[23:17] Setup to Falling Edge of ALE	15			
ISA3	tLAH	LA[23:17] Hold from Falling Edge of ALE	10			
ISA4	tM16	M16n Active from Valid LA[23:17]		40	200	
ISA5	tASMC	SA[16:0] & BHEn Setup to Memory Command Active	20			
ISA6	tAHMC	SA[16:0] & BHEn Hold to Memory Command Inactive	20			
ISA7	tMCP	Memory Command Pulse Width	80			
ISA8	t0WS	ZEROWSn Delay from Command		10	200	
ISA9	tMRDY	IOCHRDY Inactive from Memory Command Active		30	200	
ISA10	tDVMR	Read Data Valid from MRDn Active		160	200	2
ISA11	tDVRDY	Read Data Valid from IOCHRDY Active		50	200	
ISA12	tDHMR	Read Data Hold from MRDn Inactive	0		200	
ISA13	tDSMW	Write Data Setup to MRWn Active	-45			
ISA14	tDHMW	Write Data Hold from MWRn Inactive	15			

Notes:

1. This parameter is for reference only. It is intended to be the recommanded maximum bus speed. The design of this controller, however, is asynchronous to the BCLK, and therefore theoretically can run at any BCLK, as long as setup, hold and propagation delay timings meet all the above specifications.
2. tDVMR is valid for memory mapped I/O only, which is standard memory read cycle (1 wait state). Normal read access to graphics memory requires wait states, and only tDVRDY is of interest.

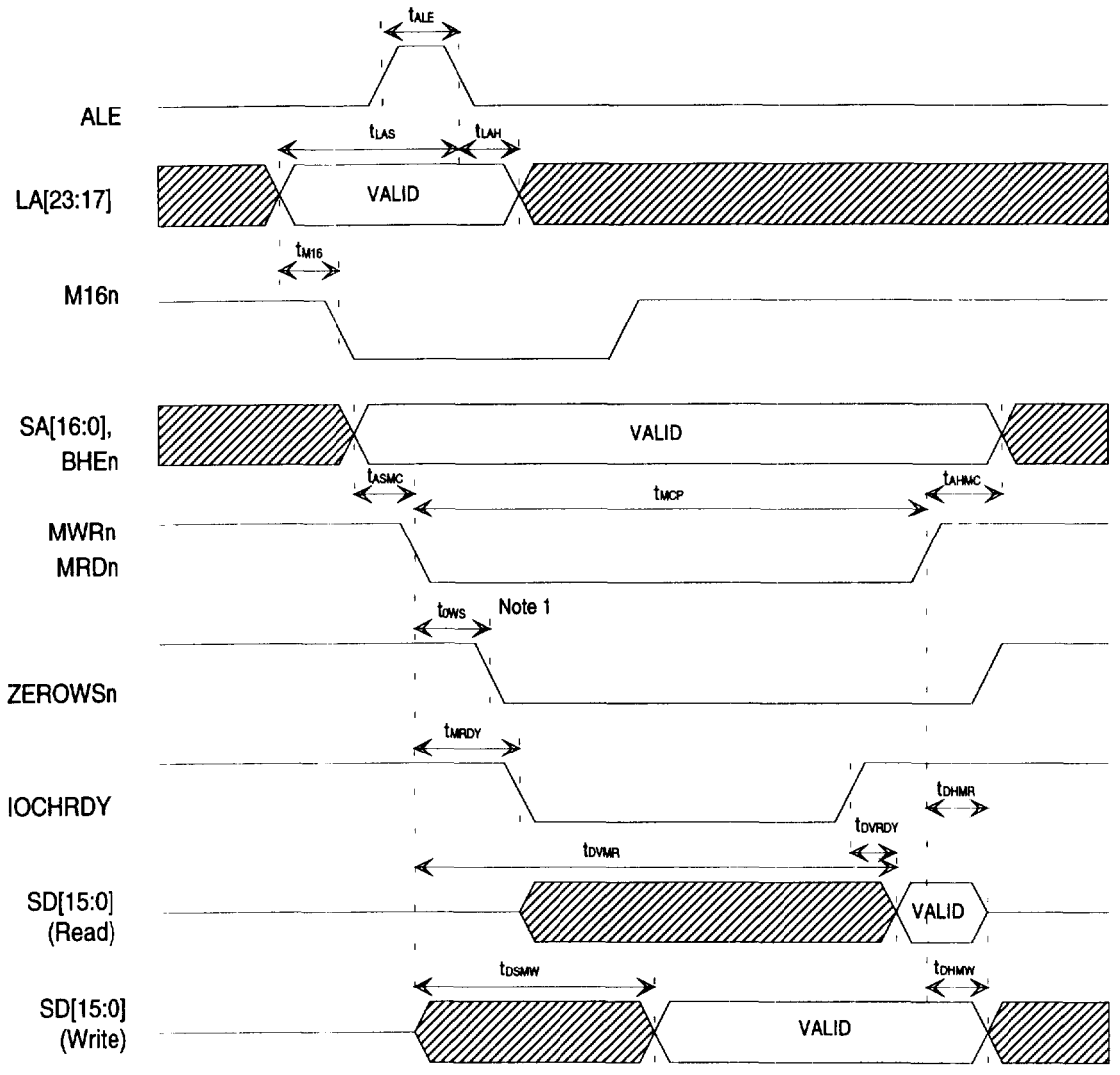


Figure 9.1 - ISA Memory Read/Write Timing

Notes: ZEROWSn and IOCHRDY are mutually exclusive, only one signal can be active at a time. The drawing merely indicates the AC timing of the signals, but not the actual logical cycle timing.

ISA ROM Read Timing

No	Symbol	Parameter	Min (ns)	Max (ns)	Load (pF)	Notes
ISA1	tALE	ALE Active to Inactive	40			
ISA2	tLAS	LA[23:17] Setup to Falling Edge of ALE	15			
ISA3	tLAH	LA[23:17] Hold from Falling Edge of ALE	10			
ISA4	tM16	M16n Active from Valid LA[23:17]		40	200	1
ISA5	tASMC	SA[16:0] & BHEn Setup to Memory Command Active	23			4
ISA6	tAHMC	SA[16:0] & BHEn Hold from Memory Command Inactive	20			
ISA7	tMCP	Memory Read Command Pulse Width	80			3
ISA15	tRE	ROMENLn Active from MRDn Active		40	50	1,4
	tROMA	*ROM Data Valid from SA[14:0]*		*148/448*	50	2,3,4
	tROME	*ROM Data Valid from MRDn*		*125/425*	50	2,4
ISA16	tBDSD	BD[7:0] Valid to SD[15:0] Valid		35	200	4
	t244P	*ROM Data Valid to SD[15:8] Valid through 244 Buffer*		*35*	200	1,4,5
ISA10	tDVMR	Read Data Valid from MRDn Active		160/460	200	3,4,6
ISA12	tDHMR	Read Data Hold from MRDn Inactive	0		200	

Notes:
1. These parameters are relevant only for 16-bit ROM (2 parts). For 8-bit ROM, M16n is not generated, ROMENLn is a "don't care", and no additional buffer is required.
2. This specification is for reference only. This is the required ROM access timing. Depending on tASMC, tROMA or tROME can be used to select the correct ROM speed. In general, 120ns ROM should be used for 8.33MHz. Faster buses will require faster ROMs. See note 4 for more details.
3. A/B where A is for 16-bit ROM, and B is for 8-bit ROM.
4. tDVMR is the specification that must be met. The calculation for tDVMR is not straight forward. If tROMA-tROME>tASMC, then tDVMR=tROMA-tASMC+tBDSD for 8-bit ROM, or for SD[7:0] of 16-bit ROM, and, tDVMR=tROMA-tASMC+t244 for SD[15:8] of 16-bit ROM. If tASMC>tROMA-tROME, then tDVMR=tROME+tBDSD for 8-bit ROM, or for SD[7:0] of 16-bit ROM, and, tDVMR=tROME+t244 for SD[15:8] of 16-bit ROM.
5. This specification is for reference only. The general rule of thumb is that the speed of the 244 buffer should not be more than tBDSD. See note 4 for more details.
6. tDVMR as specified here is based on 8.33MHz bus, this number is reduced for faster buses, but there is no standard for it.

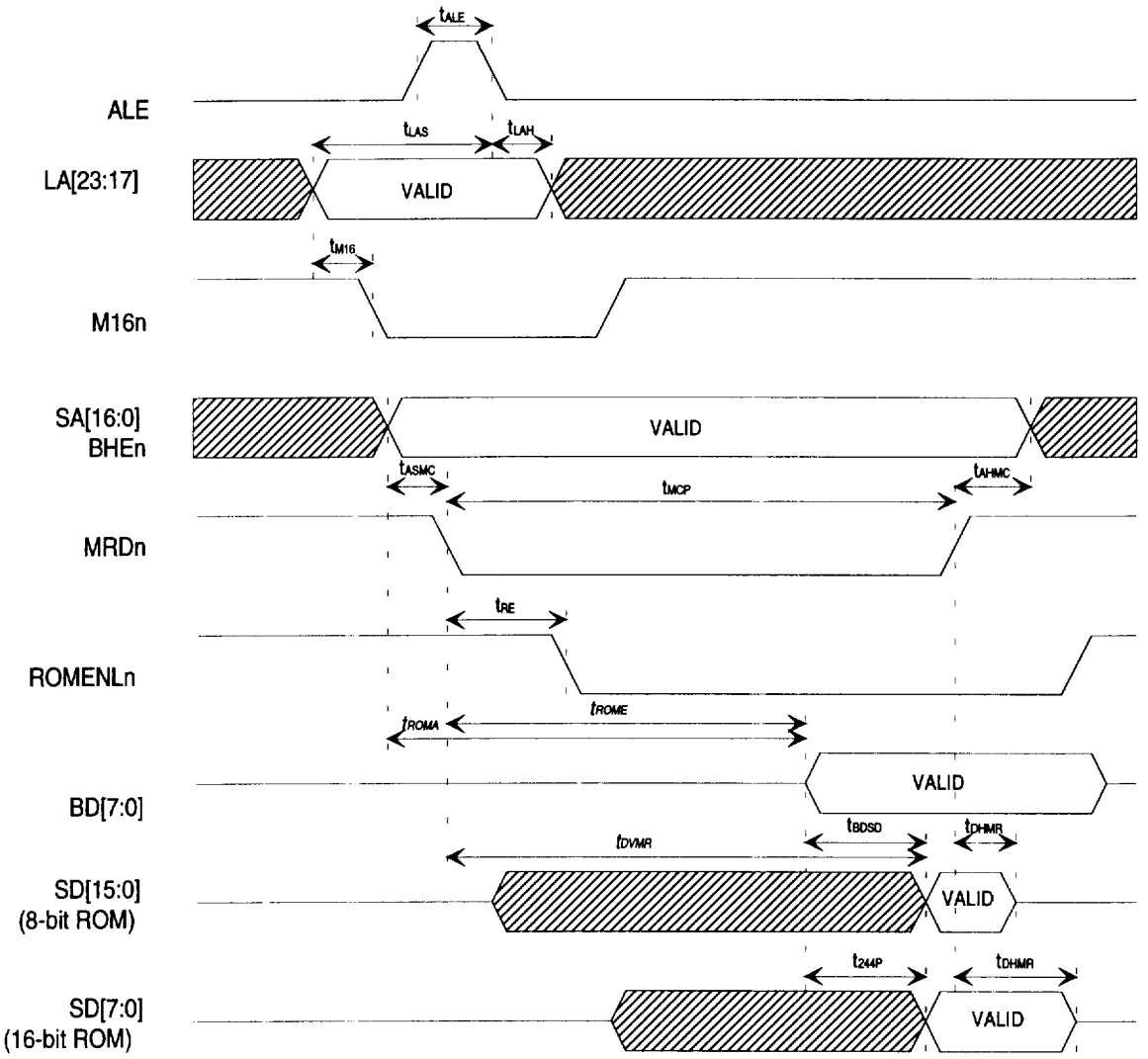


Figure 9.2 - ISA ROM Read Timing

ISA General I/O Access Timing

No	Symbol	Parameter	Min (ns)	Max (ns)	Load (pF)	Notes
ISA17	tASIO	SA[15:0] & BHEn Setup to I/O Command Active	25			
ISA18	tAHIO	SA[15:0] & BHEn Hold from I/O Command Inactive	25			
ISA19	tIOCP	I/O Command Pulse Width	115			
ISA20	tIO16	IO16n Active from Valid SA[15:0]		60	200	
ISA21	tDVIR	Read Data Valid from IORn Active		70	200	
ISA22	tDVRDY	Read Data Valid from IOCHRDY Active		50	200	
ISA23	tDHIR	Read Data Hold from IORn Inactive	0		200	
ISA24	tDIVW	Write Data Valid from IOWn Active	-55			
ISA25	tDHIW	Write Data Hold from IOWn Inactive	15			
ISA26	tIORDY	IOCHRDY Inactive from I/O Command Active		30	200	1

Notes:

1. IOCHRDY is normally not needed for I/O cycles. It is needed for special reset sequence and power saving modes only.

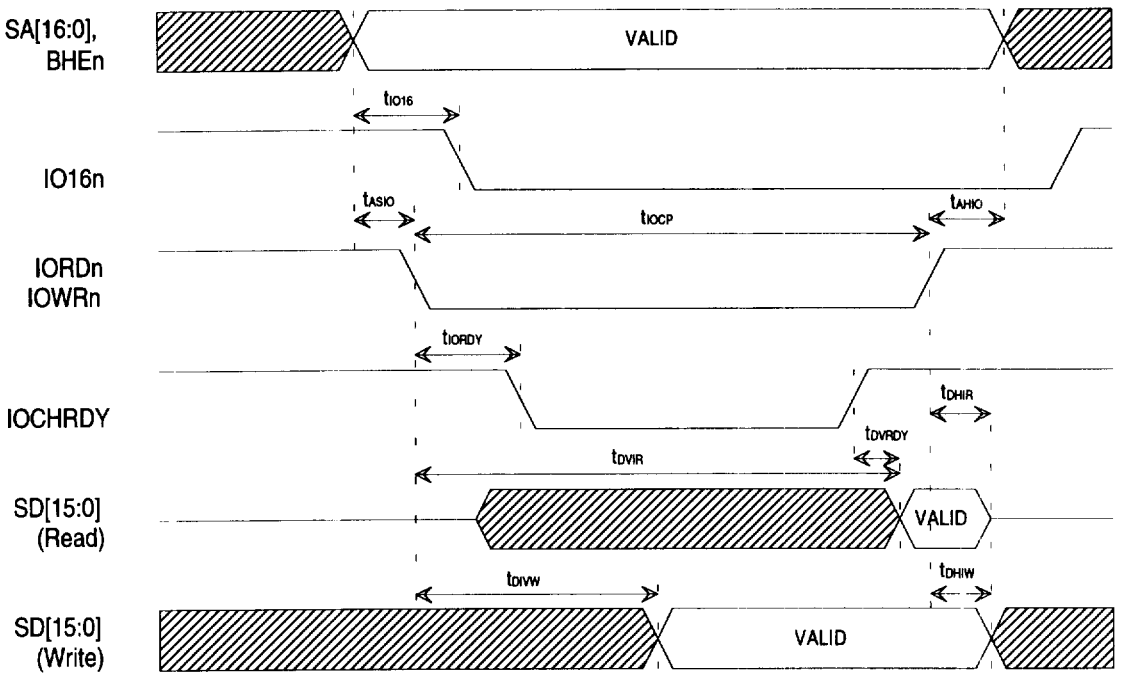


Figure 9.3 - ISA General I/O Access Timing

ISA DAC and Auxiliary I/O Timing

No	Symbol	Parameter	Min (ns)	Max (ns)	Load (pF)	Notes
ISA17	tASIO	SA[15:0] & BHEn Setup to I/O Command Active	25			
ISA18	tAHIO	SA[15:0] & BHEn Hold from I/O Command Active	25			
ISA19	tIOCP	I/O Command Pulse Width	115			
ISA27	tICDC	DAC Command Delay from I/O Command		25	50	
	tRLQV	*DAC Data Valid from DACRDn*		*395*	*50*	1
	tDVIR8	*SD[15:0] Valid from IORDn for DAC or Auxiliary Cycle*		*460*	*200*	2
ISA23	tDHIR	Read Data Hold from IORn Inactive	0		200	
ISA24	tDVIW	Write Data Valid from IOWn Active	-55			
ISA25	tDHIW	Write Data Hold from IOWn Inactive	15			
ISA28	tDWP	DACWRn Pulse Width	70			
ISA29	tSDBD	SD[7:0] Valid to BD[7:0] Valid		40	50	
ISA30	tBDSD	BD[7:0] Valid to SD[15:0] Valid		40	200	
ISA31	tACSn	Auxiliary Chip Select Delay from SA[15:0]		20	50	

Notes:
1. This is for reference only. This specification belongs to the DAC I/O access time.
2. This is for reference only. This is the specification for 8-bit I/O ISA bus. The real data valid time for the DAC should be calculated as follows: tDVIR=tICDC+tRLQV+tBDSD.

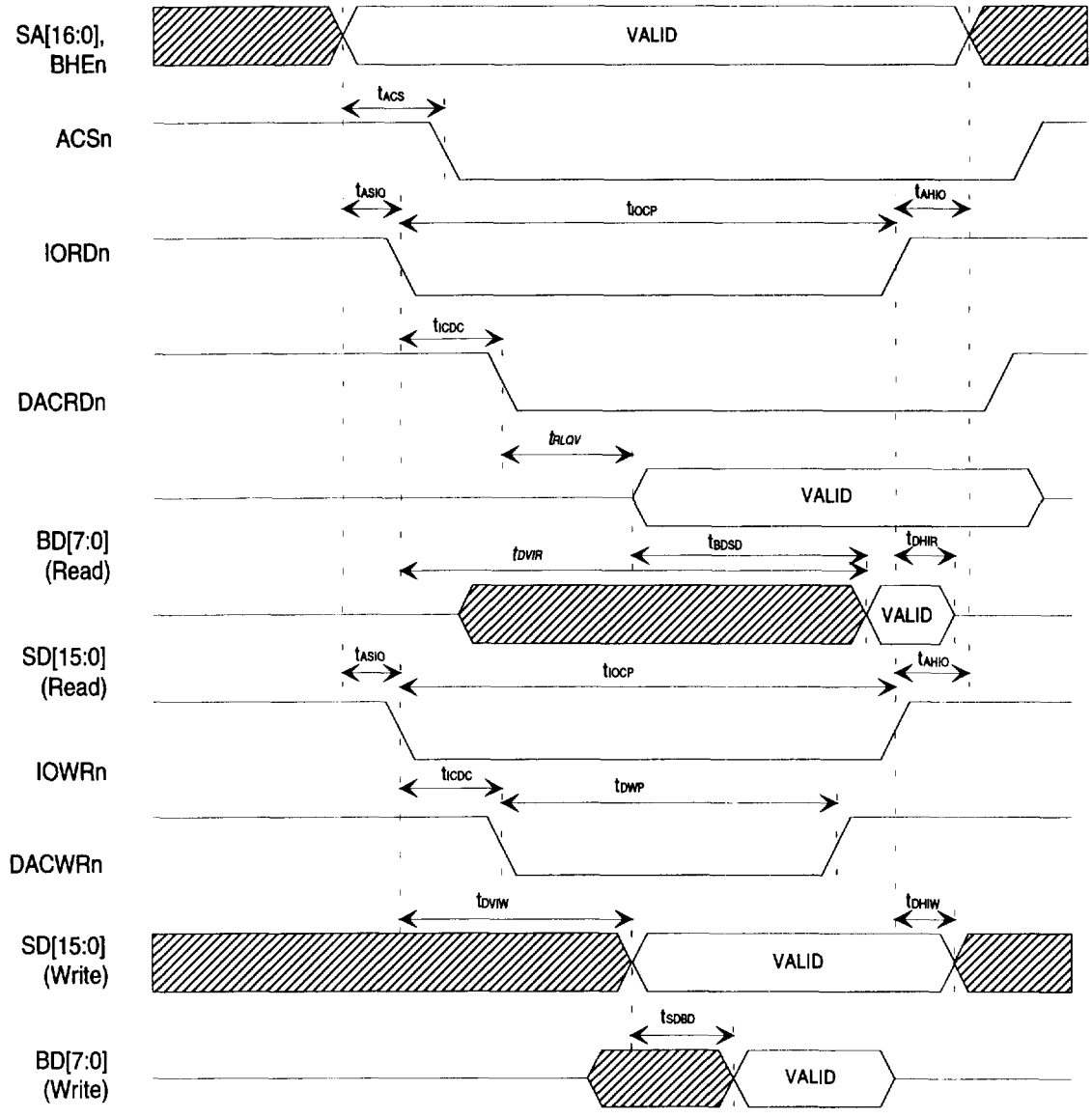


Figure 9.4- ISA DAC & Auxiliary I/O Timing

9.3.2 VL Bus Timing

VL Bus Interface Timing

No	Symbol	Parameter	Min (ns)	Max (ns)	Load (pF)	Notes
VL1	tPRCKP	Processor Clock Period	20			
VL2	tPRCKW	Processor Clock Pulse Width	8			
VL3	tPRCKR	Processor Clock Rise/Fall		2		
VL4	tSADS	ADS Setup Time	4			
VL5	tHADS	ADS Hold Time	2			
VL6	tSSA	Address Setup Time	4			
VL7	tHSA	Address Hold Time	2			
VL8	tSS	Status Setup Time	4			
VL9	tHS	Status Hold Time	2			
VL10	tLBSEL	LBSELn Valid from SA[31:2] & Status		20	25	
VL11	tSRDY	SRDYn Delay Time		13	75	
VL12	tSSRDYI	SRDYI Setup Time	5			
VL13	tHSRDYI	SRDYI Hold Time	2			
VL14	tVRD	Read Data Delay Time	3	14	125	
VL15	tHRD	Read Data Hold Time		2	125	
VL16	tSWD	Write Data Setup Time	4			
VL17	tHWD	Write Data Hold Time	2			

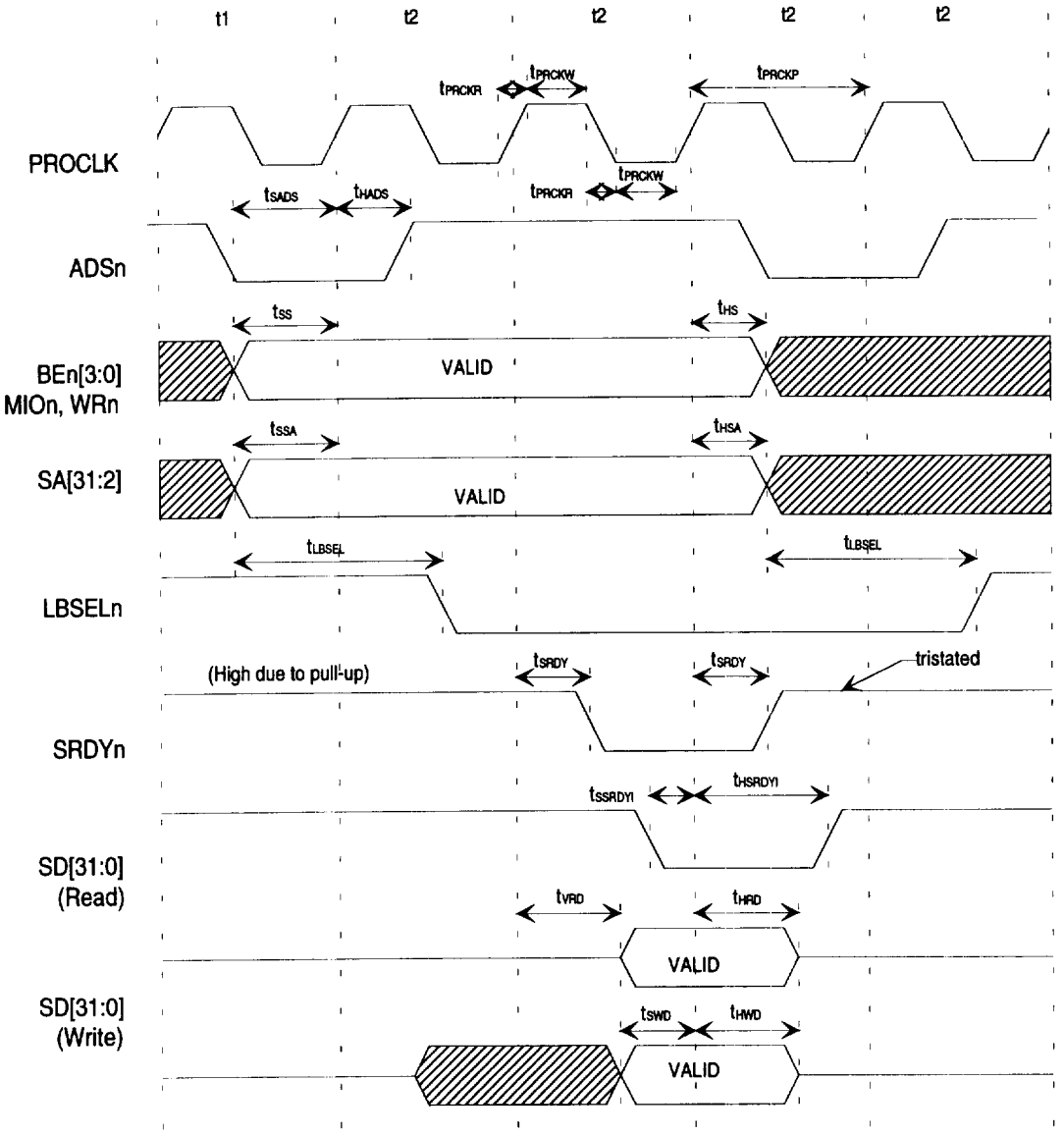


Figure 9.5 - VL Bus Interface Timing

VL ROM Read Timing

No	Symbol	Parameter	Min (ns)	Max (ns)	Load (pF)	Notes
VL4	tSADS	ADS Setup Time	4			
VL5	tHADS	ADS Hold Time	2			
VL6	tSSA	Address Setup Time	4			
VL7	tHSA	Address Hold Time	2			
VL8	tSS	Status Setup Time	4			
VL9	tHS	Status Hold Time	2			
VL18	tDOE	DOEn Delay from ISACMD		25	50	
ISA5	tASMC	SA[14:0] Setup to MRDn Active	23			
ISA6	tAHMC	SA[14:0] Hold from MRDn Inactive	20			
	tDVMR	*Read Data Valid from MRDn Active*		*460*	*200*	1,3
	tADSIC	*ISA Command (MRDn) Active Delay from ADSn*		*?*		1,2
	tROMA	*ROM Data Valid from SA[14:0]*		*448*	*50*	1
	tROME	*ROM Data Valid from MRDn Active*		*425*	*50*	1
	tROMO	*ROM Data Float from MRDn Inactive*	*0*		*50*	1
	t10P	*ISACMD Active from MRDn through LS10*		*35*	*50*	1
	t245P	*ROM Data Valid to SD[7:0] Valid through 245 Buffer*		*35*	*200*	1
	t245E	*DOEn Valid to SD[7:0] Valid through 245 Buffer*		*35*	*200*	1
	t245O	*SD[7:0] Tristated from DOEn Inactive through 245 Buffer*		*35*	*200*	1

Notes:

1. These parameters are for reference only.
2. This parameter is chipset dependent. A reasonable calculation for tADSMC should be as follows: tADSMC=(2*tPRCKP)+(2*tBCLK).
3. This is the required specification for 8-bit Memory on ISA bus. The actual timing can be calculated in two different ways. The worst of the 2 numbers should be used.
   1. tDVMR=tROME+t245P, or
   2. tDVMR=tROMA+t245P-tASMC.

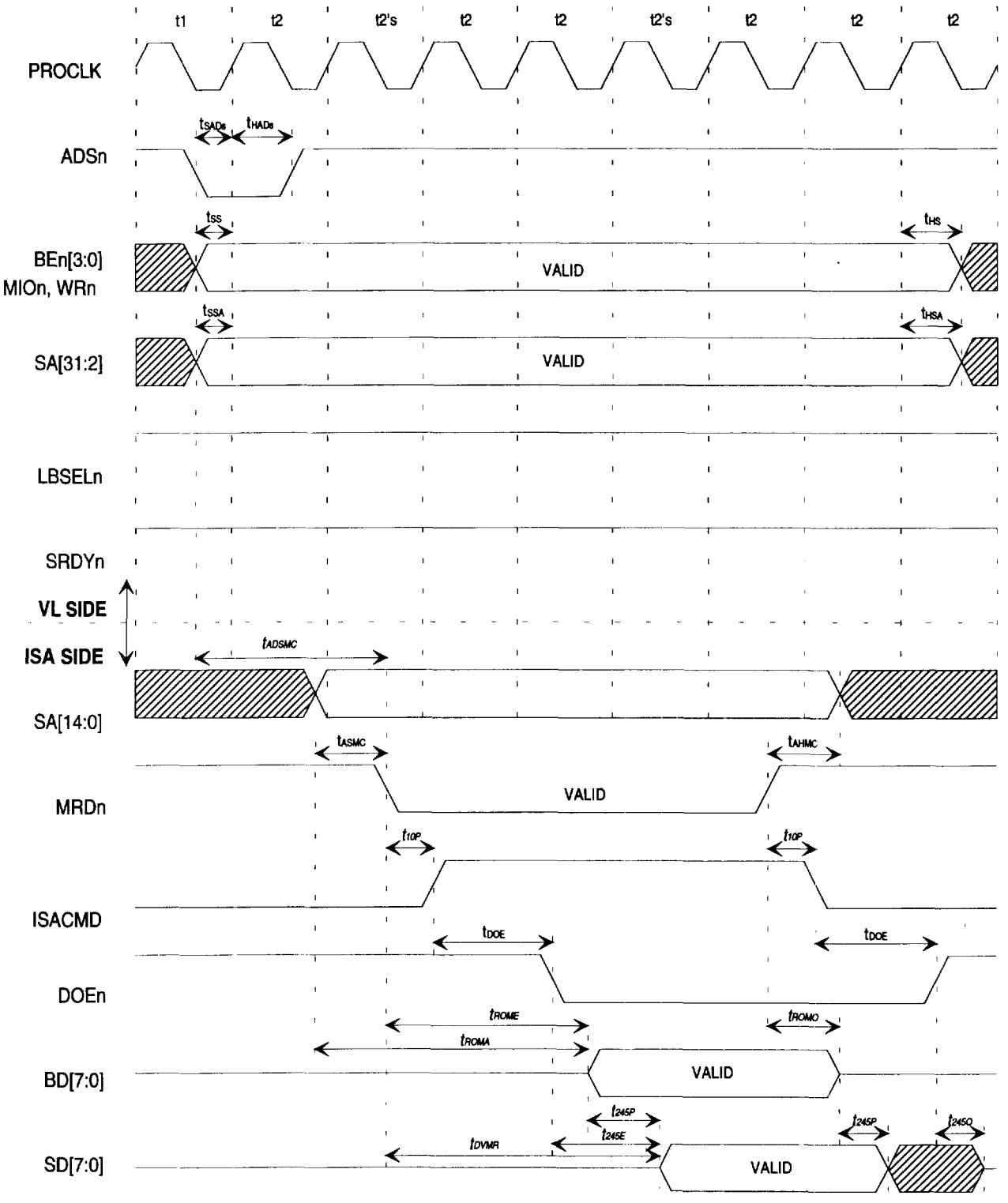


Figure 9.6 - VL ROM Read Timing

VL DAC I/O Read Timing

No	Symbol	Parameter	Min (ns)	Max (ns)	Load (pF)	Notes
VL4	tSADS	ADS Setup Time	4			
VL5	tHADS	ADS Hold Time	2			
VL6	tSSA	Address Setup Time	4			
VL7	tHSA	Address Hold Time	2			
VL8	tSS	Status Setup Time	4			
VL9	tHS	Status Hold Time	2			
	t10P	ISACMD Active from IORn through LS10		35	50	1
VL18	tDOE	DOEn Delay from ISACMD		25	50	
VL19	tICDC	DAC Command Delay from ISACMD		25	50	4
	tADSIC	*ISA Command (IORn) Active Delay from ADSn*		*?*		1,2
	tRLQV	*DAC Data Valid from DACRDn*		*395*	*50*	1
	tDVIR8	*SD[15:0] Valid from IORDn for DAC Cycle*		*460*	*200*	1,3
	t245P	*DAC Data Valid to SD[7:0] Valid through 245 Buffer*		*40*	*200*	1

Notes:

1. These parameters are for reference only.
2. This parameter is chipset dependent. A reasonable calculation for tADSMC should be as follows: tADSMC=(2*tPRCKP)+(2*tBCLK).
3. This is the required specification for 8-bit Memory on ISA bus. The actual timing can be calculated as follows: tDVIR8=t10P+tICDC+tRLQV+t245P.
4. Although this parameter is similar to the ISA27 parameter, it is essential to test this under VL configuration because the address decoding is from the VL bus.

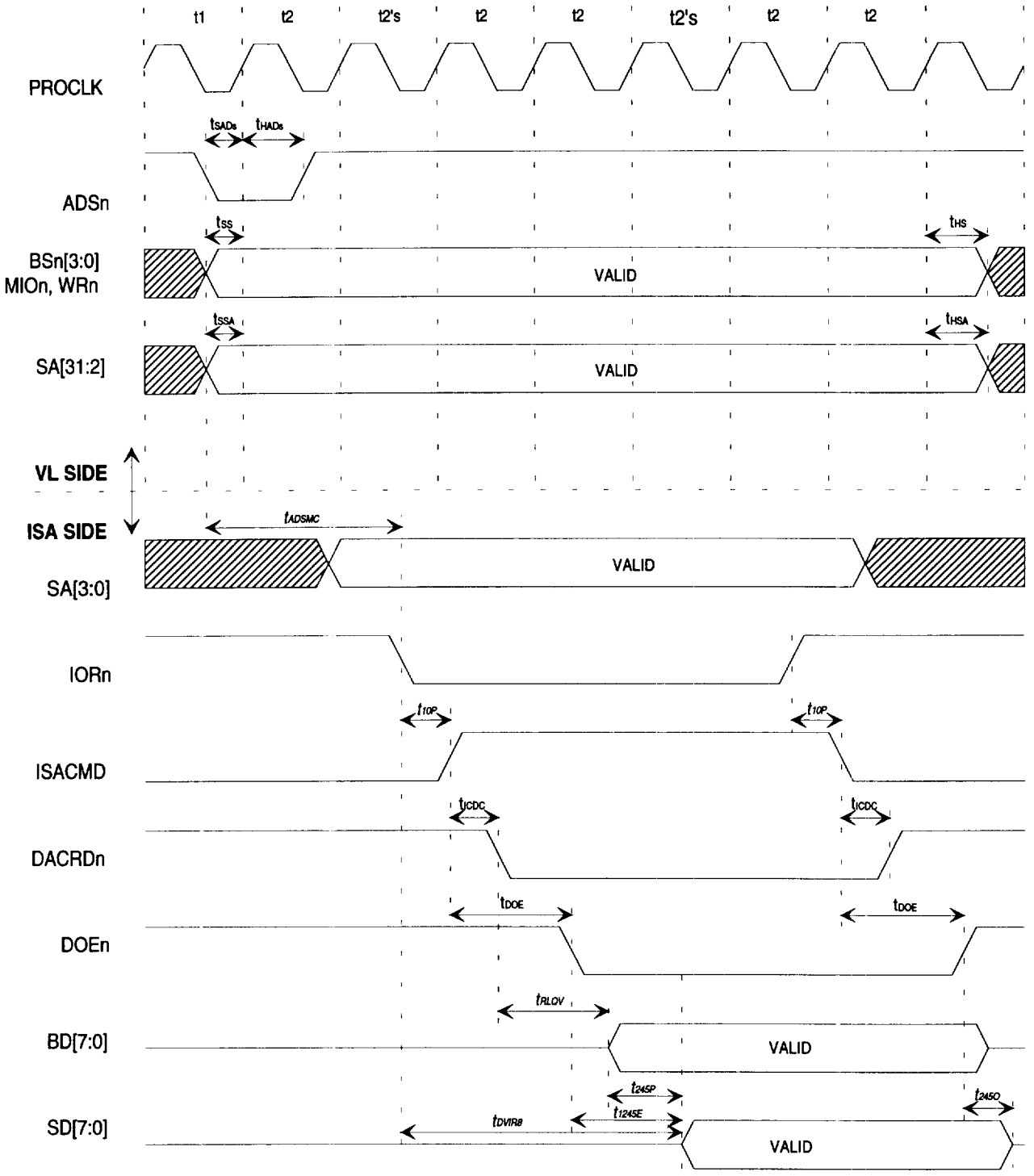


Figure 9.7 - VL DAC I/O Read Timing

VL DAC I/O Write Timing

No	Symbol	Parameter	Min (ns)	Max (ns)	Load (pF)	Notes
VL4	tSADS	ADS Setup Time	4			
VL5	tHADS	ADS Hold Time	2			
VL6	tSSA	Address Setup Time	4			
VL7	tHSA	Address Hold Time	2			
VL8	tSS	Status Setup Time	4			
VL9	tHS	Status Hold Time	2			
	t10P	*ISACMD Active from IOWn through LS10*		*35*	*50*	1
VL18	tDOE	DOEn Delay from ISACMD		25	50	
VL19	tICDC	DAC Command Delay from ISACMD		25	50	2
ISA24	tDVIW	Write Data Valid from IOWn Active	-55			
ISA28	tDWP	DACWRn Pulse Width	70			
	t245D	*DACWRn Valid to BD[7:0] Valid through 245 Buffer (DIR)*		*35*	*50*	1
	t245E	*DOEn Valid to BD[7:0] Valid through 245 Buffer (OEn)*		*35*	*50*	1
	t245P	*SD[7:0] Valid to BD[7:0] Valid through 245 Buffer (A-B)*		*35*	*50*	1

Notes:

1. These parameters are for reference only.
2. Although this parameter is similar to the ISA27 parameter, it is essential to test this under VL configuration because the address decoding is from the VL bus.

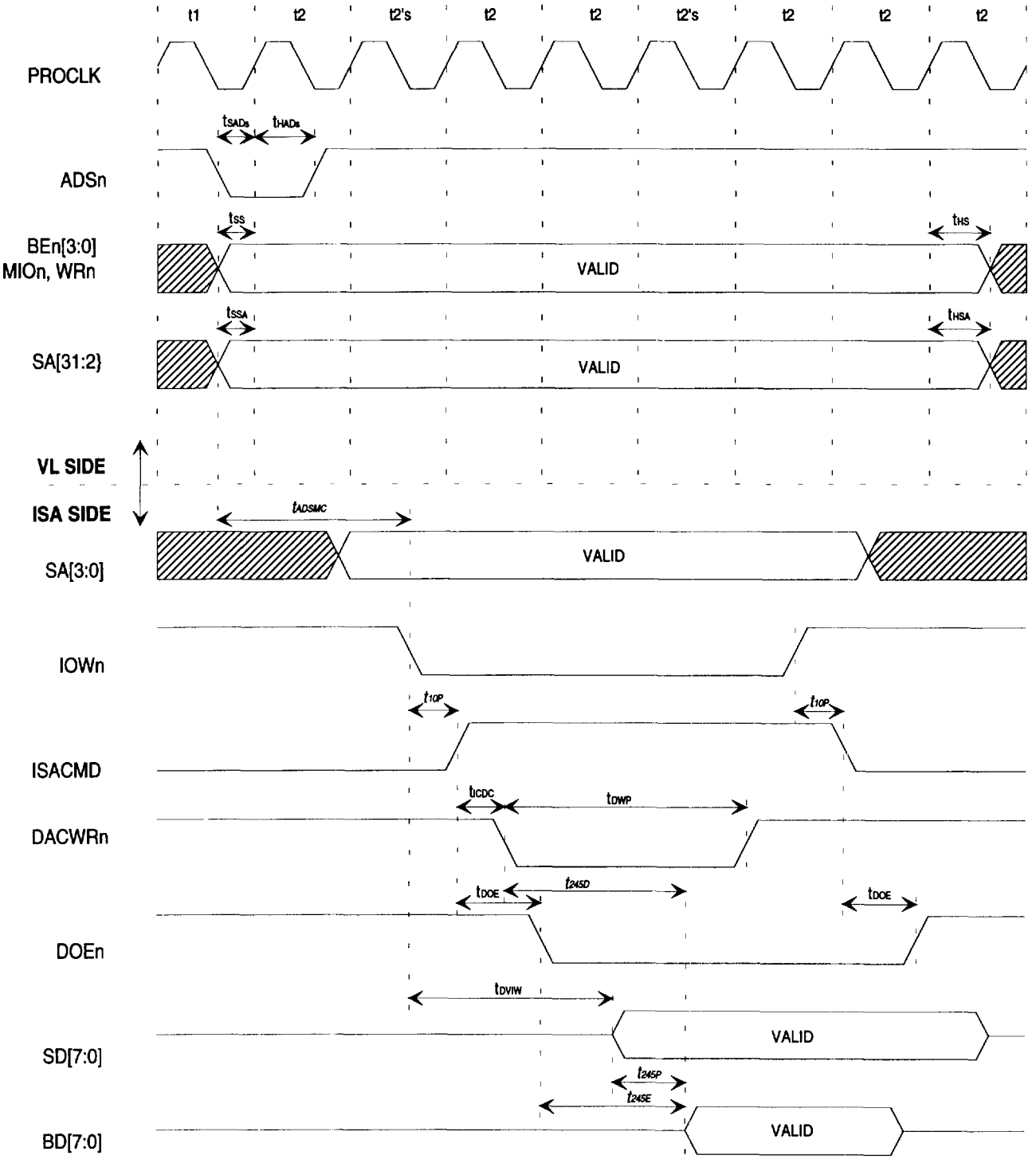


Figure 9.8 - VL DAC I/O Write Timing

9.3.3 PCI Bus Timing

PCI Bus Clock Requirement

No	Symbol	Parameter	Min (ns)	Max (ns)	Load (pF)	Notes
PCI1	tPCKP	PCI Bus Clock Period	30			
PCI2	tPCKL	PCI Bus Clock Low Time	12			
PCI3	tPCKH	PCI Bus Clock High Time	12			

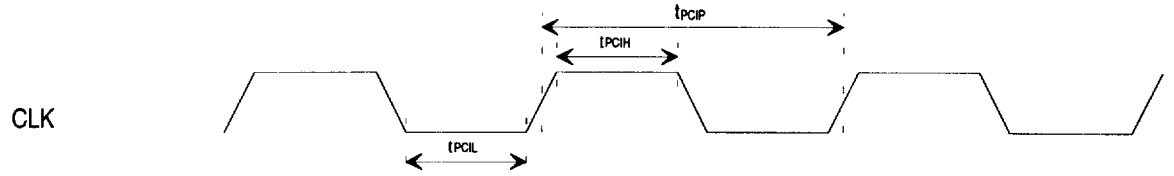


Figure 9.9 - PCI Bus Clock Requirement

PCI Bus Timing (Read Operation)

No	Symbol	Parameter	Min (ns)	Max (ns)	Load (pF)	Notes
PCI4	tSPCI	Input Setup Time to CLK	7			
PCI5	tHPCI	Input Hold Time to CLK	0			
PCI6	tPPCI	Ouput Propagation Delay from CLK	2	11	0/50	1

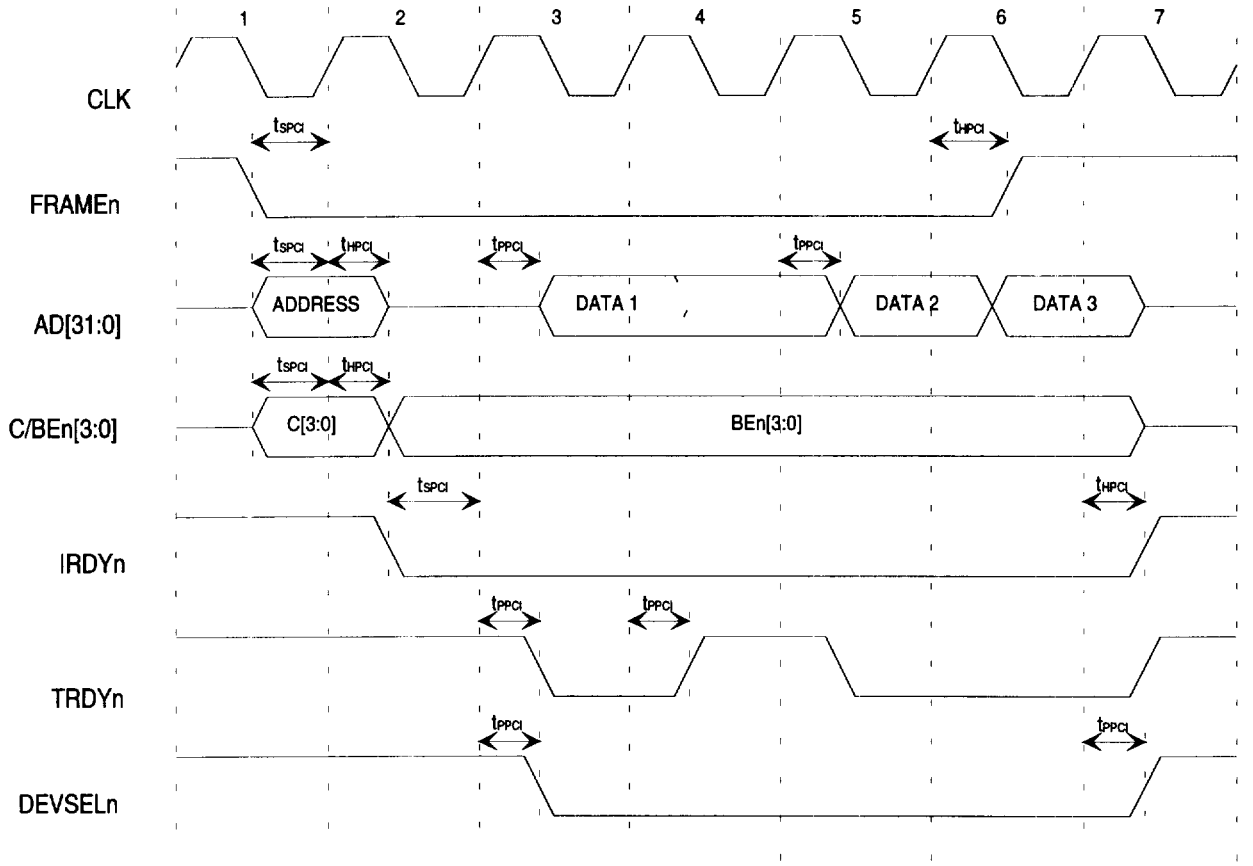


Figure 9.10 - PCI Bus Timing (Read Operation)

Notes:

1. Minimum timing is when load=0pF, and maximum timing is when load=50pF.

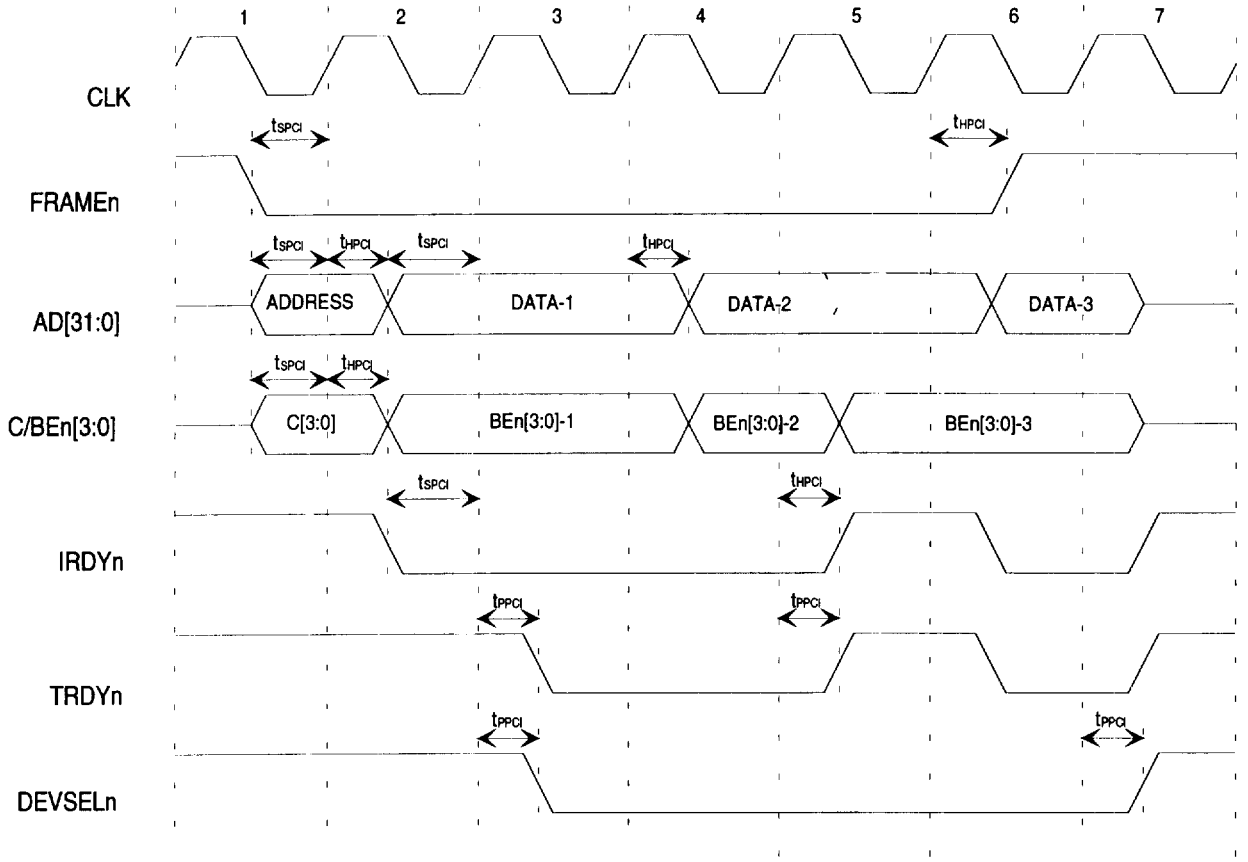


Figure 9.11 - PCI Bus Timing (Write Operation)

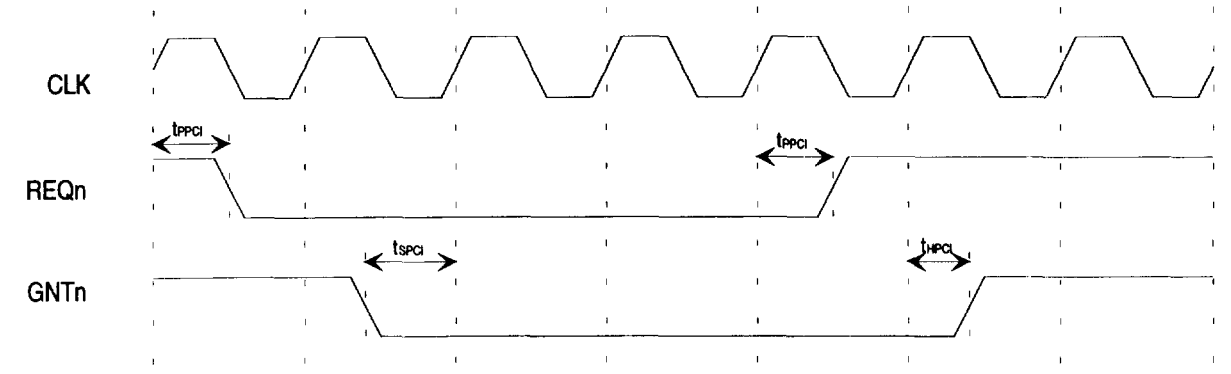


Figure 9.12 - PCI Bus Master Request Timing

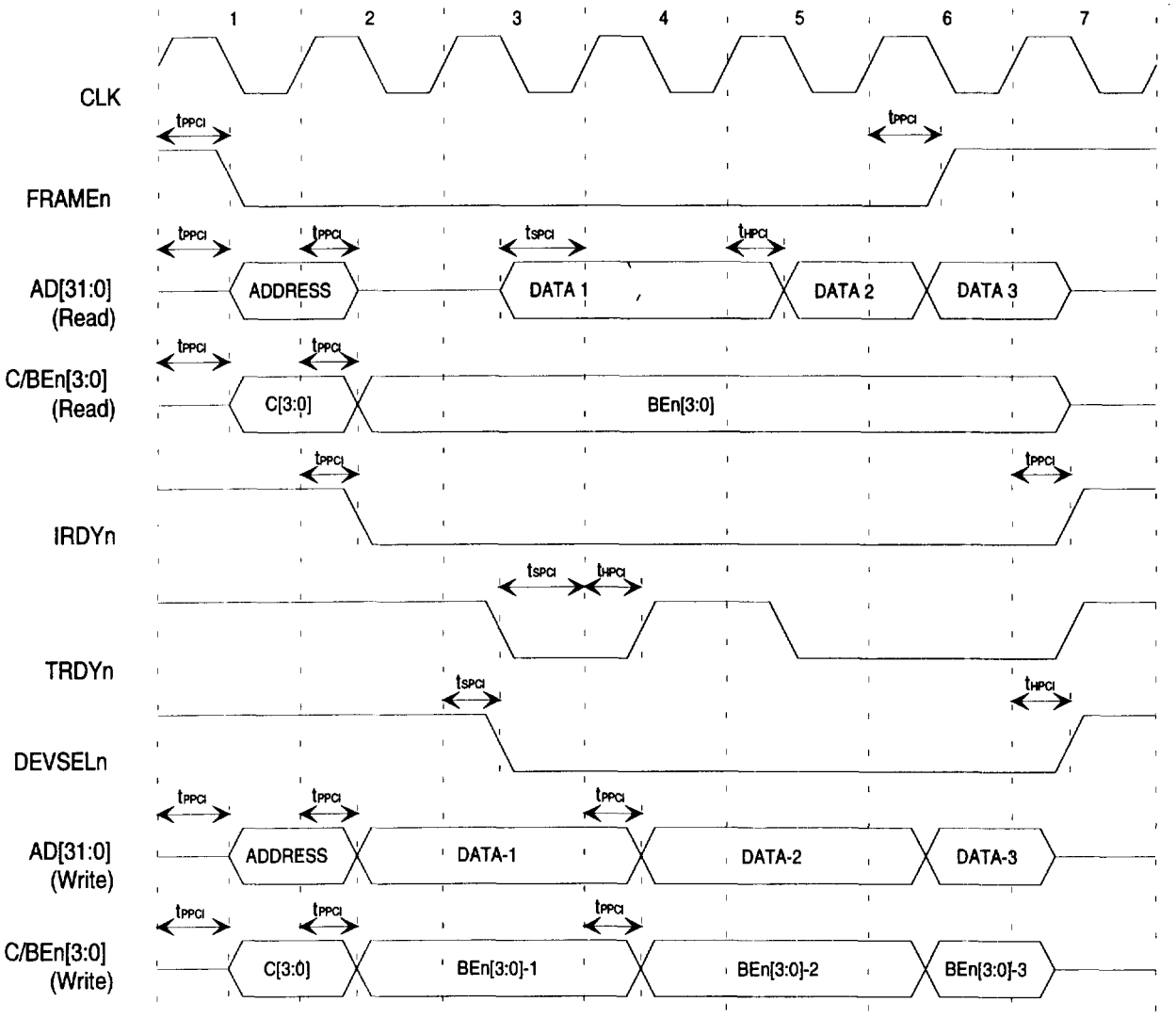


Figure 9.13 - PCI Bus Master Read/Write Timing

PCI ROM Read Timing

No	Symbol	Parameter	Min (ns)	Max (ns)	Load (pF)	Notes
PCI4	tSPCI	Input Setup Time to CLK	7			
PCI5	tHPCI	Input Hold Time to CLK	0			
PCI6	tPPCI	Ouput Propagation Delay from CLK	2	11	0/50	1
PCI7	tROMEN	ROMENLn Delay from CLK		25	50	
	tROMA	*ROM Data Valid from RA[14:0] (AD[30:16])*		*120*	*50*	2
	tROME	*ROM Data Valid from ROMENLn*		*60*	*50*	2
	tROMO	*ROM Data Float from ROMENLn*		*55*	*50*	2

Notes:

1. Minimum timing is when load=0pF, and maximum timing is when load=50pF.
   These parameters are for reference only. They can be used to choose the appropriate EPROM speed. These requirements are based on the bus clock being 33MHz.

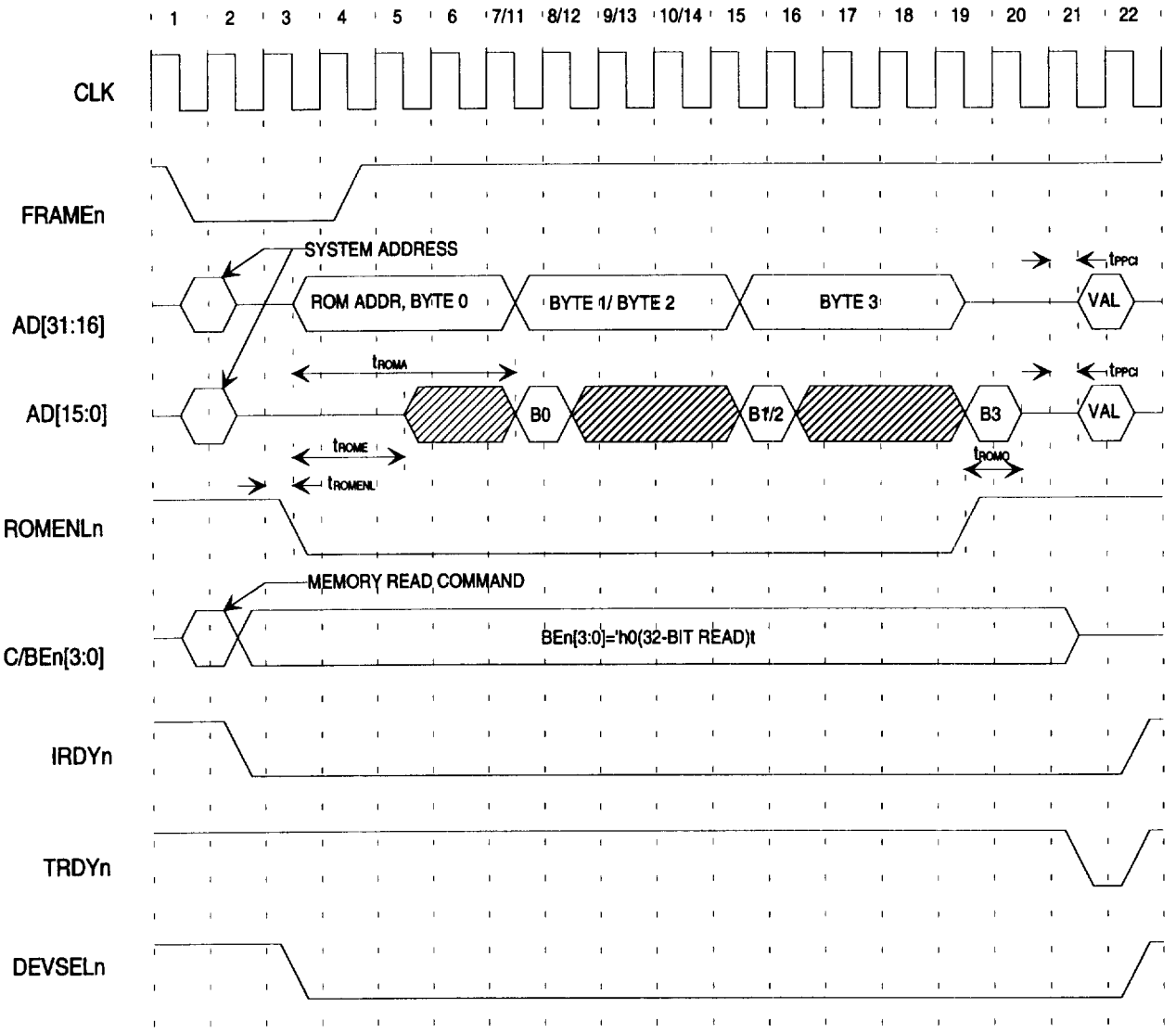


Figure 9.14 - PCI ROM Read Timing

PCI DAC & Auxiliary I/O Timing

No	Symbol	Parameter	Min (ns)	Max (ns)	Load (pF)	Notes
PCI4	tSPCI	Input Setup Time to CLK	7			
PCI5	tHPCI	Input Hold Time to CLK	0			
PCI6	tPPCI	Ouput Propagation Delay from CLK	2	11	0/50	1
PCI8	tARS	ARS[3:0] Delay from CLK		25	50	
PCI9	tADC	Auxiliary or DAC Command Delay from CLK		25	50	
PCI10	tBDAD	BD[7:0] Valid to AD[31:0] Valid		40	50	
PCI11	tADBD	AD[31:0] Valid to BD[7:0] Valid		40	50	
PCI12	tHADC	BD[7:0] Valid Hold from DACWRn/AWRn Inactive	tPCIP		50	
	tRLQV	*BD[7:0] Valid from ARDn or DACRDn*		*65*	*50*	2

Notes:

1. Minimum timing is when load=0pF, and maximum timing is when load=50pF.
2. This parameter is for reference only. They can be used to choose the appropriate DAC or Auxiliary I/O speed. These requirements are based on the bus clock being 33MHz.

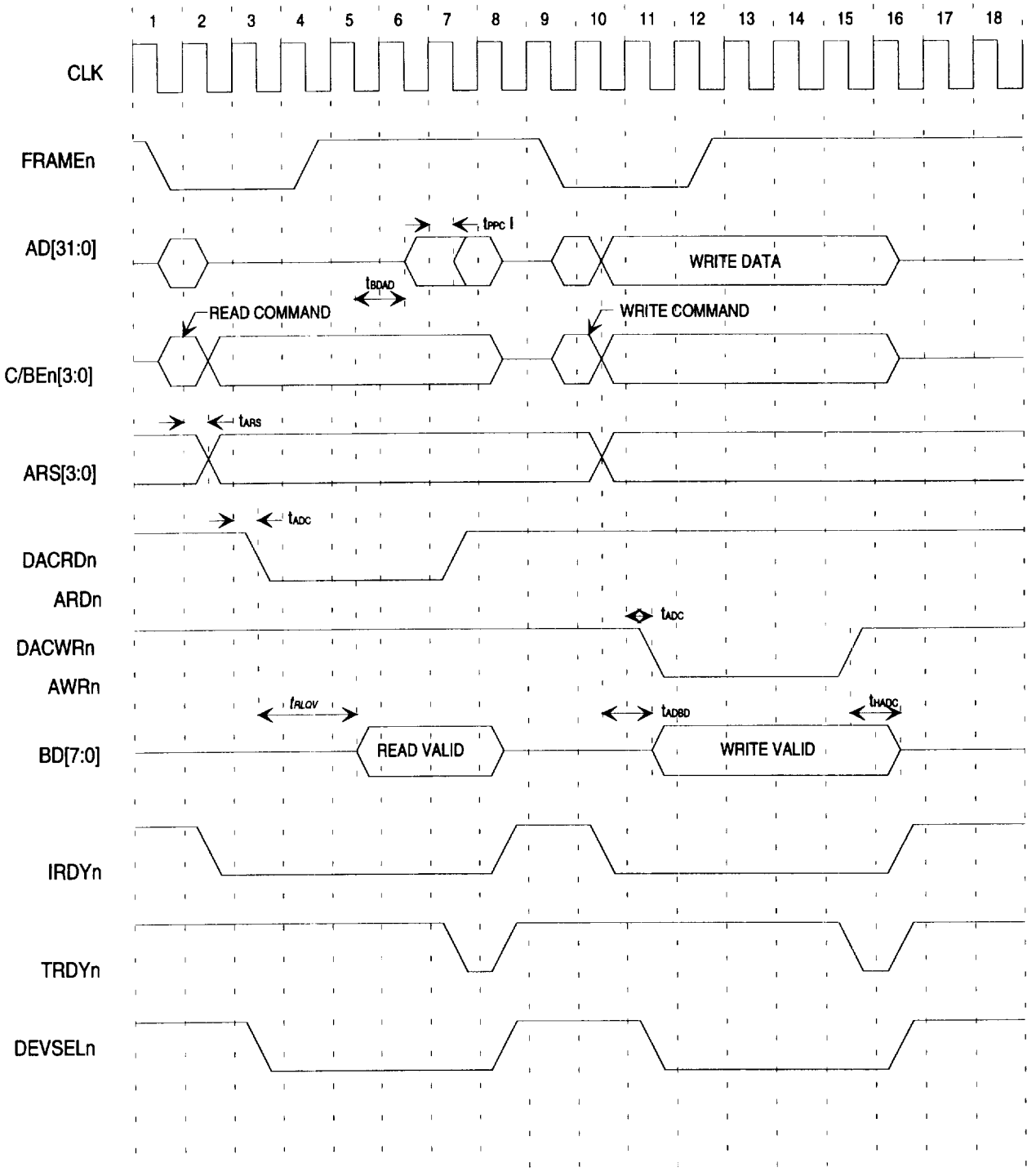


Figure 9.15 - PCI DAC & Auxiliary I/O Timing

9.3.4 - DAC Interface Timing

DAC Pixel Port Interface Timing

No	Symbol	Parameter	Min (ns)	Max (ns)	Load (pF)	Notes
DAC1	tVCKP	Video Clock Period	9			
DAC2	tVCKL	Video Clock Low Time	3			
DAC3	tVCKH	Video Clock High Time	3			
DAC4	tCHCH	Pixel Clock Period	9		50	1
DAC5	tCLCH	Pixel Clock Low Time	3		50	
DAC6	tCHCL	Pixel Clock High Time	3		50	
DAC7	tPVCH	P[23:0] Setup to PCLK	2		50	1
DAC8	tCHPX	P[23:0] Hold to PCLK	2		50	
DAC9	tBVCH	BLANKn Setup to PCLK	2		50	1
DAC10	tCHBX	BLANKn Hold to PCLK	2		50	

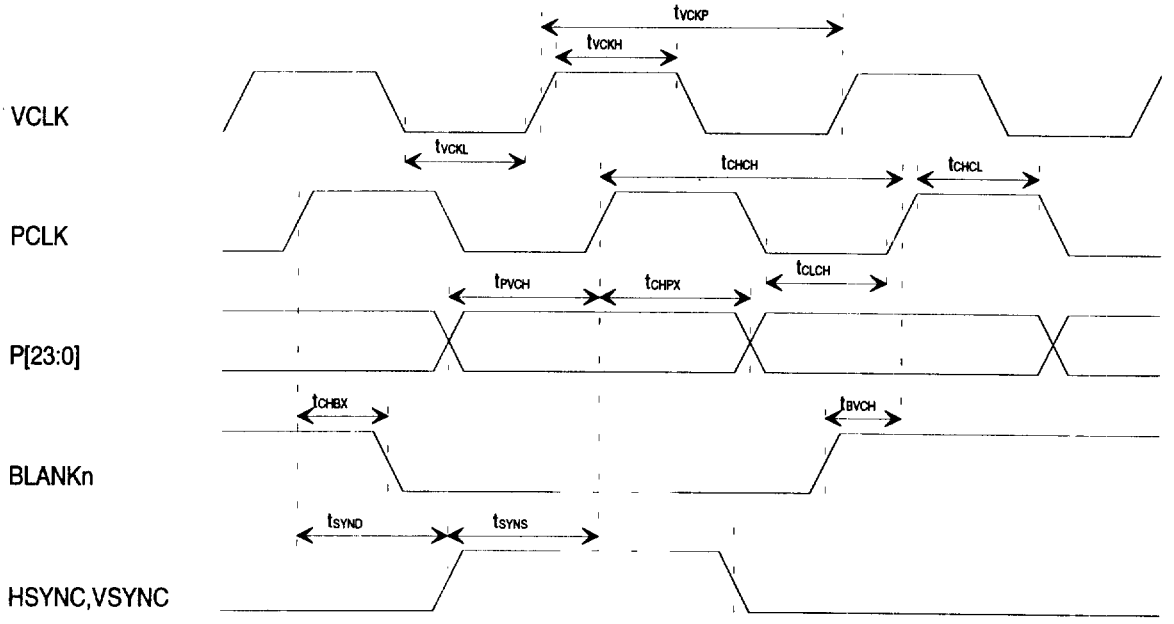


Figure 9.16 - DAC Pixel Port Interface Timing

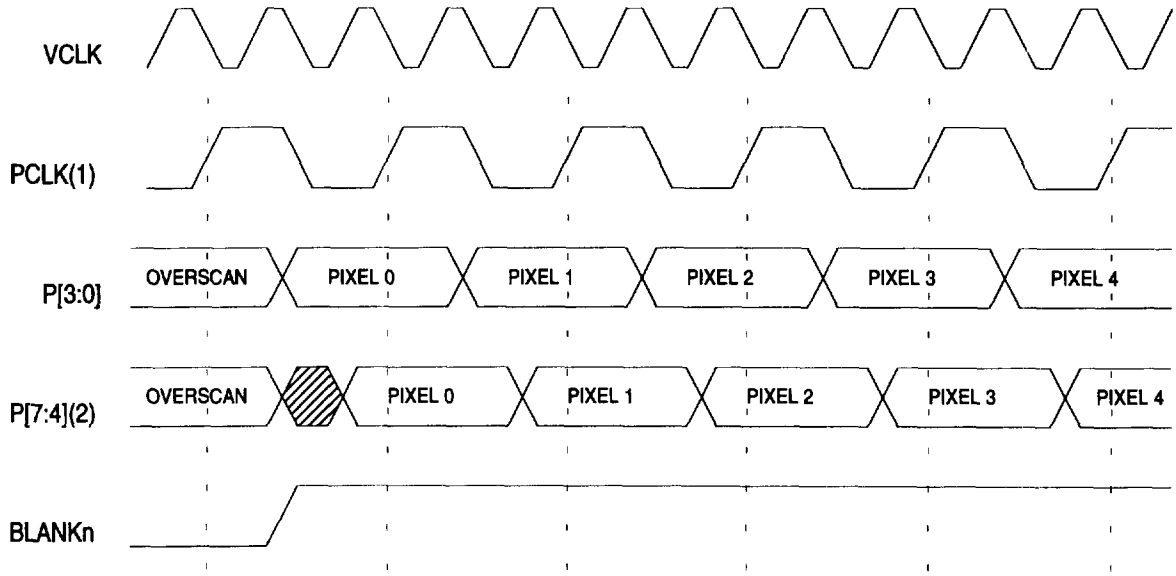


Figure 9.17 - DAC Interface - Attribute Mode 0, VGA Mode 13 (8bpp, 8-bit port)

Notes:

1. PCLK frequency is half that of VCLK frequency.
2. Nibble P[7:4] is one VCLK delayed from nibble P[3:0] for the same pixel.

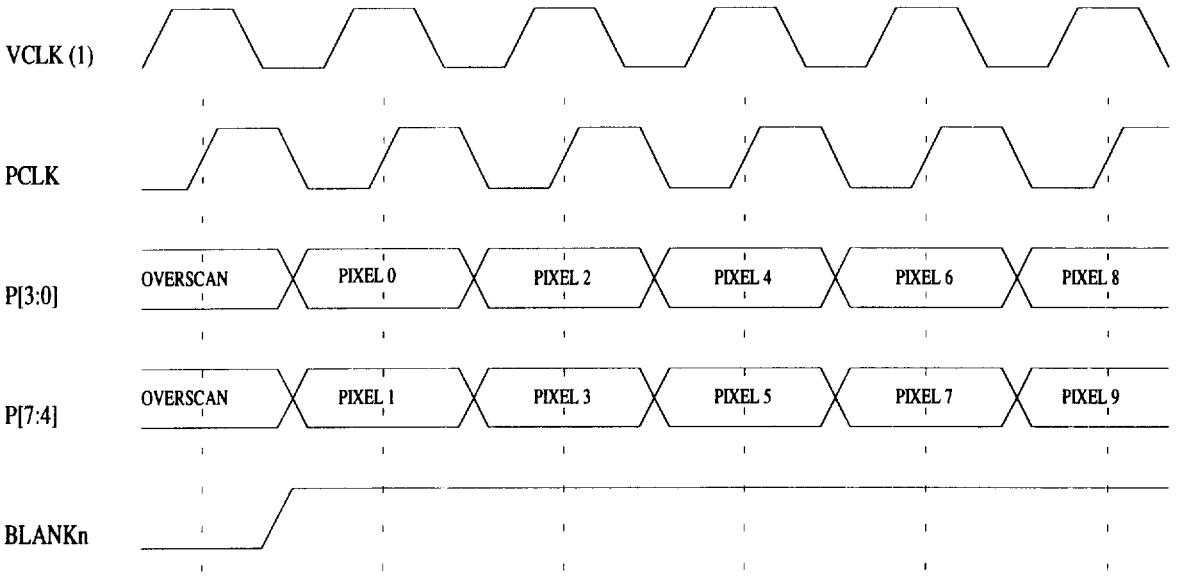


Figure 9.18 - DAC Interface - Attribute Mode 1 (4bpp, 8-bit port)

Notes:

1. The VCLK frequency is only half of the normally required frequency. For example, normal frequency for 1280x1024 70Hz is 135MHz, but it only needs to be 67.5MHz for this mode.

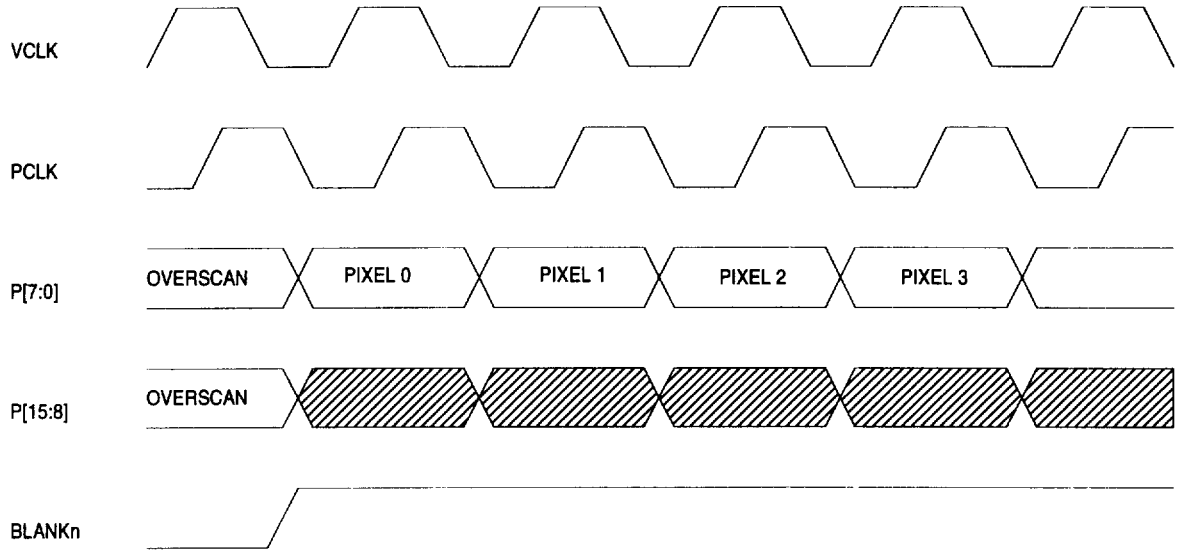


Figure 9.19 - DAC Interface - Attribute Mode 2A (8bpp, 8-bit port)

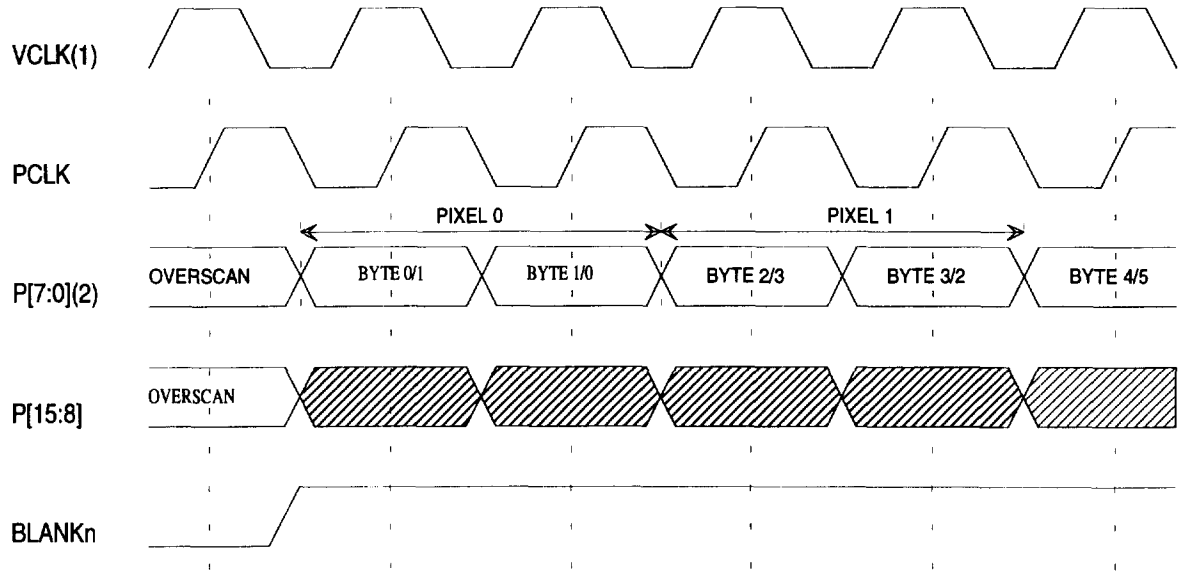


Figure 9.20 - DAC Interface - Attribute Mode 2B (15/16bpp, 8-bit port)

Notes:

1. VLCK frequency is twice that of normally required frequency. For example, the normal frequency for 640x480 60 Hz is 25MHz, but it has to be 50MHz for this mode.
2. The pixel data ordering can be byte 0, byte 1, byte 2, byte 3, ... or byte 1, byte 0, byte 3, byte 2, ..., depending on ER38b4.

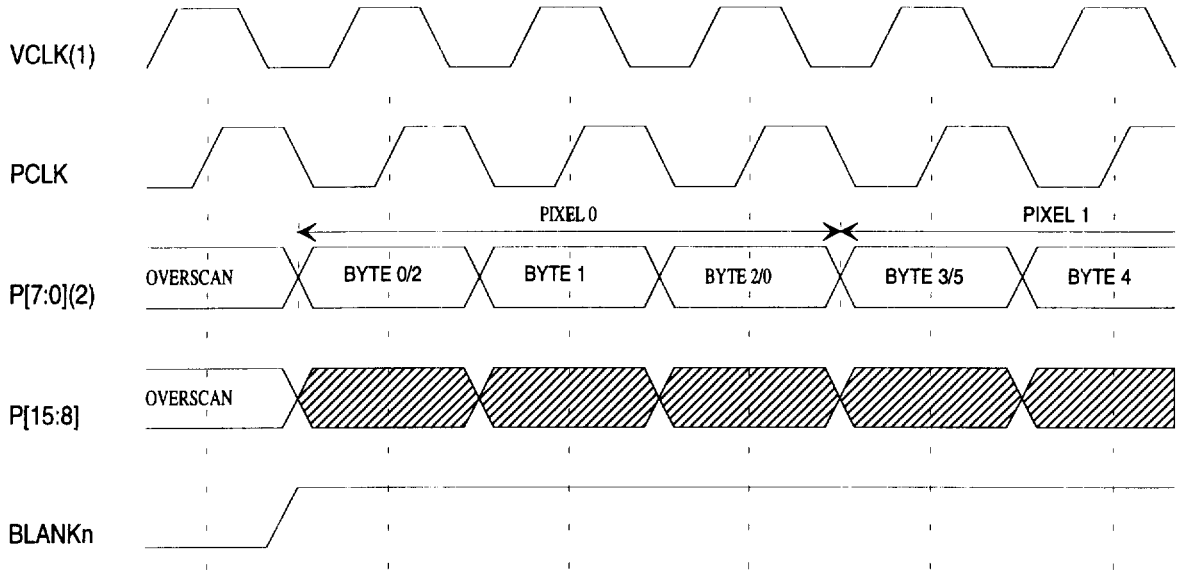


Figure 9.21 - DAC Interface - Attribute Mode 2C (24bpp, 8-bit port)

Notes:

1. VLCK frequency is three times that of normally required frequency. For example, the normal frequency for 640x480 60 Hz is 25MHz, but it has to be 75MHz for this mode.
2. The pixel data ordering can be byte 0, byte 1, byte 2, byte 3, byte 4, byte 5 ... or byte 2, byte 1, byte 0, byte 5, byte 4, byte 3, ..., depending on ER38b4.

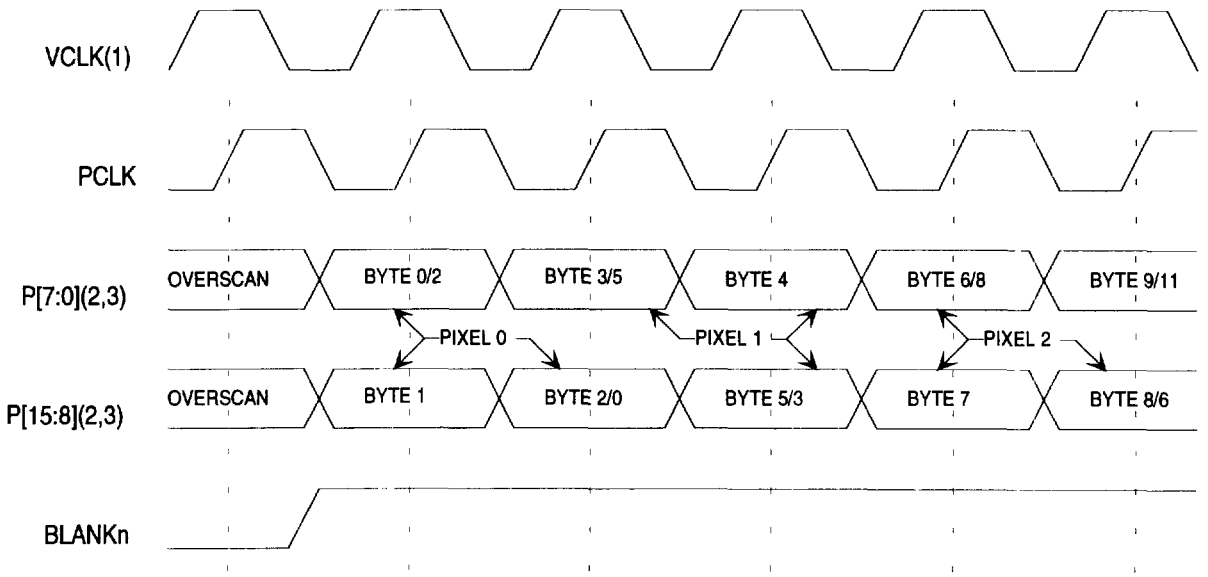


Figure 9.22 - DAC Interface - Attribute Mode 3 (24bpp, 16-bit port)

Notes:

1. VLCK frequency is 3/2 times that of normally required frequency. For example, the normal frequency for 640x480 60 Hz is 25MHz, but it has to be 37.5MHz for this mode.
2. The pixel data ordering can be byte 0, byte 1, byte 2, byte 3, byte 4, byte 5 ... or byte 2, byte 1, byte 0, byte 5, byte 4, byte 3, ..., depending on ER38b4.
3. The third byte of a pixel is always on the high byte of P bus (P[15:8]).

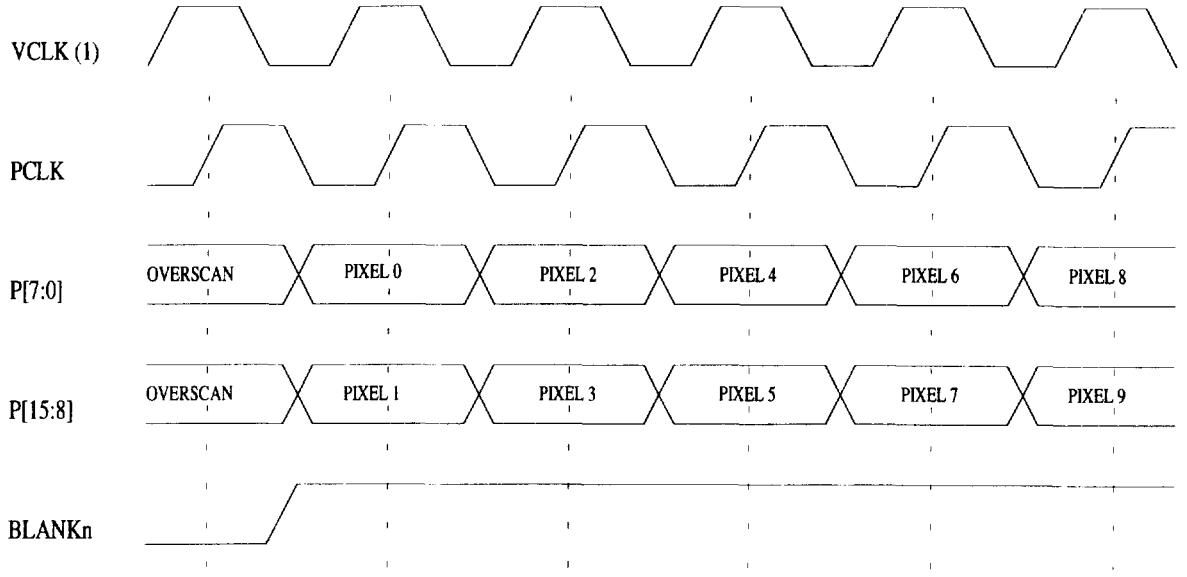


Figure 9.23 - DAC Interface - Attribute Mode 4 (8bpp, 16-bit port)

No es:

1. The VCLK frequency is only half of the normally required frequency. For example, normal frequency for 1280x1024 70Hz is 135MHz, but it only has to be 67.5MHz for this mode.

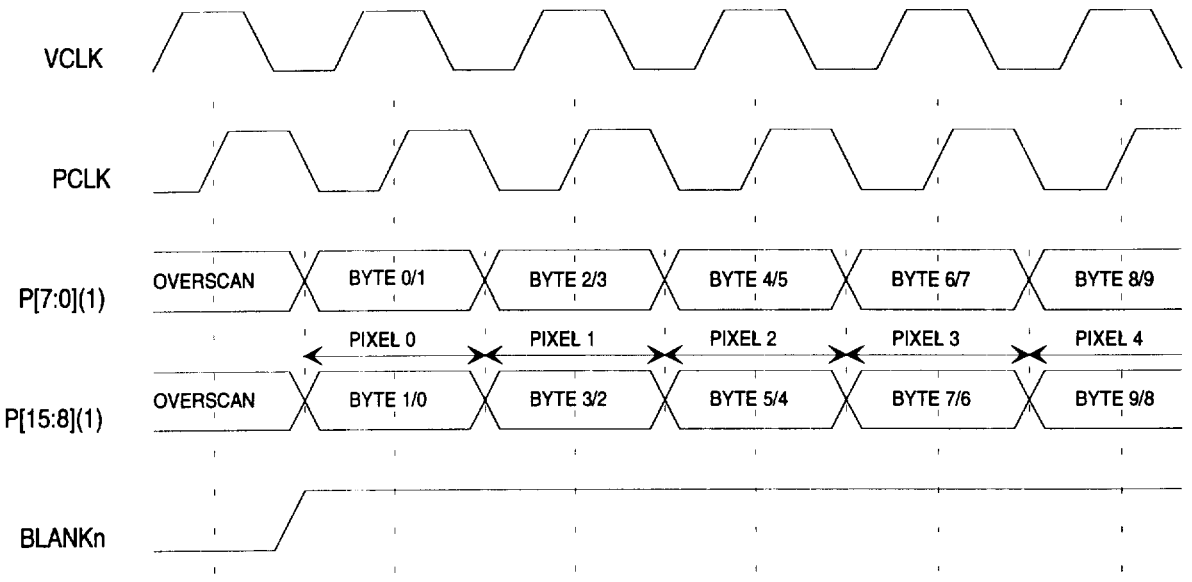


Figure 9.24 - DAC Interface - Attribute Mode 5 (15/16bpp, 16-bit port)

Notes:

1. The pixel data ordering can be byte 0, byte 1, byte 2, byte 3, ... or byte 1, byte 0, byte 3, byte 2, ..., depending on ER38b4.

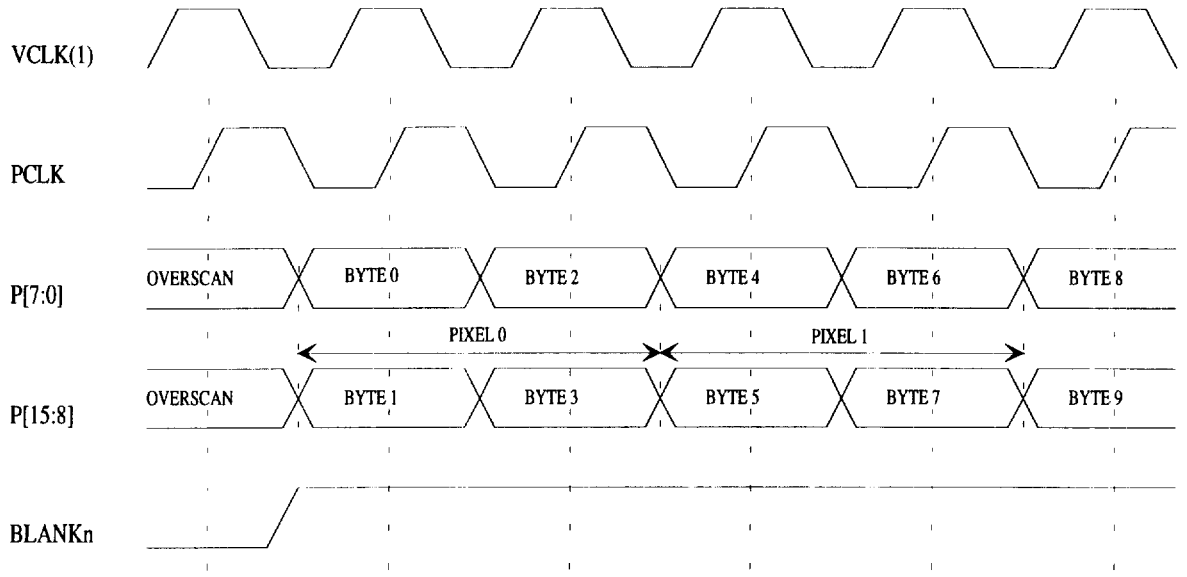


Figure 9.25 - DAC Interface - Attribute Mode 6 (32bpp, 16-bit port)

Notes:

1. VLCK frequency is twice that of normally required frequency. For example, the normal frequency for 640x480 60 Hz is 25MHz, but it has to be 50MHz for this mode.

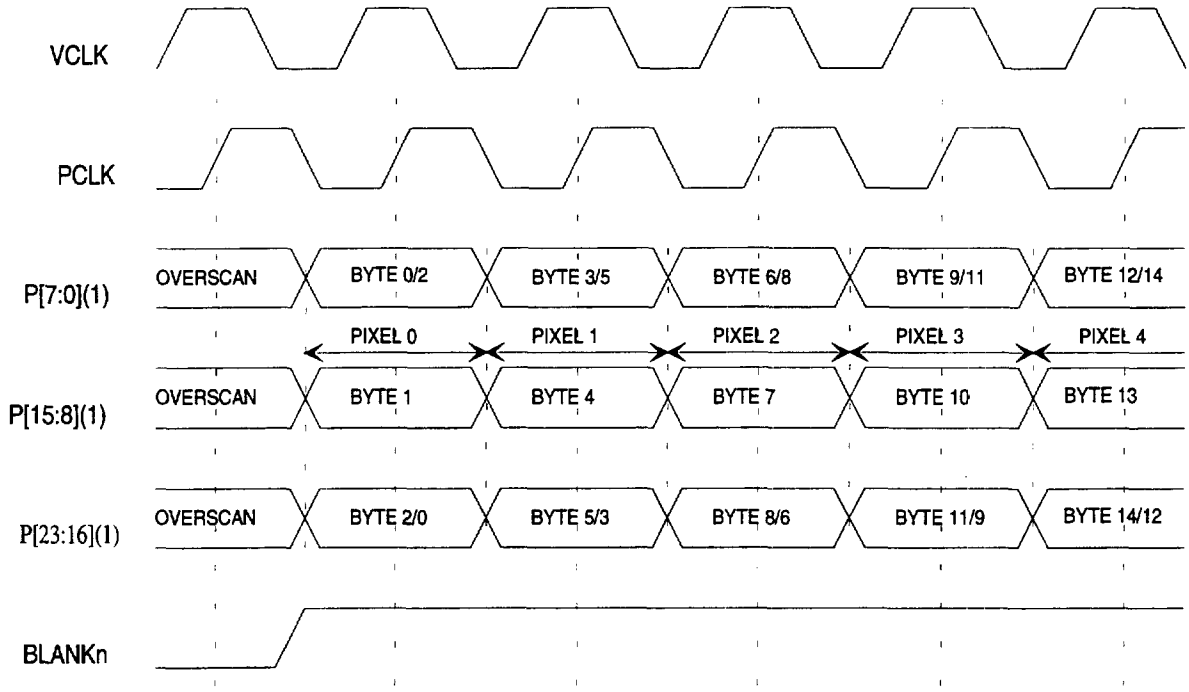


Figure 9.26 - DAC Interface - Attribute Mode 7 (24bpp, 24-bit port)

Notes:

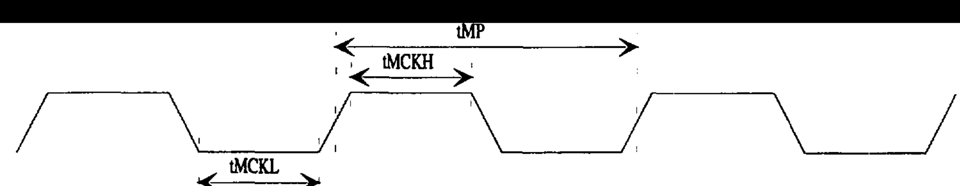
1. The pixel data ordering can be byte 0, byte 1, byte 2, byte 3, ... or byte 2, byte 1, byte 0, byte 5, ..., depending on ER38b4.

9.3.5 - Memory Interface Timimg

Memory Clock Requirement

No	Symbol	Parameter	Min (ns)	Max (ns)	Load (pF)	Notes
M1	tMP	Memory Clock Period	15	25		1

MCLK



Programmable Parameters

No	Symbol	Parameter	Min (tMP)	Max (tMP)	Register	Notes
M4	tRP	RASxn Precharge	1.5	5	ER26[3,1:0]	
M9	tCP	CASxn Precharge	0.5	2	ER27[1:0]	
M8	tCAS	CASxn Pulse Width	1	2.5	ER27[2:1]	
	tRCPD	RASxn Low to CASxn Precharge Delay	1	4	ER27[5:4]	

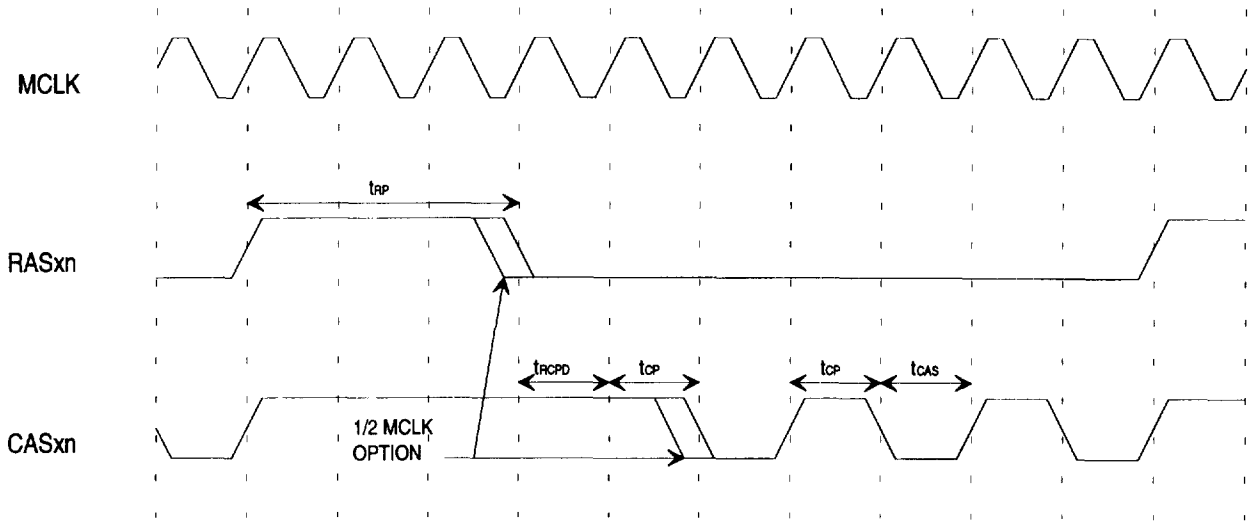


Figure 9.28 - Programmable Parameters

Memory Interface Timimg

No	Symbol	Parameter	Min (tMP)	Max (tMP)	Tol. (ns)	Load (pF)	Notes
	tRC	*Random Rd/Wr Cycle time*	*5*	*13*			1
	tPC	*Fast Page Mode Cycle Time*	*2*	*4*			1
	tRAC	*Access Time From RASn*	*3*	*8*			1
	tCAC	*Access Time From CASn*	*1*	*2.5*			1
	tAA	*Access Time From Col. Addr. (MA)*	*2*	*4*			1
	tCPA	*Access Time From CASn Precharge*	*2*	*4*			1
	tOFF	*Output Buffer Turn-off Delay ****	*1*	*2*			1
M4	tRP	RASn Precharge Time	1.5	5		100	
M5	tRAS	RASn Pulse Width	3	8		100	2
M6	tRSH	RASn Hold Referenced to CASn	1	2		100	
M7	tCSH	CASn Hold Referenced to RASn	3	8		100	
M8	tCAS	CASxn Pulse Width	1	2.5		100	
M9	tCP	CASxn Precharge Time	0.5	2		100	
M10	tRCD	RASxn to CASn Delay Time	1.5	6		100	
M11	tRAD	RASxn to Column Address Delay Time	1	4		100	
M12	tASR	Row Address Setup Time	0.5	1		100	
M13	tRAH	Row Address Hold Time	1	1.5		100	
M14	tASC	Column Address Setup Time	0.5	2		100	

No	Symbol	Parameter	Min (tMP)	Max (tMP)	Tol. (ns)	Load (pF)	Notes
M15	tCAH	Column Address Hold Time	1	2.5		100	
M16	tAR	Column Address Hold Ref. to RASxn	3	8		100	2
M17	tRAL	Column Address to RASn Lead Time	2	4		100	
M18	tWCH	WExxn Hold Ref. to CASxn	1	2		100	
M19	tWCR	WExxn Hold Ref. to RASxn	3	8		100	
M20	tWP	WExxn Pulse Width	1.5	2.5		100	
M21	tRWL	WExxn to RASn Lead Time	1.5	2.5		100	2
M22	tCWL	WExxn to CASn Lead Time	1.5	2.5		100	
M23	tWCS	WExxn Setup to CASxn	0	0.5		100	
M24	tDS	MD Setup to CASxn	1	2		100	
M25	tDH	MD Hold to CASxn	1	2		100	
M26	tDHR	MD Hold Ref. to RASxn	3	8		100	
M27	tCSR	CASn Setup to RASxn (Ref. Cycle)	0.5	1		100	3
M28	tCHR	CASn Hold to RASxn (Ref. Cycle)	2	2.5		100	3

Notes:

1. These parameters are for reference only.
2. The maximum specified is for maximum programmable for a single cycle, it is not the absolute maximum.
3. These parameters are for CAS-before-RAS refresh only.

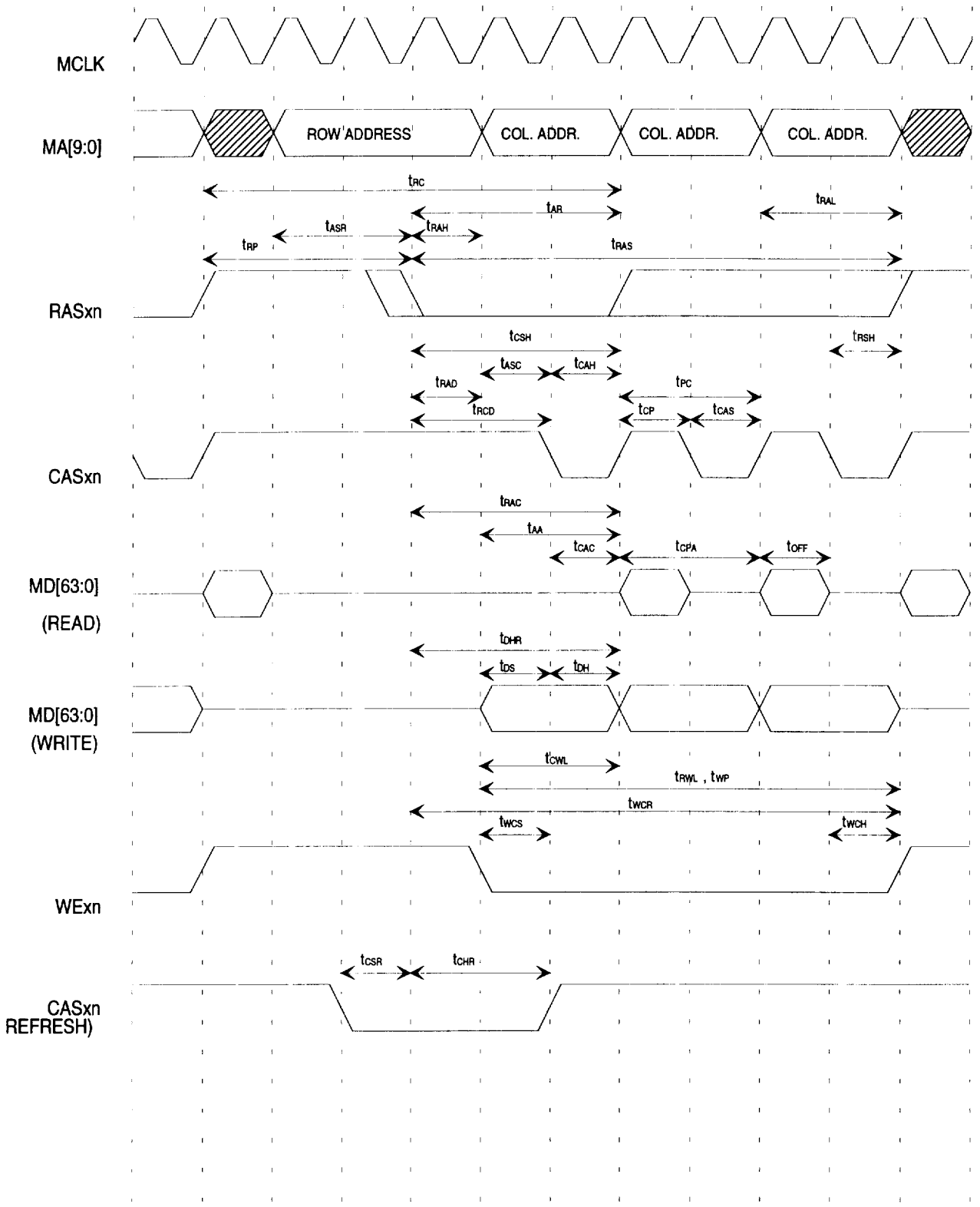


Figure 9.29 - Memory Interface Timing

Standard Memory Design for 70ns and 45ns DRAM's

Symbol	Parameter	DS1	50MHz	DS1	50Mhz	DS2	66MHz	DS2	66MHz
	Half clock option	off		on		off		on	
tMP	Memory Clock Period		20		20		15		15
tRC	Random Rd/Wr Cycle time	7	140	7	140	6	90	6	90
tPC	Fast Page Mode Cycle Time	2	40	2	40	2	30	2	30
tRAC	Access Time From RASn	4	80	4	80	3.5	52.5	3.5	52.5
tCAC	Access Time From CASn	1	20	1.5	30	1	15	1.5	22.5
tAA	Access Time From Col. Addr. (MA)	2	40	2	40	2	30	2	30
tCPA	Access Time From CASn Precharge	2	40	2	40	2	30	2	30
tOFF	Output Buffer Turn-off Delay ***	1	20	1.3	25	1.3	18.8	1.3	18.8
tRP	RASn Precharge Time	3	60	3	60	2.5	37.5	2.5	37.5
tRAS	RASn Pulse Width	4	80	4	80	3.5	52.5	3.5	52.5
tRSH	RASn Hold Referenced to CASn	1	20	1.5	30	1	15	1.5	22.5
tCSH	CASn Hold Referenced to RASn	4	80	4	80	3.5	52.5	3.5	52.5
tCAS	CASn Pulse Width	1	20	1.5	30	1	15	1.5	22.5
tRCD	RASn to CASn Delay Time	3	60	3	60	2.5	37.5	2	30
tRAD	RASn to Column Address Delay Time	1	20	1	20	1.5	22.5	1.5	22.5
tCP	CASn Precharge Time	1	20	0.5	10	1	15	0.5	7.5
tASR	Row Address Setup Time	1	20	1	20	0.5	7.5	0.5	7.5
tRAH	Row Address Hold Time	1	20	1	20	1.5	22.5	1.5	22.5
tASC	Column Address Setup Time	1	20	0.5	10	1	15	0.5	7.5
tCAH	Column Address Hold Time	1	20	1.5	30	1	15	1.5	22.5
tAR	Column Address Hold Ref. to RASn	4	80	4	80	3.5	52.5	3.5	52.5

Symbol	Parameter	DS1	50MHz	DS1	50Mhz	DS2	66MHz	DS2	66MHz
tRAL	Column Address to RASn Lead Time	2	40	2	40	2	30	2	30
tWCH	WExxn Hold Ref. to CASn	1	20	1	20	2	30	1.5	22.5
tWCR	WExxn Hold Ref. to RASn	4	80	4	80	3.5	52.5	3.5	52.5
tWP	WExxn Pulse Width	1	20	1.5	30	2	30	1.5	22.5
tRWL	WExxn to RASn Lead Time	1	20	1.5	30	1.5	22.5	1.5	22.5
tCWL	WExxn to CASn Lead Time	2	40	1.5	30	2	30	1.5	22.5
tDS	WExxn Setup to CASn	1	20	0	0	1	15	0.5	7.5
tDS	MD Setup to WExxn	1	20	0.5	10	1	15	0.5	7.5
tDH	MD Hold to WExxn	1	20	1.5	30	1	15	1.5	22.5
tDHR	MD Hold Ref. to RASn	4	80	4	80	3.5	52.5	3.5	52.5
tCSR	CASn Setup to RASn (Ref. Cycle) (3)	1	20	1	20	0.5	7.5	0.5	7.5
tCHR	CASn Hold to RASn (Ref. Cycle) (3)	2	40	2	40	2.5	37.5	2.5	37.5
tRMW	Read-Modify-Write Cycle Time	10	200	10	200	9	135	9	135
tPRMW	Page Read-Modify-Write Cycle Time	5	100	5	100	5	75	5	75

9.3.6 - Multimedia Port Timing

Multimedia Port Timing

No	Symbol	Parameter	Min (ns)	Max (ns)	Load (pf)	Notes
MM1	tMCKP	Multimedia Clock Period	30			
MM2	tMCKL	Multimedia Clock Low Time	10			
MM3	tMCKH	Multimedia Clock High Time	10			
MM4	tMMS	Multimedia Input Setup to IMCLK	4			
MM5	tMMH	Multimedia Input Hold to IMCLK	4			

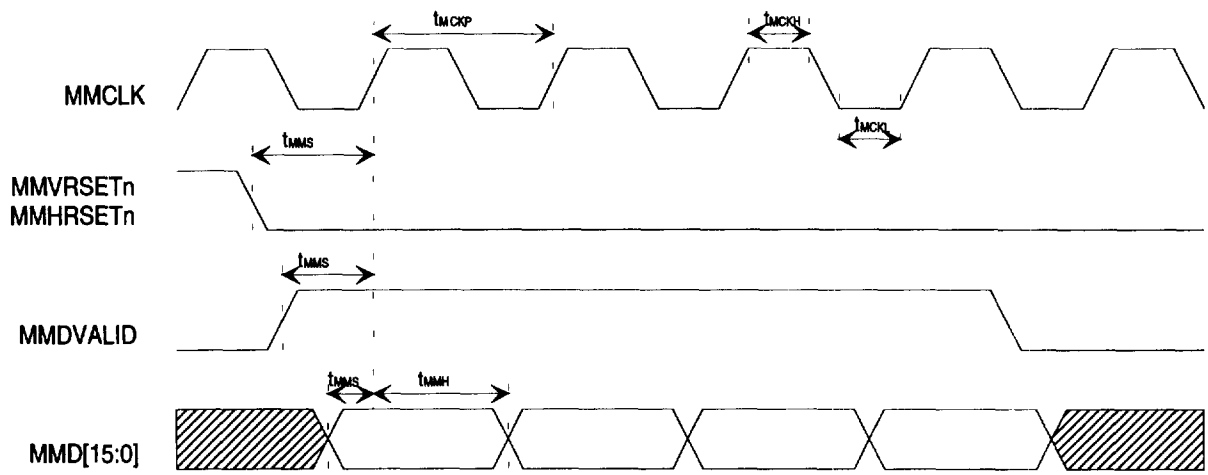


Figure 9.30 - Multimedia Port Timing

Multimedia Output Port (Video Window) Timing - MD64

No	Symbol	Parameter	Min (ns)	Max (ns)	Load (pf)	Notes
MM6	tMCKP	Video Window Clock Period	15			
MM7	tCASD	CASxn Delay from MCLK		10	50	1
MM8	tMXD	MDMXn Delay from MCLK		10	50	1
MM9	tVLD	VDVALID Delay from MCLK		10	50	
	tCAC	*MD[63:0] Valid from CASxn*		*tCAS-2*	50	
	tVDS	*Video Data Setup to MCLK*	*3*			2
	tVDH	*Video Data Hold from MCLK*	*1*			
	t374S	*MD[63:0] Setup to CASxn (Setup of 374)*		*2*	50	
	t374C	*VD[31:0] Delay from CASxn (374 clock to data delay)*		*2*	50	
	t374E	*VD[31:0] Delay from CASxn/MDMXn (374 Enable to data delay)*		*7*	50	

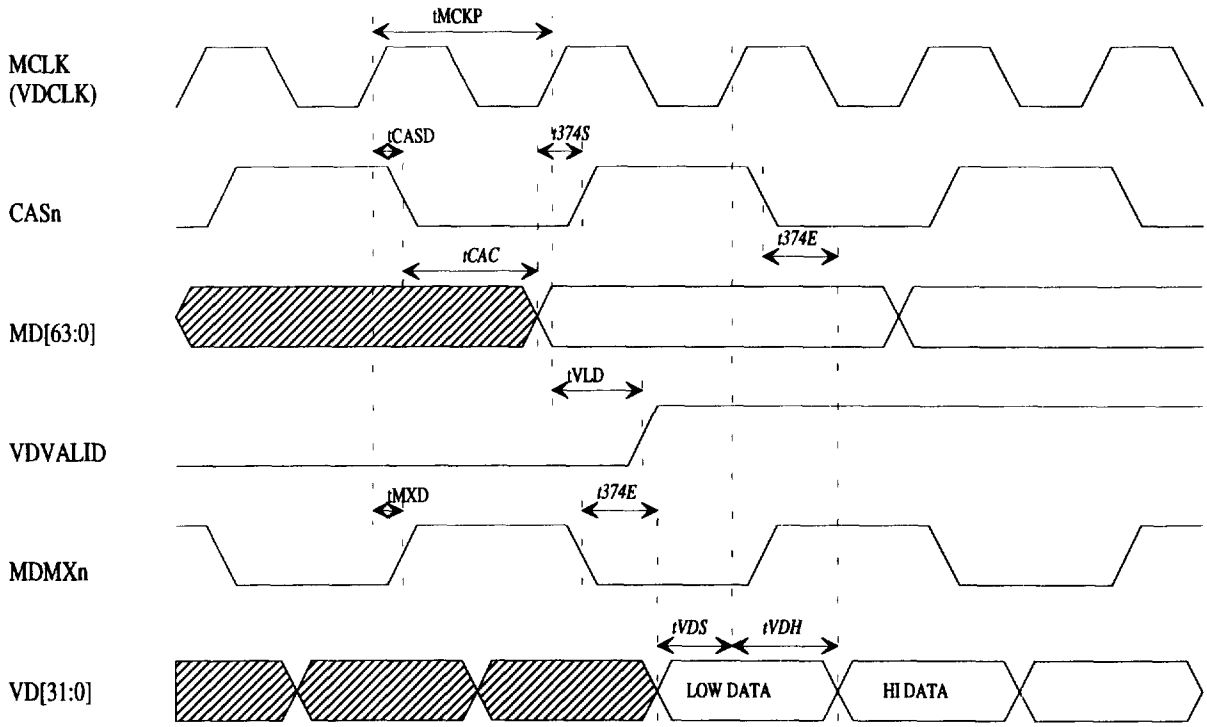


Figure 9.31 - Multimedia Output Port (Video Window) Timing - MD64

Notes:

1. The delays of these two signals should match to avoid contention on VD [31:0].
2. tVDS = tMXD + t374E or tCASD + t374C, whichever is worse. To improve tVDS, MCLK can be buffered to generate VDCLK.