Standard Products

UT82CRH51A USART

Preliminary Data Sheet

December 9, 1999

FEATURES

- Synchronous and asynchronous operation
- Synchronous 5-8 bit characters; internal or external character synchronization; automatic synchronization insertion
- Asynchronous 5-8 bit characters; Clock Rate - 1, 16, or 64 Times Baud Rate; break character generation; 1, 1.5, or 2 stop bits; false start bit detection; automatic break detect and handling
- Synchronous baud rate - 1 to 64K baud
- Asynchronous baud rate - 1 to 19.2K baud
- Full-Duplex, double-buffered transmitter and receiver
- Error detection - parity, overrun and framing errors
- Radiation-hardened process and design; total dose iradiation testing to MIL-STD-883 Method 1019
  - Total-dose: 300 krad(Si)
  - SEL LET threshold: greater than 120MeV-cm^2/mg
  - Neutron Fluence: 3.0E14n/cm^2
- Packaging options:
  - 36-lead Flatpack
  - 68-lead Flatpack
- 5.0 and 3.3 volt operation
- Standard Microcircuit Drawing 5962-00505
  - QML Q and V compliant part
- Available as core IP for ASIC applications

INTRODUCTION

The UT82CRH51A is an enhanced version of the industry standard, Universal Synchronous/Asynchronous Receiver Transmitter (USART), designed to provide data communications between subsystem. The UT82CRH51A USART is built using UTMC's Commercial RadHard^{TM} epitaxial CMOS technology and is ideal for space applications. In a communication environment an interface device converts parallel format system data into serial format for transmission, and converts incoming serial format data into parallel system data for reception. The UT82CRH51A is used as a peripheral device and is programmed by a host CPU to operate using virtually any serial data transmission technique. The USART accepts data characters from the CPU in a parallel format and then converts the data into a continuous serial data stream for transmission. Simultaneously, the UT82CRH51A receives serial data streams and converts the data into a parallel data character for the host CPU. The USART signals the CPU whenever it accepts a new character for transmission or whenever it has received a character for the CPU. The CPU reads the complete status of the USART at any time. These include data transmission errors and control signals such as SYNDET/BRKDET, TxEMPTY.

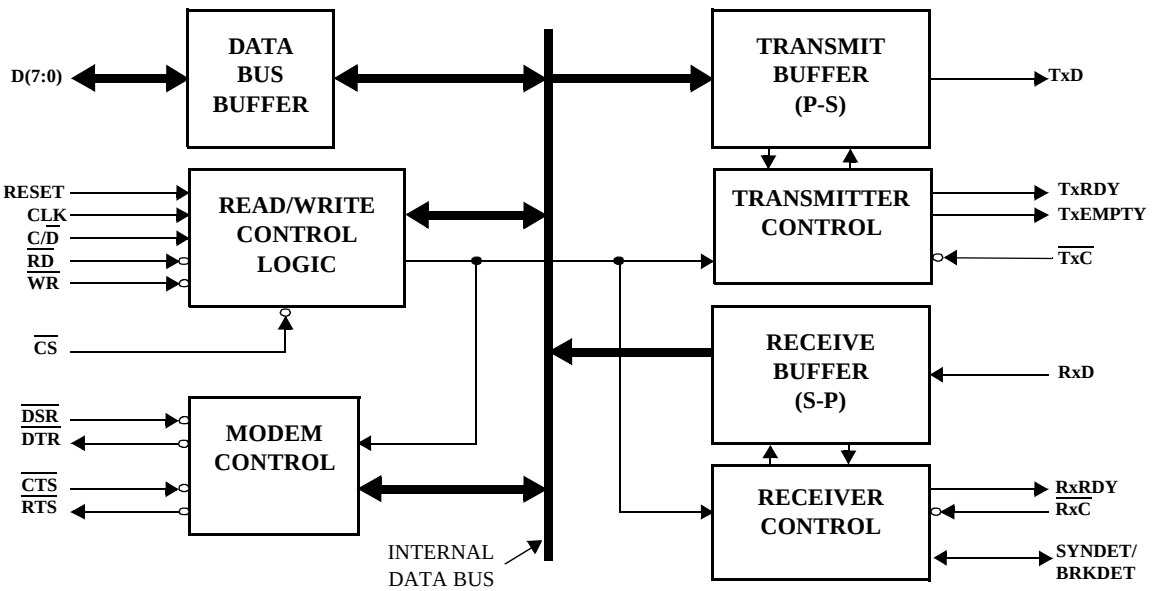


Figure 1. UT82CRH51A USART Block Diagram

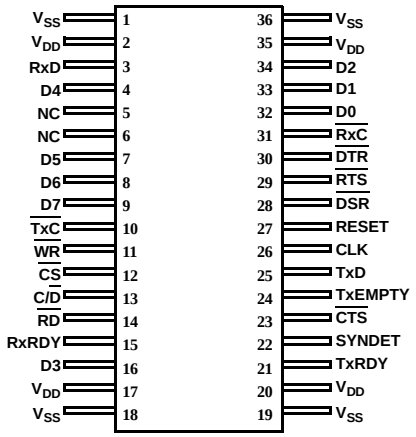


Figure 2. UT82CRH51A Pinout (36)

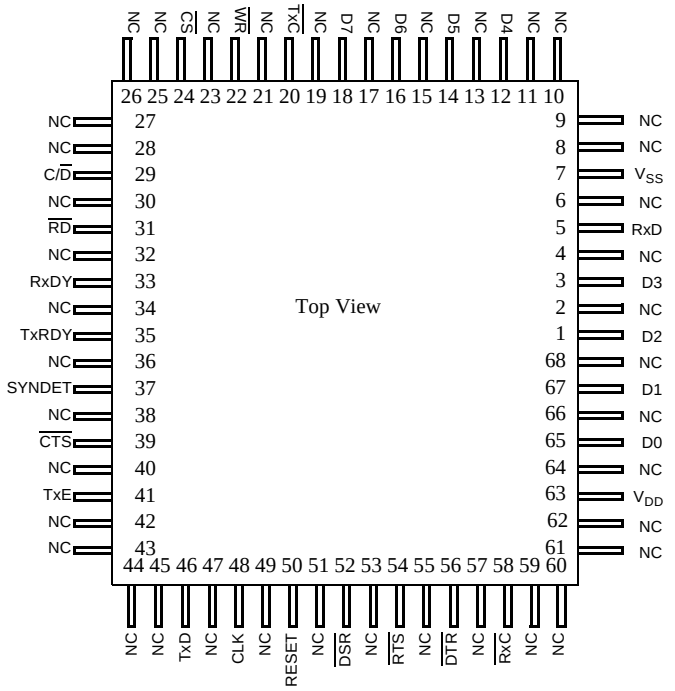


Figure 3. UT82CRH51A Pinout (68)

1.0 Functional Description

The UT82CRH51A is designed for a wide range of microcomputers. Like other I/O devices in a microcomputer system, its functional configuration is programmed by the system's software for maximum flexibility. The UT82CRH51A can support most serial data techniques in use.

In a communication environment an interface device must convert parallel format system data into serial format for transmission and convert incoming serial format data into parallel system data for reception. The interface device must also delete or insert bits or characters that are functionally unique to the communication technique. Therefore, the interface should appear "transparent" to the CPU, a simple input or output of byte-oriented system data (figure 7).

1.1 DATA BUS BUFFER

This three-state, bidirectional, 8-bit buffer is used to interface the UT82CRH51A to the system Data Bus. Data is transmitted or received by the buffer upon execution of INput or OUTput instructions of the CPU. Control words, Command words and Status information are also transferred through the Data Bus Buffer. The Command Status, Data-In and Data-Out registers are separate, 8-bit registers communicating with the system bus through the Data Bus Buffer.

This functional block accepts inputs from the system Control bus and generates control signals for overall device operation. It contains the Control Word Register and Command Word Register that store the various control formats for the device functional definition.

1.2 READ/WRITE CONTROL LOGIC

1.2.1 RESET (Reset)

A "high" on this input forces the UT82CRH51A into an "Idle" mode. The device remains at "Idle" until a new set of control words is written into the UT82CRH51A to program its functional definition. Minimum RESET pulse width is $6t_{CY}$ (clock must be running).

A command reset operation also puts the device into the "Idle" state.

1.2.2 CLK (CLOCK)

The CLK input is used to generate internal device timing and is normally connected to the Phase 2 (TTL) output of the Clock Generator. No external inputs or outputs are referenced to CLK, but the frequency of CLK must be greater than 30 times the Receiver or Transmitter data bit rates.

1.2.3 $\overline{\text{WR}}$ (Write)

A "low" on this input informs the UT82CRH51A the CPU is writing data or control words to the UT82CRH51A (figure 4).

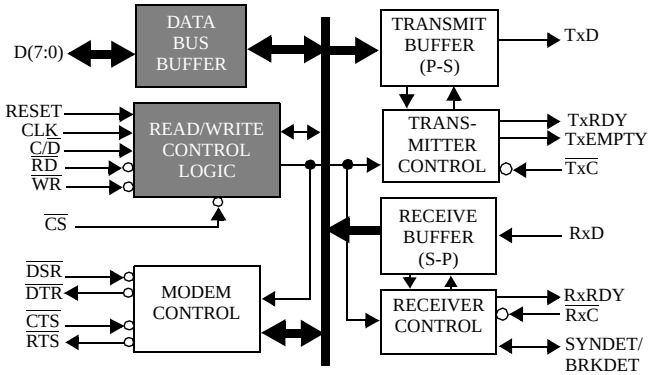


Figure 4. UT82CRH51A Block Diagram Showing Data Bus Buffer and Read/Write Logic Functions

1.2.4 $\overline{RD}$ (Read)

A "low" on this input informs the UT82CRH51A the CPU is reading data or status information from the UT82CRH51A (figure 4).

C/$\overline{D}$	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	
0	0	1	0	DATA -> DATA BUS
0	1	0	0	DATA BUS -> DATA
1	0	1	0	STATUS -> DATA BUS
1	1	0	0	DATA BUS -> CONTROL
X	1	1	0	DATA BUS -> 3-STATE
X	X	X	1	DATA BUS -> 3-STATE

1.2.5 C/$\overline{D}$ (Control/Data)

This input, in conjunction with the $\overline{WR}$ and $\overline{RD}$ inputs, informs the UT82CRH51A the word on the Data Bus is either a data character, control word or status information.

1 = CONTROL/STATUS; 0 = DATA

1.2.6 $\overline{CS}$ (Chip Select)

A "low" on this input selects the UT82CRH51A. No reading or writing will occur unless the device is selected. When $\overline{CS}$ is high, the Data Bus is in the float state and $\overline{RD}$ and $\overline{WR}$ have no effect on the chip.

1.3 MODEM CONTROL

The UT82CRH51A has a set of control inputs and outputs that can be used to simplify the interface to almost any modem. The modem control signals are general purpose in nature and can be used to functions, other than modem control, if necessary (figure 5).

1.3.1 $\overline{DSR}$ (Data Set Ready)

The $\overline{DSR}$ input signal is a general-purpose, 1-bit inverting input port. Its condition can be tested by the CPU using a Status Read operation. The $\overline{DSR}$ input is normally used to test modem conditions such as Data Set Ready.

1.3.2 $\overline{DTR}$ (Data Terminal Ready)

The $\overline{DTR}$ output signal is a general-purpose, 1-bit inverting output port. It can be set "low" by programming the appropriate bit in the Command Instruction word. The $\overline{DTR}$ output signal is normally used for modem control such as Data Terminal Ready.

1.3.3 $\overline{RTS}$ (Request to Send)

The $\overline{RTS}$ output signal is a general-purpose, 1-bit inverting output port. It can be set "low" by programming the appropriate bit in the Command Instruction word. The $\overline{RTS}$ output signal is normally used for modem control such as Request to Send.

1.3.4 $\overline{CTS}$ (Clear to Send)

A "low" on this input enables the UT82CRH51A to transmit serial data if the TxEnable bit in the Command byte is set to a "one". If either a TxEnable off or $\overline{CTS}$ off condition occurs while the Tx is in operation, the Tx transmits all the data in the USART written prior to TxDisable command before shutting down.

1.4 TRANSMIT BUFFER

The Transmit Buffer Accepts parallel data from the Data Bus Buffer, converts it to a serial bit stream, inserts the appropriate characters or bits (based on the communication technique) and outputs a composite serial stream of data on the TxD output pin on the falling edge of TxC. The transmitter begins transmission upon being enabled if $\overline{CTS}$ = 0. The TxD line will be held in the marking state immediately upon a master Reset or when TxEnable or $\overline{CTS}$ is off or the transmitter is empty (figure 5).

1.5.TRANSMITTER CONTROL

The Transmitter Control manages all activities associated with the transmission of serial data. It accepts and issues signals both externally and internally to accomplish this function (figure 5).

1.5.1 TxRDY (Transmitter Ready)

This output signals the CPU the transmitter is ready to accept a data character. The TxRDY output pin can be used as an interrupt to the system since it is masked by TxEnable; or, for Polled operation, the CPU can check TxRDY using a Status Read operation. TxRDY is automatically reset by the leading edge of $\overline{WR}$ when a data character is loaded from the CPU.

Note: When using the Polled operation, the TxRDY status bit is *not* masked by TxEnable, but will only indicate the Empty/ Full Status of the Tx Data Input Register.

1.5.2 TxEMPTY (Transmitter Empty)

When the UT82CRH51A has no characters to send, the TxEMPTY output will go "high". It resets upon receiving a character

from the CPU if the transmitter is enabled. TxEMPTY remains low when the transmitter is disabled even if it is actually empty. TxEMPTY can be used to indicate the end of a transmission mode, so the CPU knows when to turn the line around in the half-duplex operational mode.

In the Synchronous mode, a "high" on this output indicates that a character has not been loaded and the SYNC character or characters are about to be or are being transmitted automatically as "fillers". TxEMPTY does not go low when the SYNC characters are being shifted out.

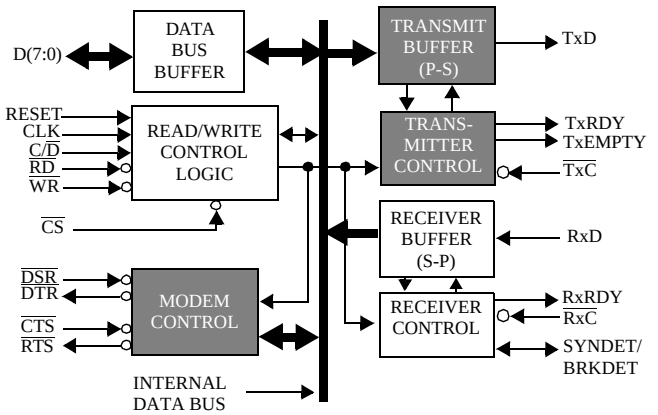


Figure 5. UT82CRH51A Block Diagram Showing Modem and Transmitter Buffer and Control Functions

1.5.3 $\overline{\text{TxC}}$ (Transmitter Clock)

The Transmitter Clock controls the rate at which the character is to be transmitted. In the Synchronous transmission mode, the Baud Rate (1x) is equal to the $\overline{\text{TxC}}$ frequency. In Asynchronous transmission mode, the baud rate is a fraction of the actual $\overline{\text{TxC}}$ frequency. A portion of the mode instruction selects this factor; it can be 1, 1/16 or 1/64 the $\overline{\text{TxC}}$.

For example:

If Baud Rate equals 110 Baud,
$\overline{\text{TxC}}$ equals 110 Hz in the 1x mode
$\overline{\text{TxC}}$ equals 1.72 kHz in the 16x mode
$\overline{\text{TxC}}$ equals 7.04 kHz in the 64x mode

The falling edge of $\overline{\text{TxC}}$ shifts the serial data out of the UT82CRH51A.

1.6 RECEIVE BUFFER

The Receiver accepts serial data, converts this serial input to parallel format, checks for bits or characters that are unique to the communication technique and sends an "assembled" character to the CPU. Serial data is input to RxD pin, and is clocked in on the rising edge of RxC (figure 6).

1.7 RECEIVER CONTROL

This functional block manages all receiver-related activities which consists of the following features (figure 6).

- The RxD initialization circuit prevents the UT82CRH51A from mistaking an unused input line for an active low data line in the "break condition". Before starting to receive serial characters on the RxD line, a valid "1" must first be detected after a chip master Reset. Once this has been determined, a search for a valid low (Start bit) is enabled. This feature is only active in the asynchronous mode, and is only done once for each master Reset.

- The False Start bit detection circuit prevents false starts due to a transient noise spike by first detecting the falling edge and then strobing the nominal center of the Start bit (RxD = low).

- Parity error detection sets the corresponding status bit.

- The Framing Error status bit is set if the Stop bit is absent at the end of the data byte (asynchronous mode).

1.7.1 RxRDY (Receiver Ready)

This output indicates the UT82CRH51A contains a character ready to be input to the CPU. RxRDY can be connected to the interrupt structure of the CPU or, for polled operation, the CPU checks the condition of RxRDY using a Status Read operation.

RxEnable, when off, holds RxRDY in the Reset Condition. For Asynchronous mode, to set RxRDY, the Receiver must be enabled to sense a Start Bit and a complete character must be assembled and transferred to the Data Output Register. For Synchronous mode, to set RxRDY, the Receiver must be enabled and a character must finish assembly and be transferred to the Data Output Register.

Failure to read the received character from the Rx Data Output Register prior to the assembly of the next Rx Data character will set overrun condition error and the previous character will be written over and lost. If the Rx Data is being read by the CPU when the internal transfer is occurring, overrun error will be set and the old character will be lost.

1.7.2 $\overline{\text{RxC}}$ (Receiver Clock)

The Receiver Clock controls the rate at which the character is to be received. In Synchronous Mode, the Baud Rate (1x) is equal to the actual frequency of $\overline{\text{RxC}}$. In Asynchronous Mode, the Baud Rate is a fraction of the actual $\overline{\text{RxC}}$ frequency. A portion of the mode instruction selects this factor: 1, 1/16 or 1/64 the $\overline{\text{RxC}}$.

For example:

Baud Rate Equals 300 Baud, if
$\overline{\text{RxC}}$ equals 300 Hz in the 1x mode
$\overline{\text{RxC}}$ equals 4800 Hz in the 16x mode
$\overline{\text{RxC}}$ equals 19.2 kHz in the 64x mode

Baude Rate equals 2400 Baude, if
$\overline{\text{RxC}}$ equals 2400 Hz in the 1x mode
$\overline{\text{RxC}}$ equals 38.4 kHz in the 16x mode
$\overline{\text{RxC}}$ equals 153.6 kHz in the 64x mode

Data is sampled into the UT82CRH51A on the rising edge of

$\overline{RxC}$.

NOTE: In most communications systems, the UT82CRH51A handles both the transmission and reception operations of a single link. Consequently, the Receive and Transmit Baud Rates will be the same. Both $\overline{TxC}$ and $\overline{RxC}$ requires identical frequencies for this operation and can be tied together and connected to a single frequency source (Baud Rate Generator) to simplify the interface.

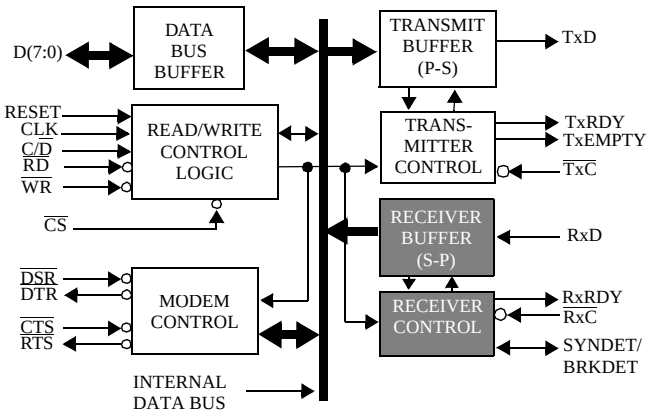


Figure 6. UT82CRH51A Block Diagram Showing Receiver Buffer and Control Functions

1.7.3 SYNDET (SYNC Detect/BRKDET Break Detect)

This pin is used in Synchronous Mode for SYNDET and may be used as either input or output programmable through the Control Word. It is reset to output mode low upon RESET. When used as an output (internal Sync mode), the SYNDET pin goes high to indicate that the UT82CRH51A has located the SYNC character in the Receive mode. If the UT82CRH51A is programmed to use double Sync characters (bisync), then SYNDET goes high in the middle of the last bit of the second Sync character. SYNDET automatically resets upon a Status Read Operation.

When used as an input (external SYNC detect mode), a positive going signal causes the UT82CRH51A to start assembling data characters on the rising edge of the next $\overline{RxC}$. Once in SYNC, the "high" input signal can be removed. When External SYNC Detect is programmed, Internal SYNC Detect is disabled.

1.7.4 BREAK (Async Mode Only)

This output goes high whenever the receiver remains low through two consecutive stop bit sequences (including the start bits, data bits, and parity bits). Break Detect may also be read as a Status bit. It is reset only upon a master chip Reset or Rx Data returning to a "one" state.

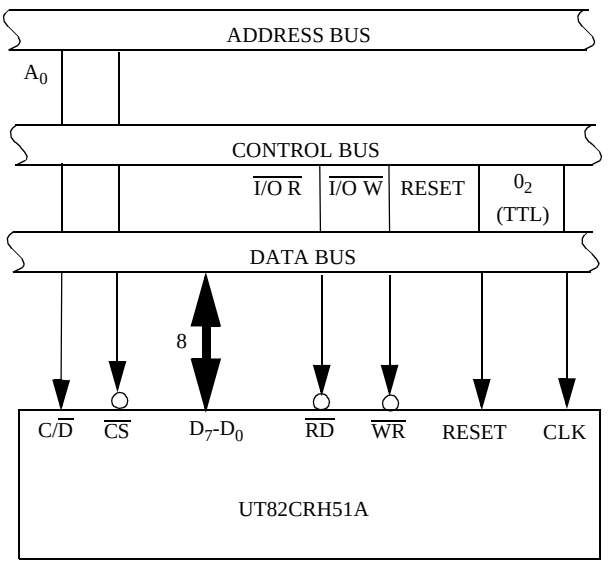


Figure 7. UT82CRH51A Interface to Standard System Bus

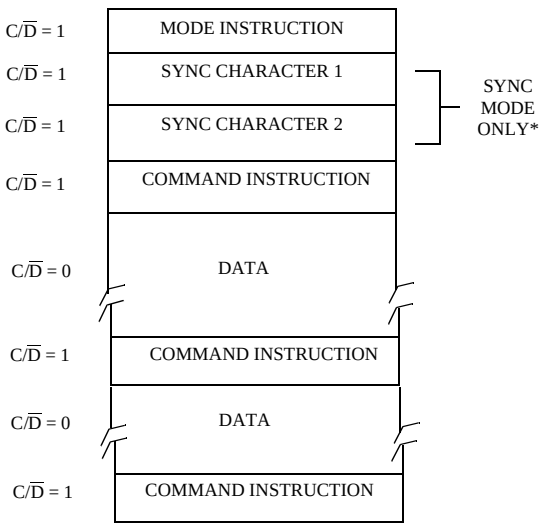
2.0 DETAILED OPERATION DESCRIPTION

2.1 General

The complete functional definition of the UT82CRH51A is programmed by the system's software. A set of control words must be sent out by the CPU to initialize the UT82CRH51A to support the desired communications format. These control words will program the: BAUD RATE, CHARACTER LENGTH, NUMBER OF STOP BITS, SYNCHRONOUS or ASYNCHRONOUS OPERATION, EVEN/ODD/OFF PARITY, etc. In the Synchronous Mode, options are also provided to select either internal or external character synchronization (figure 8).

Once programmed, the UT82CRH51A is ready to perform its communication functions. The TxRDY output is raised "high" to signal the CPU the UT82CRH51A is ready to receive a data character from the CPU. This output (TxRDY) is reset automatically when the CPU writes a character into the UT82CRH51A. On the other hand, the UT82CRH51A receives serial data from the MODEM or I/O device. Upon receiving an entire character, the RxRDY output is raised "high" to signal the CPU the UT82CRH51A has completed character ready for the CPU to fetch. RxRDY is reset automatically upon the CPU data read operation.

The UT82CRH51A cannot begin transmission until the TxEnable (Transmitter Enable) bit is set in the Command Instruction and it has received a Clear to Send ($\overline{CTS}$) input. The TxD output is held in the marking state upon Reset.



NOTE: The second SYNC character is skipped if MODE instruction has programmed the UT82CRH51A to single character internal SYNC Mode. Both SYNC characters are skipped if MODE instruction has programmed the UT82CRH51A to ASYNC mode or External SYNC mode.

Figure 8. Typical Data Block

2.2 Programming the UT82CRH51A

Prior to starting data transmission or reception, the UT82CRH51A must be loaded with a set of control words generated by the CPU. These control signals define the complete functional definition of the UT82CRH51A and must immediately follow a Reset operation (internal or external).

The control words are split into two formats:

1. Mode Instruction
2. Command Instruction

2.2.1 Mode Instruction

This instruction defines the general operational characteristics of the UT82CRH51A. It must follow a Reset operation (internal or external), once the Mode Instruction has been written into the UT92CRH51A by the CPU, SYNC characters or Command Instructions (figure 8).

2.2.2 Command Instruction

This instruction defines a word that is used to control the actual operation of the UT82CRH51A.

Both the Mode and Command Instructions must conform to a specified sequence for proper device operation (see Figure 8). The Mode Instruction must be written immediately following a Reset operation prior to using the UT82CRH51A for data communication.

All control words written into the UT82CRH51A after the Mode Instruction loads the Command Instruction. Command Instructions can be written into the UT82CRH51A at any time in the data block during the operation of the UT82CRH51A. To return to the Mode Instruction format, the master Reset bit in the Command Instruction word can be set to initiate an internal Reset operation which automatically places the UT82CRH51A back into the Mode Instruction format. Command Instructions must follow the Mode Instructions or Sync characters.

2.2.3 Mode Instruction Definition

The UT82CRH51A can be used for either Asynchronous or Synchronous data communication. To understand how the Mode Instruction defines the functional operation of the UT82CRH51A, the designer views the device as two separate components, one Asynchronous and the other Synchronous, sharing the same package. The format definition can be changed only after a master chip Reset. For explanation purposes the two formats will be isolated.

NOTE: When parity is enabled it is not considered as one of the data bits for the purpose of programming the word length. The actual parity bit received on the Rx Data line cannot be read on the Data bus. In the case of a programmed character length of less than 8 bits, the least significant Data Bus bits holds the data; unused bits are "don't care" when writing data to the UT82CRH51A and will be "zeroes" when reading the data from the UT82CRH51A.

2.2.4 Asynchronous Mode (Transmission)

Whenever a data character is sent by the CPU the UT82CRH51A automatically adds a Start bit (low level) followed by the data bits (least significant bit first), and the programmed number of Stop bits to each character. Also, an even or odd Parity bit is inserted prior to the Stop bit(s) as defined by

the Mode Instruction. The character is then transmitted as a serial data stream on the TxD output. The serial data is shifted out on the falling edge of $\overline{TxC}$ at a rate equal to 1, 1/16, or 1/64 that of the $\overline{TxC}$ as defined by the Mode Instruction. BREAK characters can be continuously sent to the TxD if commanded to do so.

When no data characters have been loaded into the UT82CRH51A the TxD output remains "high" (marking) unless a Break (continuously low) has been programmed (figure 9).

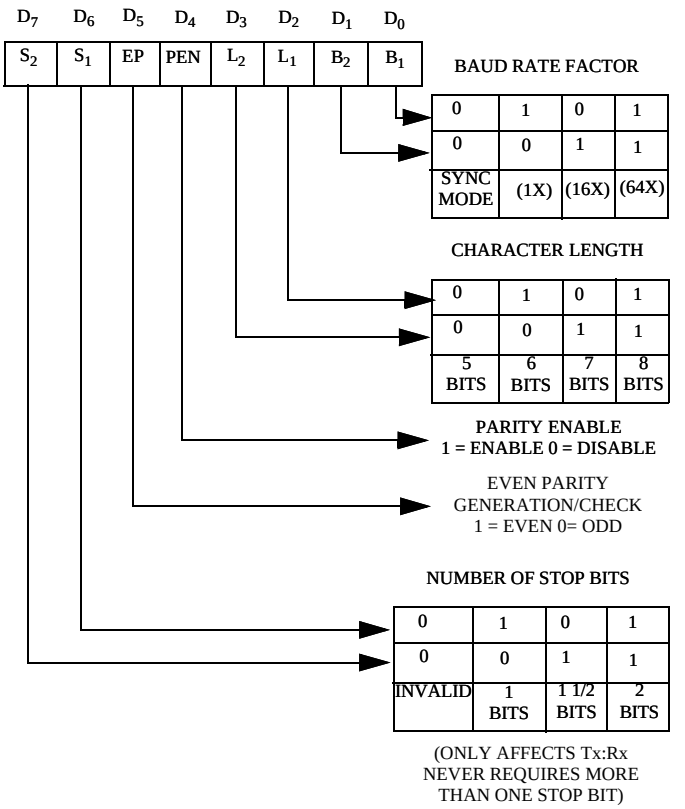


Figure 9. Mode and Command Instruction Format, Asynchronous Node

2.2.5 Asynchronous Mode (Receive)

The RxD line is normally high. A falling edge on this line triggers the beginning of a START bit. The validity of this START bit is checked by again strobing this bit at its nominal center (16x or 64x mode only). If a low is detected again, it is a valid START bit, and the bit counter starts counting. The bit counter thus locates the center of the data bits, the parity bit (if it exists), and the stop bits. If parity error occurs, the parity error flag is set. Data and parity bits are sampled on the RxD pin with the rising edge of $\overline{RxC}$. If a low level is detected as the STOP bit, the Framing Error flag sets. The STOP bit signals the end of a character. **Note:** The *receiver* requires only *one* stop bit regardless of the number of stop bits programmed. This character is then loaded into the parallel I/O buffer of the UT82CRH51A. The RxRDY pin is raised to signal the CPU that a character is ready to be fetched. If a previous character has not been fetched by the CPU, the present character replaces it in the I/O buffer, and the OVERRUN Error flag is raised (thus the previous character is lost). All of the error flags can be reset by an Error Reset Instruction. The occurrence of any of these errors will not affect the operation of the UT82CRH51A (figure 10).

2.2.6 Synchronous Mode (Transmission)

The TxD output is continuously high until the CPU sends its first character to the UT82CRH51A which usually is a SYNC character. When the $\overline{CTS}$ line goes low, the first character is serially transmitted out. All characters are shifted out on the falling edge of $\overline{TxC}$. Data is shifted out at the same rate as the $\overline{TxC}$.

Once transmission has started, the data stream at TxD output continues at the TxC rate. If the CPU does not provide the UT82CRH51A with a data character before the UT82CRH51A Transmitter Buffers become empty, the SYNC characters (or character if in single SYNC character mode) will be automatically inserted in the TxD data stream. In this case, the TxEMPTY pin is raised high to signal that the UT82CRH51A is empty and SYNC characters are being sent out. TxEMPTY does not go low when the SYNC is being shifted out (see figure 11). The TxEMPTY pin is internally reset by a data character being written into the UT82CRH51A.

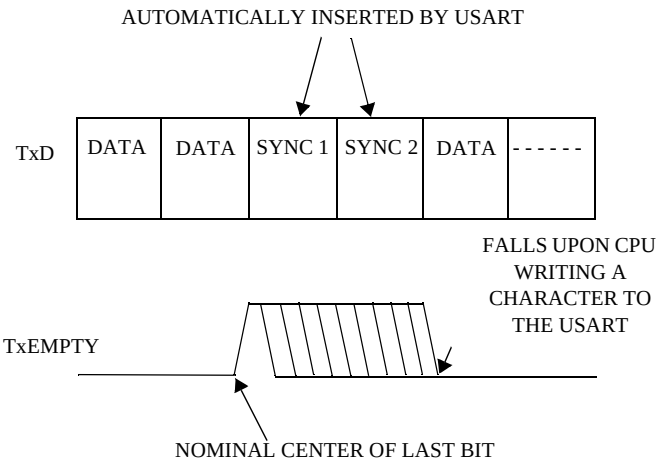


Figure 11. Synchronous Mode

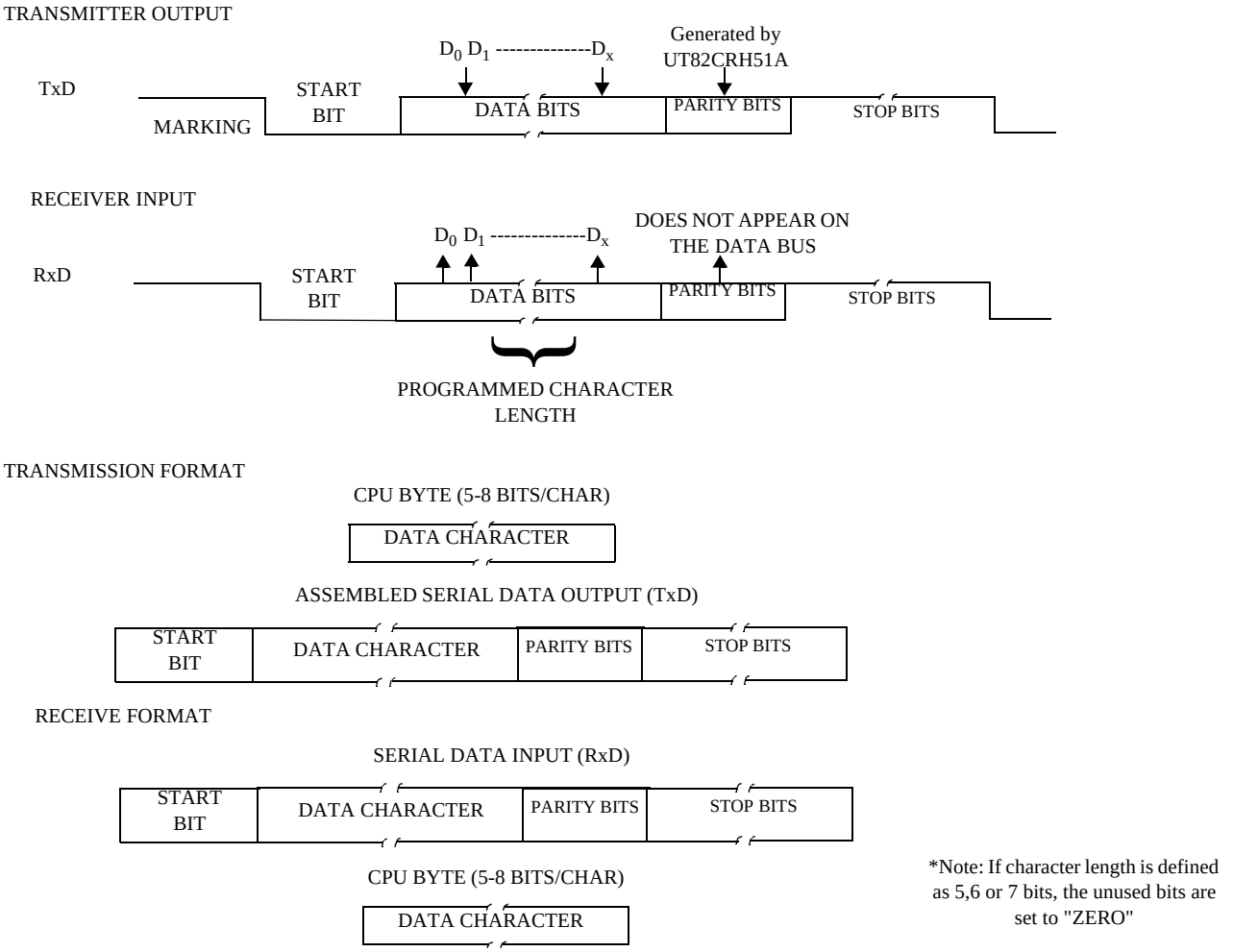


Figure 10. Asynchronous Mode

2.2.7 Synchronous Mode (Receive)

In this mode, character synchronization can be internally or externally achieved. If the SYNC mode has been programmed, an ENTER HUNT command should be included in the first command instruction word written. Data on the RxD pin is then sampled on the rising edge of $\overline{RxC}$. The content of the Rx buffer is compared at every bit boundary with the first SYNC character until a match occurs. If the UT82CRH51A has been programmed for two SYNC characters, the subsequent received character is also compared; when both SYNC characters have been detected, the USART ends the HUNT mode and is in character synchronization. The SYNDET pin is then set high and is reset automatically by a STATUS READ. If parity is programmed, SYNDET will not be set until the middle of the parity bit instead of the middle of the last data bit.

In the external SYNC mode, synchronization is achieved by applying a high level of the SYNDET pin, thus forcing the UT82CRH51A out of the HUNT mode. The high level can be removed after one $\overline{RxC}$ cycle. An ENTER HUNT command has no effect in the asynchronous mode of operation.

Parity error and overrun error are both checked in the same way as in the Asynchronous Rx mode. Parity is checked when not in HUNT, regardless of whether the Receiver is enabled or not (Figure 12).

The CPU can command the receiver to enter the HUNT mode if synchronization is lost. This will also set all the used character bits in the buffer to a "one", thus preventing a possible false SYNDET caused by data that happens to be in the Rx Buffer at ENTER HUNT time. **Note:** The SYNDET F/F is reset at each Status Read regardless of whether internal or external sync has been programmed. This does not cause the UT82CRH51A to return to the HUNT mode. When the SYNC mode but not in HUNT, Sync Detection is still functional, but only occurs at the "known" word boundaries. Thus, if one Status Read indicates SYNDET and a second Status Read also indicates SYNDET, then the programmed SYNDET characters have been received since the previous Status Read. (If double character sync has been programmed, then both sync characters have been contiguously received to gate a SYNDET indication.) When external SYNDET mode is selected, internal Sync Detection is disabled, and the SYNDET F/F may be set at any bit boundary (figure 13).

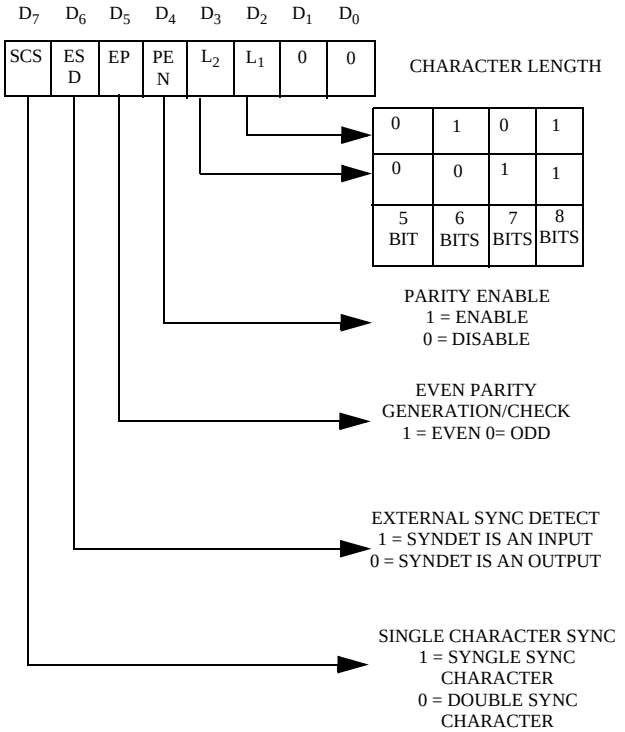


Figure 12. Mode Instruction Format, Synchronous Mode

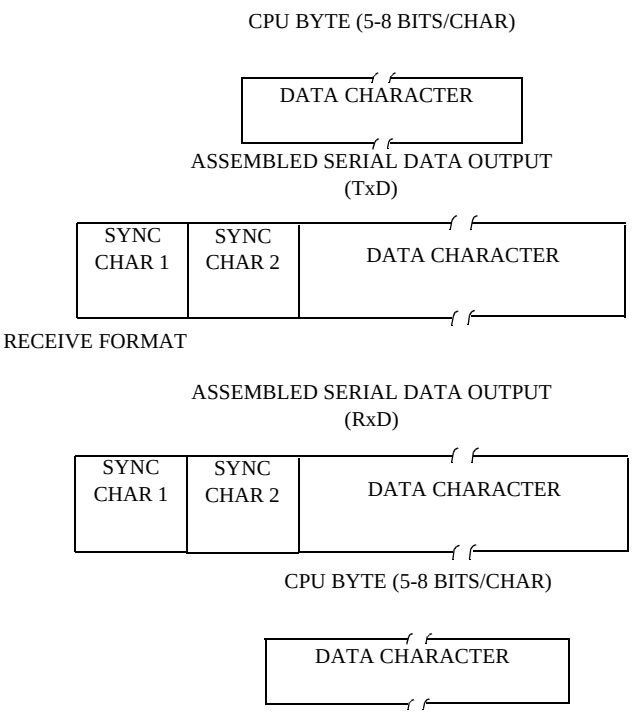


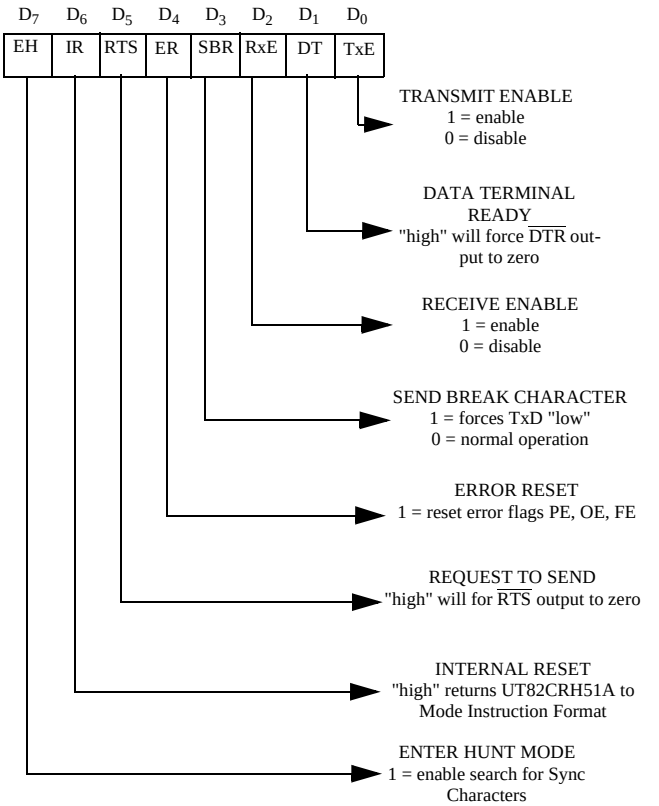
Figure 13. Data Format, Synchronous Mode

3.0 COMMAND INSTRUCTION DEFINITION

Once the functional definition of the UT82CRH51A has been programmed by the Mode Instruction and the sync characters are loaded (if in Sync Mode) then the device is ready to be used for data communication. The Command Instruction controls the actual operation of the selected format. Functions such as Enable Transmit/Receive, Error Reset and Modem Controls are provided by the Command Instruction.

Once the Mode Instruction has been written into the UT82CRH51A and the Sync characters inserted, if necessary, then all further "control write" (C/D = 1) will load a Command Instruction. A Reset Operation (internal or external) returns the UT82CRH51A to the Mode Instruction format. **Note:** Internal Reset on Power-Up

When power is first applied, the UT82CRH51A may come up in the Mode, Sync character or Command format. To guarantee that the device is in the Command Instruction format before the Reset command is issued, it is safest to execute the worst-case initialization sequence (sync mode with two sync characters). Loading three 00Hs consecutively into the device with C/$\overline{D}$ = 1 configures sync operation and writes two dummy 00H sync characters. An Internal Reset command (40H) may then be issued to return the device to the "Idle" state (figure 14).



Note: Error Reset must be performed whenever RxEnable and Enter Hunt are programmed.

Figure 14. Mode Instruction Format, Synchronous Mode

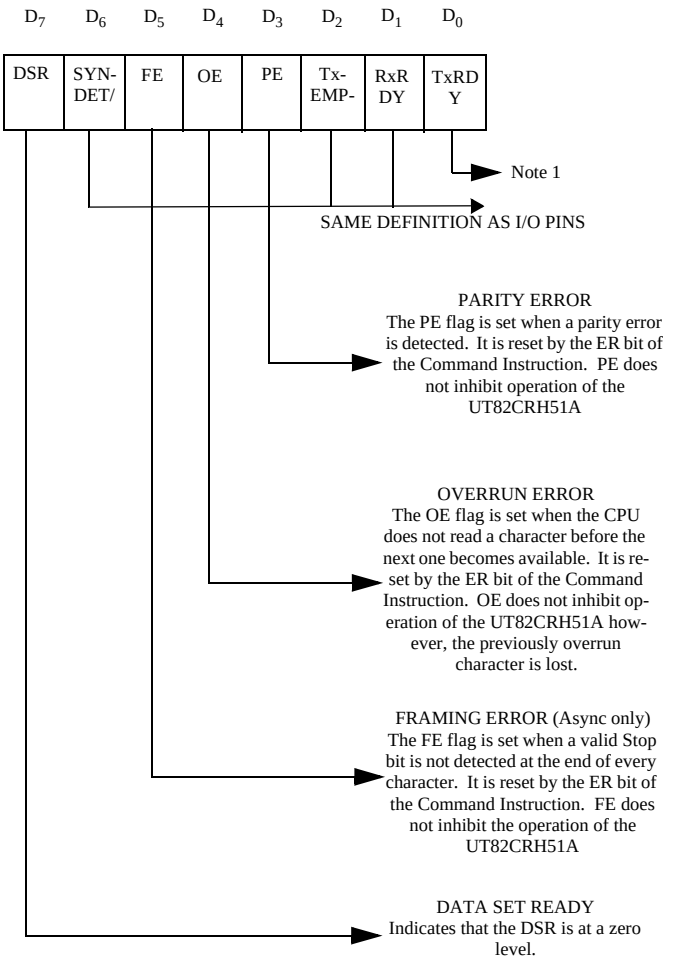
4.0 STATUS READ DEFINITION

In data communication systems it is often necessary to examine the "status" of the active device to ascertain if errors have occurred or other conditions requiring the processor's attention. The UT82CRH51A has facilities that allow the programmer to "read" the status of the device at any time during the functional operation. (Status update is inhibited during status read.)

A normal "read" command is issued by the CPU with C/$\overline{D}$ = 1 to accomplish this function.

Some of the bits in the Status Read Format have identical meanings to external output pins to that the UT82CRH51A can be used in a completely polled or interrupt-driven environment. TxRDY is an exception (figure 15).

Note: Status update can have a maximum delay of 28 clock periods from the actual event affecting the status.



Note : TxRDY status bit has different meanings from the TxRDY output pin. The former is not conditioned by $\overline{CTS}$ and TxEN; the latter is conditioned by both CTS and TxEN.

i.e TxRDY status bit = DB Buffer Empty

TxRDY pin out = DB Buffer Empty + ($\overline{CTS}$-0) + (TxEN-1)

Figure 15. Status Read Format

5.0 APPLICATIONS OF THE UT82CRH51A

Figures 16 thru 19 are examples of UT82CRH51A application environments.

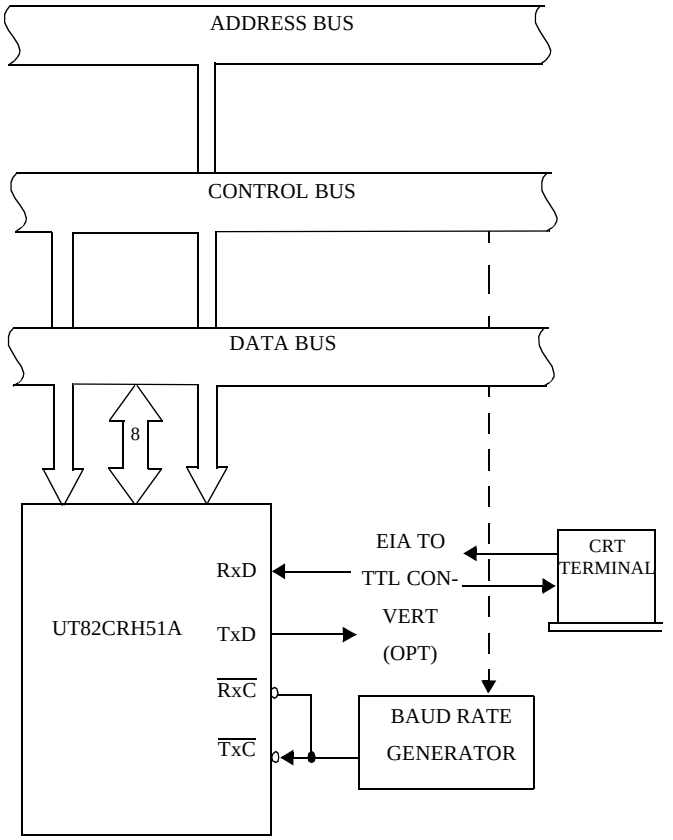


Figure 16. Asynchronous Serial Interface to CRT Terminal, DC-9600 Baud

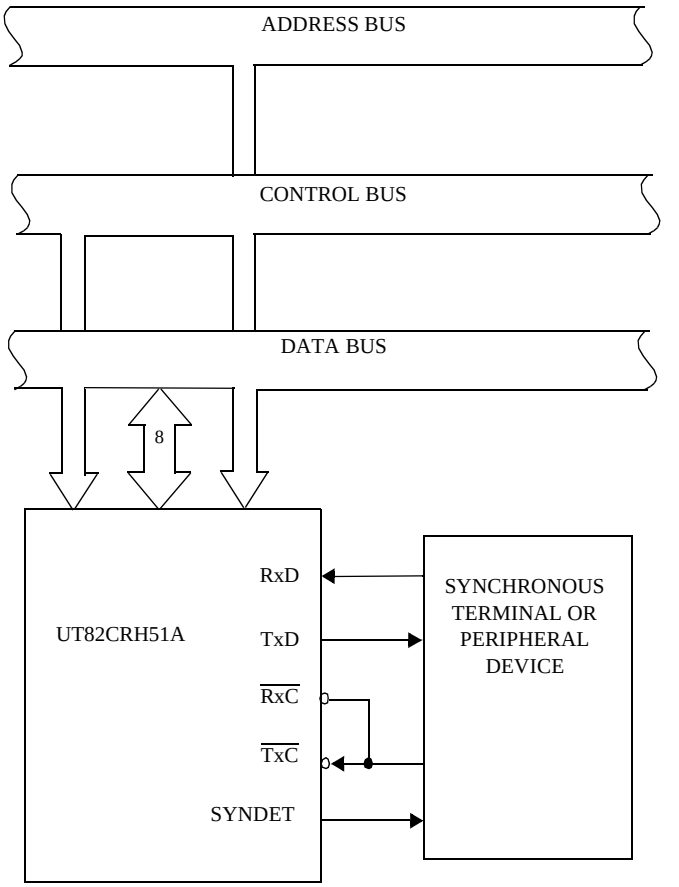


Figure 17. Synchronous Interface to Terminal, or Peripheral Device

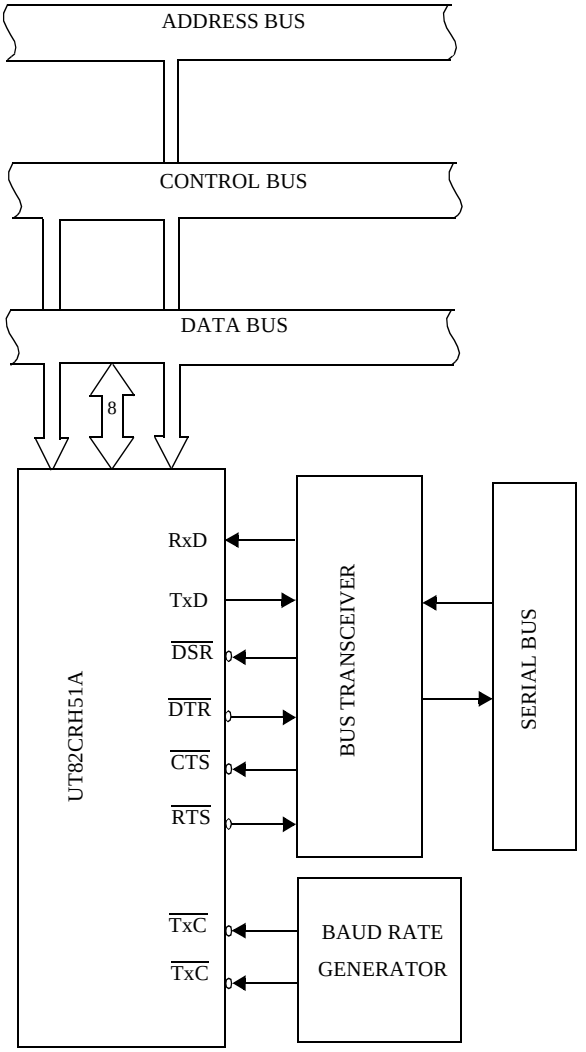


Figure 18. Asynchronous Interface to Serial Bus

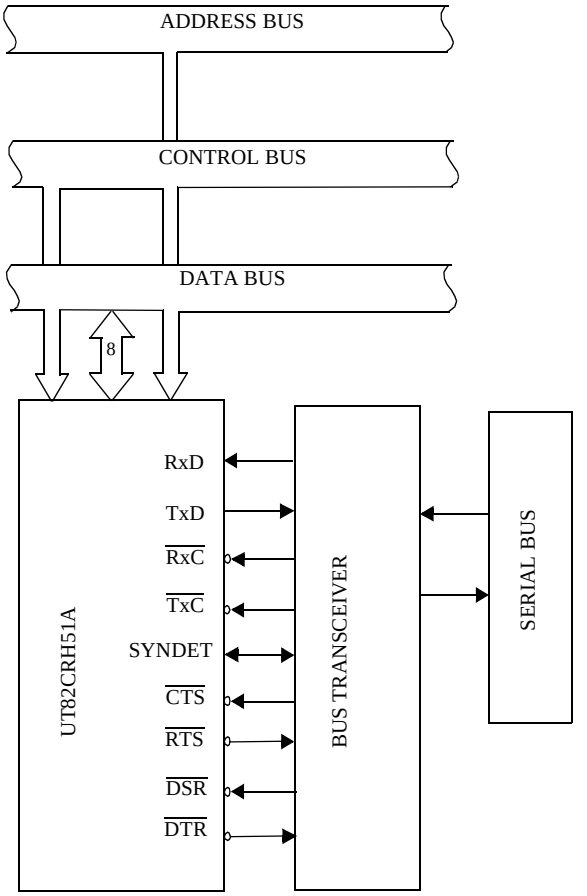


Figure 19. Synchronous Interface to Serial Bus

RADIATION HARDNESS SPECIFICATIONS [1]

PARAMETER	LIMIT	UNITS
Total Dose	300	krad(Si)
SEL Latchup	>120	MeV-cm^2/mg
Neutron Fluence[2]	1.0E14	n/cm^2

Notes:
1. Logic will not latchup during radiation exposure within the limits defined in the table.
2. Not tested, inherent of CMOS technology.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	LIMIT (Mil only)	UNITS
$V_{I/O}$	Voltage any pin	-.5 to +7	V
T_{STG}	Storage Temperature range	-65 to +150	°C
T_J	Maximum junction temperature	+175	°C
P_D	Maximum power dissipation	1	W

Note:
1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, functional operation of the device at these or any other conditions beyond limits indicated in the operational sections is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and performance.

6.0 DC ELECTRICAL CHARACTERISTICS (Pre/Post-Radiation)*

V_{DD} = 5.0V ± 10%; T_A = -55°C to 125°C, GND = 0V)

SYMBOL	PARAMETER	CONDITION	MINIMUM	MAXIMUM	UNIT
V_{IL}	Low-level Input Voltage		-0.5	0.8	V
V_{IH}	High-level Input Voltage		2.2	V_{CC}	V
V_{OL}	Low-level Output Voltage	I_{OL} = 2.2mA		0.45	V
V_{OH}	High-level Output Voltage	I_{OH} = -400µA	2.4		V
I_{OFL}	Output Float Leakage	V_{OUT} = V_{CC} to 0.45V		±10	µA
I_{IL}	Input Leakage	V_{IN} = V_{CC} to 0.45V		±10	µA
I_{CC}	Power Supply Current	All Outputs = High		100	mA
C_{IN}	Input Capacitance	fc = 1MHz		10	pF
$C_{I/O}$	I/O Capacitance	Unmeasured pins returned to GND		20	pF

Notes:

* Post-radiation performance guaranteed at 25°C per MIL-STD-883.

7.0 AC CHARACTERISTICS (Post-Radiation)

(V_{DD} = 5.0V ± 5%; T_A = -55°C to 125°C, GND = 0V)

SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNIT
t_{CY}	Clock Period[1,2]	200	-	ns
t_{CLK}	Clock High Pulse Width	100	-	ns
$t_{\overline{CLK}}$	Clock Low Pulse Width	100		ns
t_R, t_F	Clock Rise and Fall Time		20	ns
t_{DTx}	TxD Delay from Falling Edge of $\overline{TxC}$		1	µs
f_{Tx}	Transmitter Input Clock Frequency 1x Baud Rate 16x Baud Rate 64x Baud Rate	 1 1 1	 64 310 615	kHz
t_{TPW}	Transmitter Input Clock Pulse Width 1x Baud Rate 16x and 64x Baud Rate	 12 1		t_{CY}
t_{TPD}	Transmitter Input Clock Pulse Delay 1x Baud Rate 16x and 64x Baud Rate	 15 3		t_{CY}
f_{Rx}	Receiver Input Clock Frequency 1x Baud Rate 16x Baude Rate 64x Baude Rate	 1 1 1	 64 310 615	kHz
t_{RPW}	Receiver Input Clock Pulse Width 1x Baude Rate 16x and 64x Baude Rate	 12 1		t_{CY}
t_{RPD}	Receiver Input Clock Pulse Width 1x Baude Rate 16x and 64x Baude Rate	 15 3		t_{CY}
t_{TxRDY}	TxRDY Pin Delay from End of Last Bit[3]		35	ns
$t_{TxRDY\ CLEAR}$	TxRDY falling from Leading Edge of $\overline{WR}$ [3]		50	ns
t_{RxRDY}	RxRDY Pin Delay from Center of Last Bit[3]		26	t_{CY}
$t_{RxRDY\ CLEAR}$	RxRDY falling from Leading Edge of $\overline{RD}$ [3]		400	ns
t_{IS}	Internal SYNDET Delay from Rising Edge of $\overline{RxC}$ [3]		26	t_{CY}
t_{ES}	External SYNDET Set-Up Time After Rising Edge of $\overline{RxC}$ [3]	18		t_{CY}
$t_{TxEMPTY}$[4]	TxEMPTY Delay from Center of Last Bit [3]	20	-	t_{CY}
t_{WC}[4]	Control Delay from Rising Edge of WRITE (TxEn, $\overline{DTR}$, $\overline{RTS}$)[3]	8	-	t_{CY}
t_{CR}[4]	Control to READ Set-Up Time ($\overline{DSR}$, $\overline{CTS}$)[3]	20	-	t_{CY}

Note:

* Post-radiation performance guaranteed at 25°C per MIL-STD-883 Method 1019 at 300 krad(Si).

1. The TxC and RxC frequencies have the following limitations with respect to CLK: For 1x Vaude Rate, f_{Tx} or $f_{RX} < 1/(30\ t_{CY})$. For 16x and 64x Baud Rate, f_{Tx} or $f_{Rx} < 1/(4.5\ t_{CY})$.
2. Rest Pulse Width = 6 t_{CY} minimum. System Clock must be running during Reset.
3. Status update can have a maximum delay of 28 clock periods from the event affecting the status.
4. Guaranteed by simulation, not tested.

AC CHARACTERISTICS READ CYCLE (Post-Radiation)[1]

(V_{DD} = 5.0V ± 5%; T_A = -55°C to 125°C, GND = 0V)

SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNIT
t_{AR}[4]	Address Stable Before $\overline{READ}$ ($\overline{CS}$, C/$\overline{D}$)[2]	0	-	ns
t_{RA}[4]	Address Hold Time for $\overline{READ}$ ($\overline{CS}$, C/$\overline{D}$)[2]	0	-	ns
t_{RR}[4]	$\overline{READ}$ Pulse Width	20	-	ns
t_{RD}	Data Delay from $\overline{READ}$ [3] C_L = 150 pF	-	30	ns
t_{DF}	$\overline{READ}$ to Data Floating	1.8	45	ns

Note:

* Post-radiation performance guaranteed at 25°C per MIL-STD-883 Method 1019 at 300 krad(Si).

1. AC timing measured V_{OH} = 2.0, V_{OL} = 0.8.
2. Chip Select (CS) and Command/Data (C/D) are considered as addresses.
3. Assumes that address is valid beroe $\overline{READ}$ falling.
4. Guaranteed by simulation, not tested.

AC CHARACTERISTICS WRITE CYCLE (Post-Radiation)[1]

(V_{DD} = 5.0V ± 5%; T_A = -55°C to 125°C, GND = 0V)

SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNIT
t_{AW}[3]	Address Stable Before $\overline{WRITE}$	0	-	ns
t_{WA}[3]	Address Hold Time for $\overline{WRITE}$	0	-	ns
t_{WW}[3]	$\overline{WRITE}$ Pulse Width	20	-	ns
t_{DW}[3]	Data Delay from $\overline{WRITE}$	15	-	ns
t_{WD}[3]	Data Hold Time for $\overline{WRITE}$	5	-	ns
t_{RV}[3]	Recovery Time Between Writes[2]	6	-	t_{CY}

Note:

* Post-radiation performance guaranteed at 25°C per MIL-STD-883 Method 1019 at 300 krad(Si).

1. AC timing measured V_{OH} = 2.0, V_{OL} = 0.8.
2. This recovery time is for Mode Initialization only. Write data is allowed only when TxRDY = 1. Recovery time between writes for Asynchronous Mode is 8 t_{CY} and for Synchronous Mode is 16 t_{CY}.
3. Guaranteed by simulation, not tested.

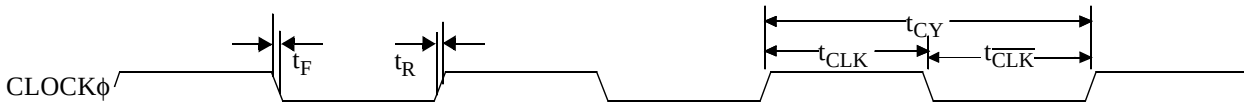


Figure 20. SYS CLOCK

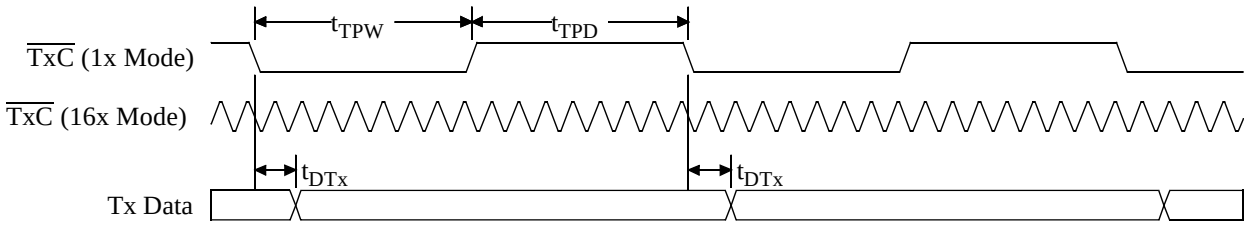


Figure 21. Tx CLOCK And DATA

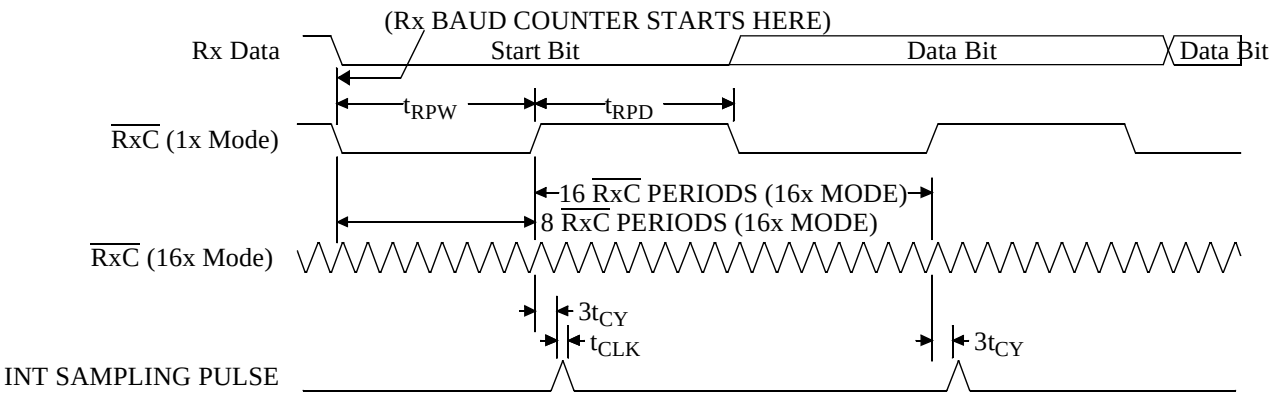


Figure 22. Rx CLOCK And DATA

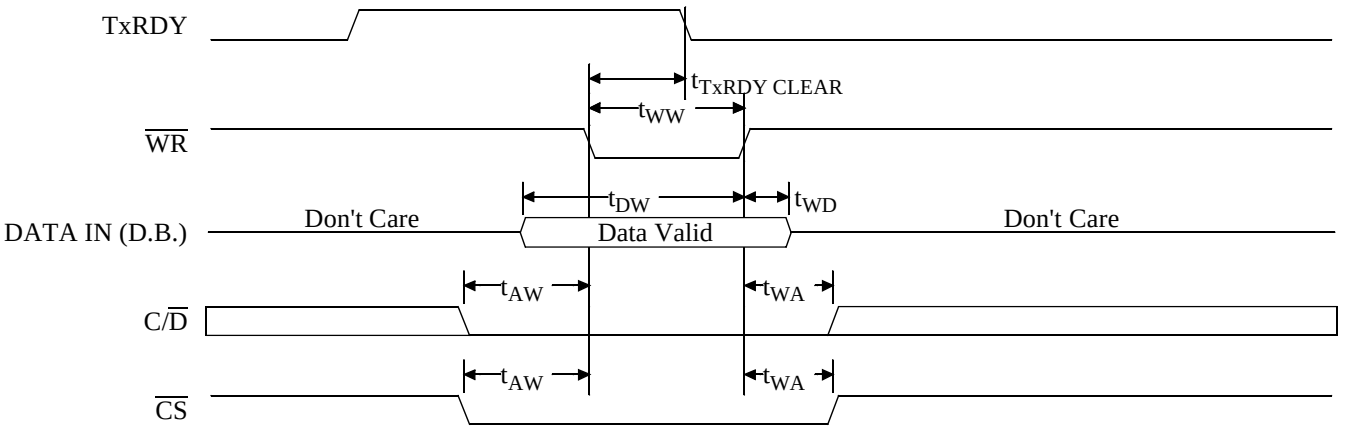


Figure 23. CPU To USART $\overline{WR}$ DATA

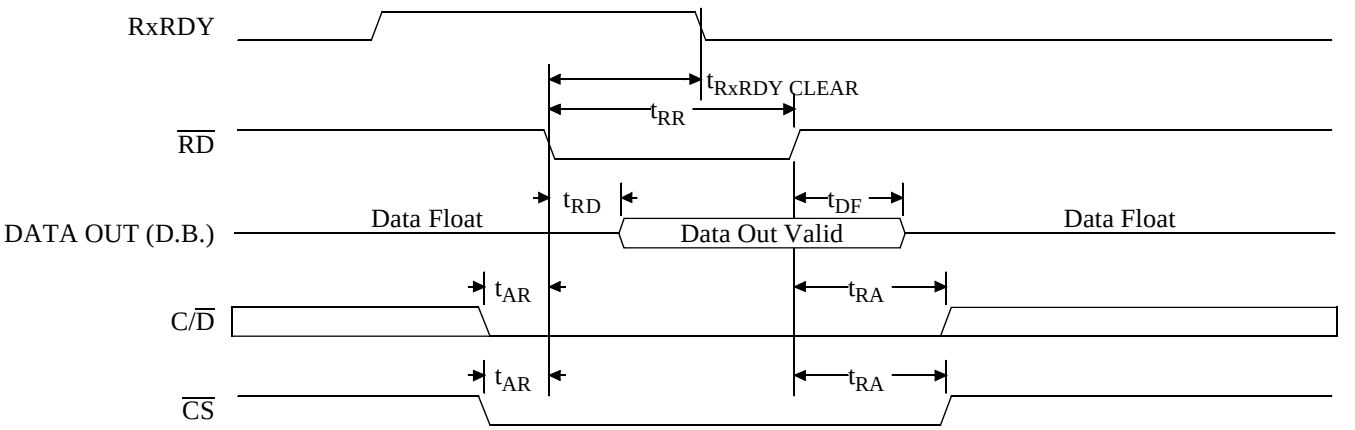


Figure 24. USART To CPU $\overline{RD}$ DATA

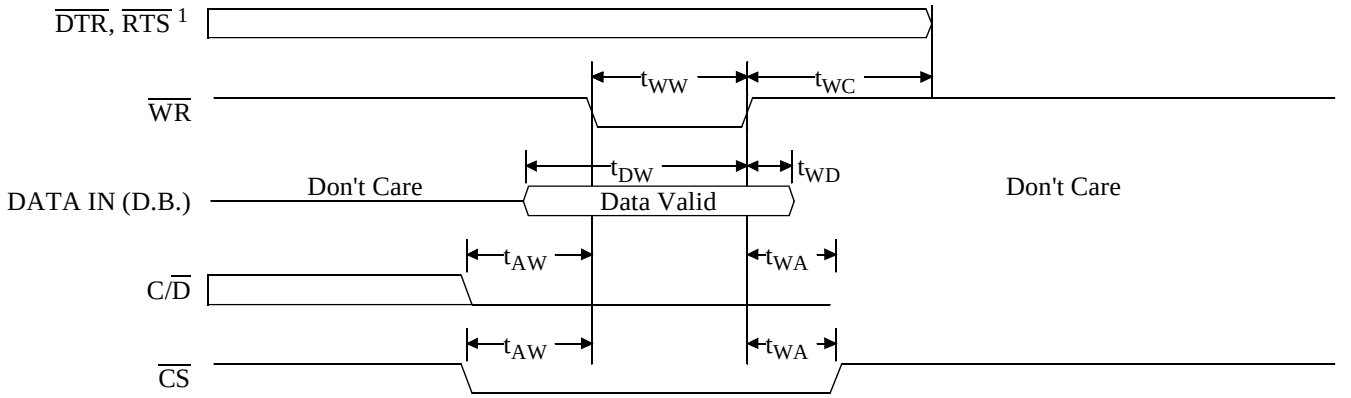


Figure 25. WR CONTROL

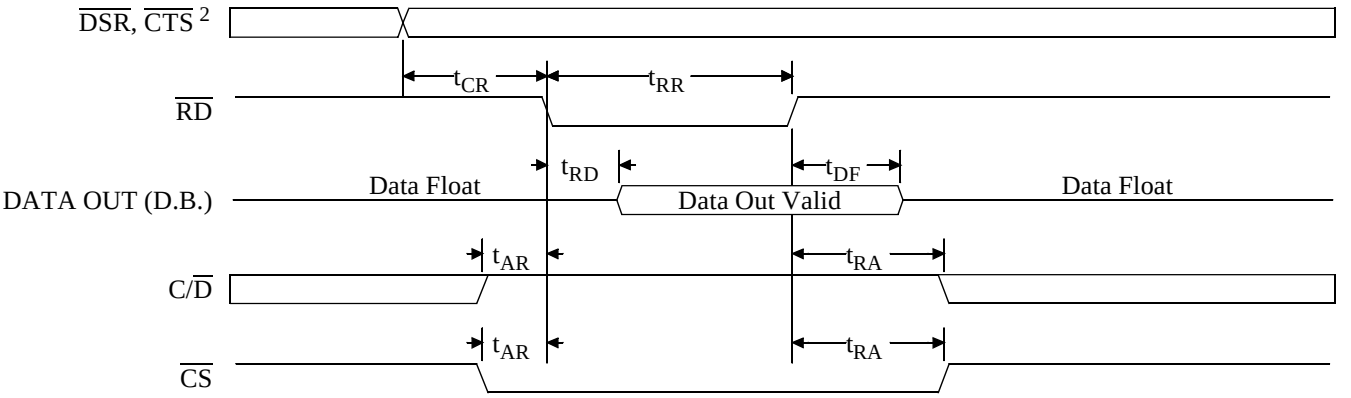
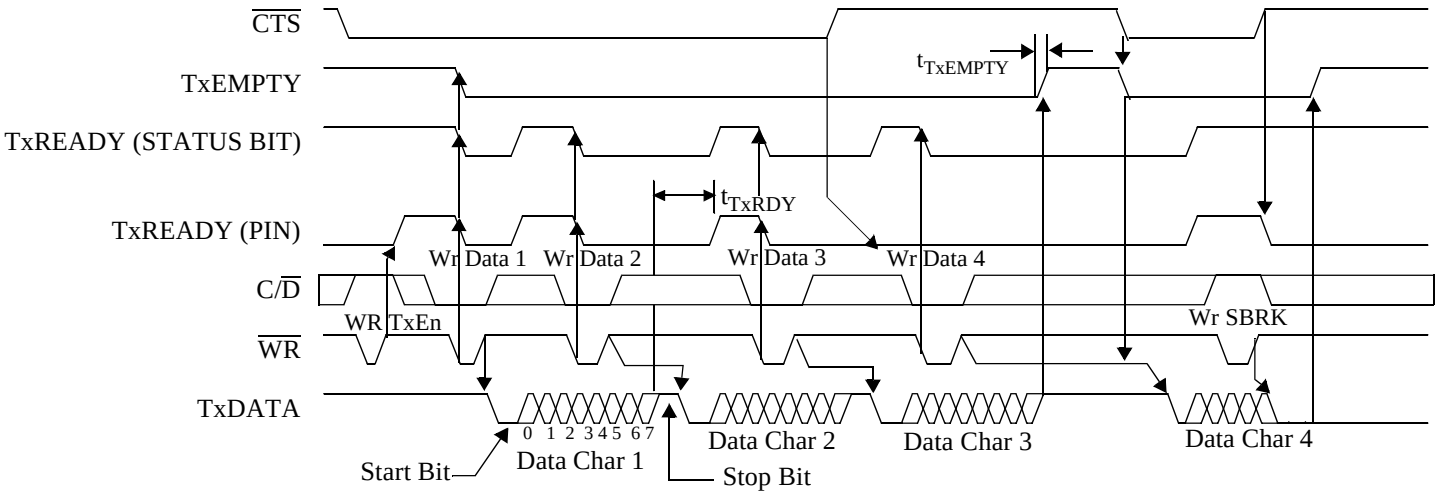
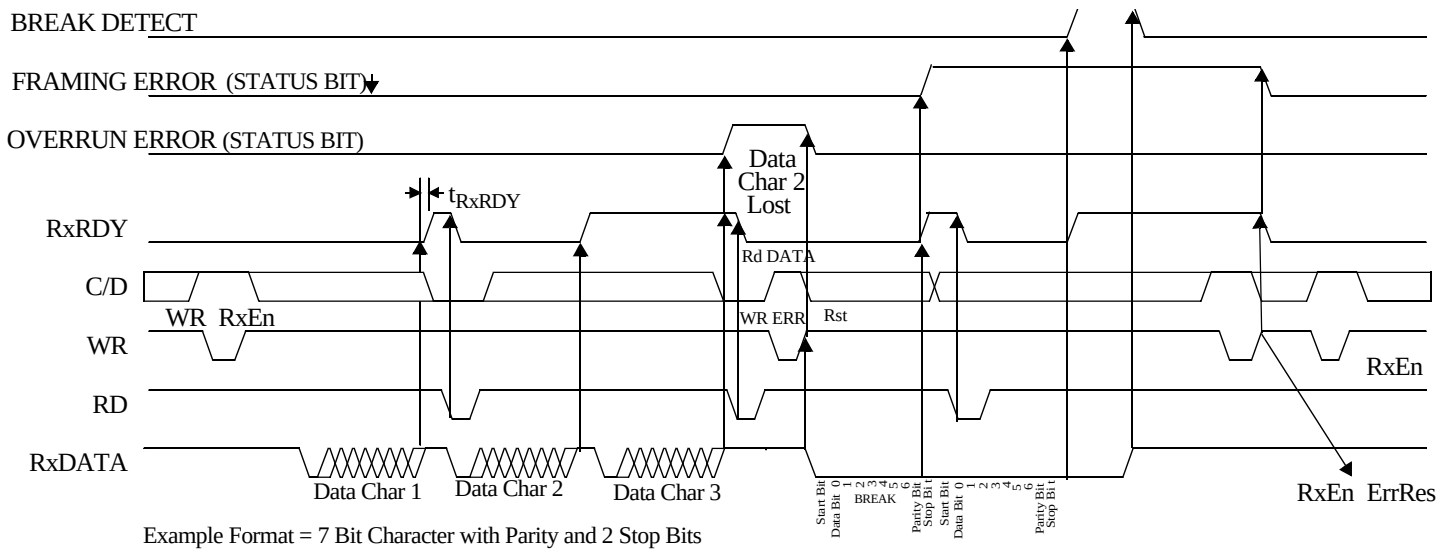


Figure 26. RD CONTROL



EXAMPLE FORMAT = 7 BIT CHARACTER WITH PARITY & 2 STOP BITS

Figure 27. Tx CONTROL-FLAGS ASYNC



Example Format = 7 Bit Character with Parity and 2 Stop Bits

Figure 28. Rx CONTROL-FLAGS ASYNC

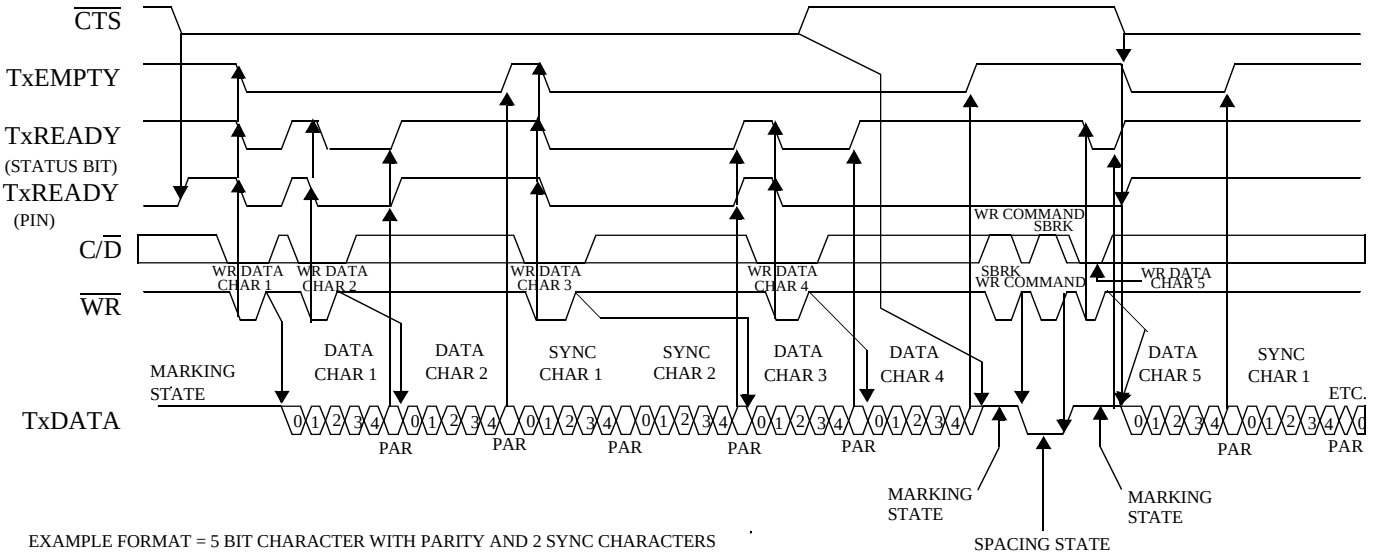
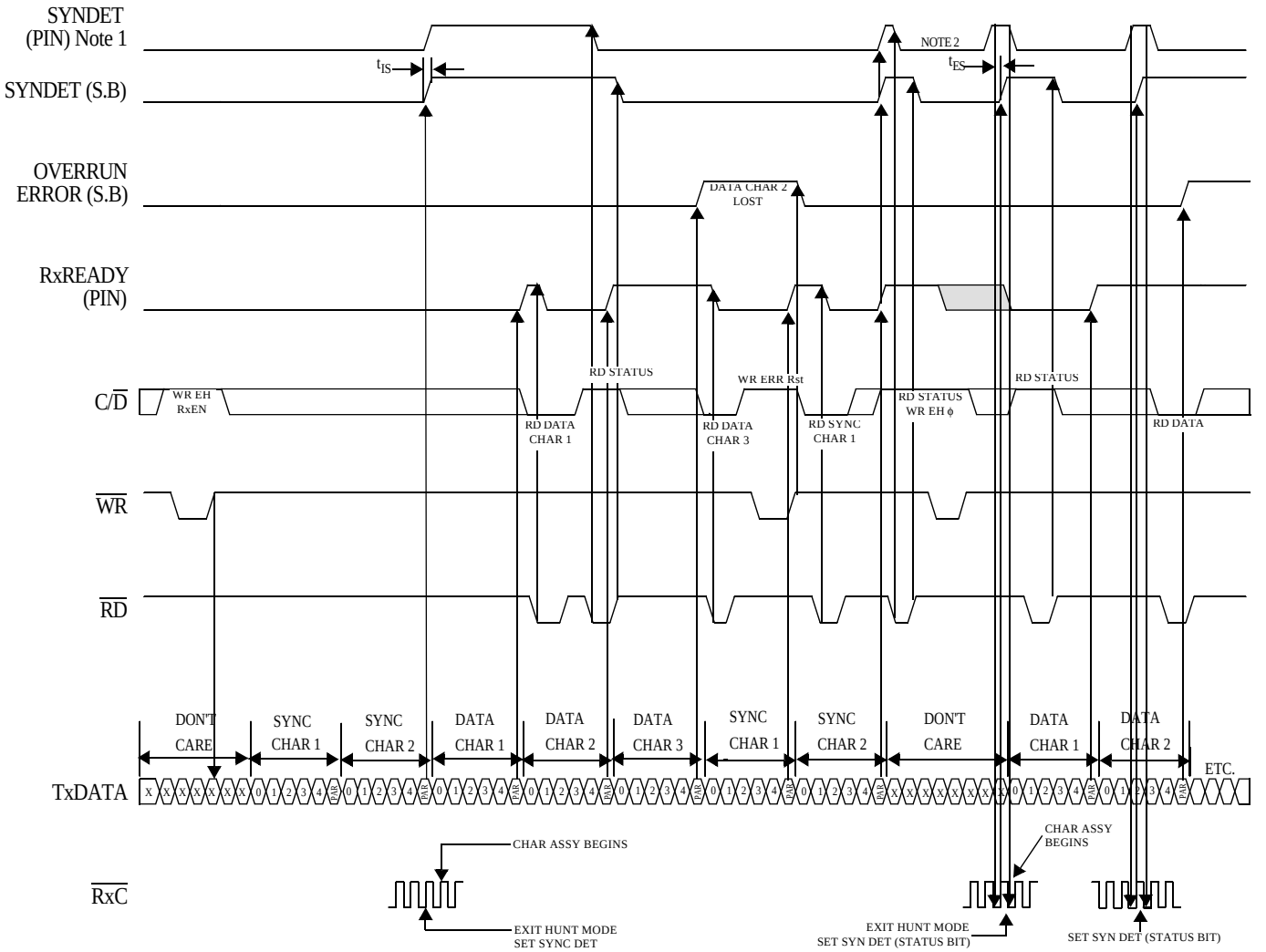


Figure 29. Tx CONTROL-FLAGS SYNC

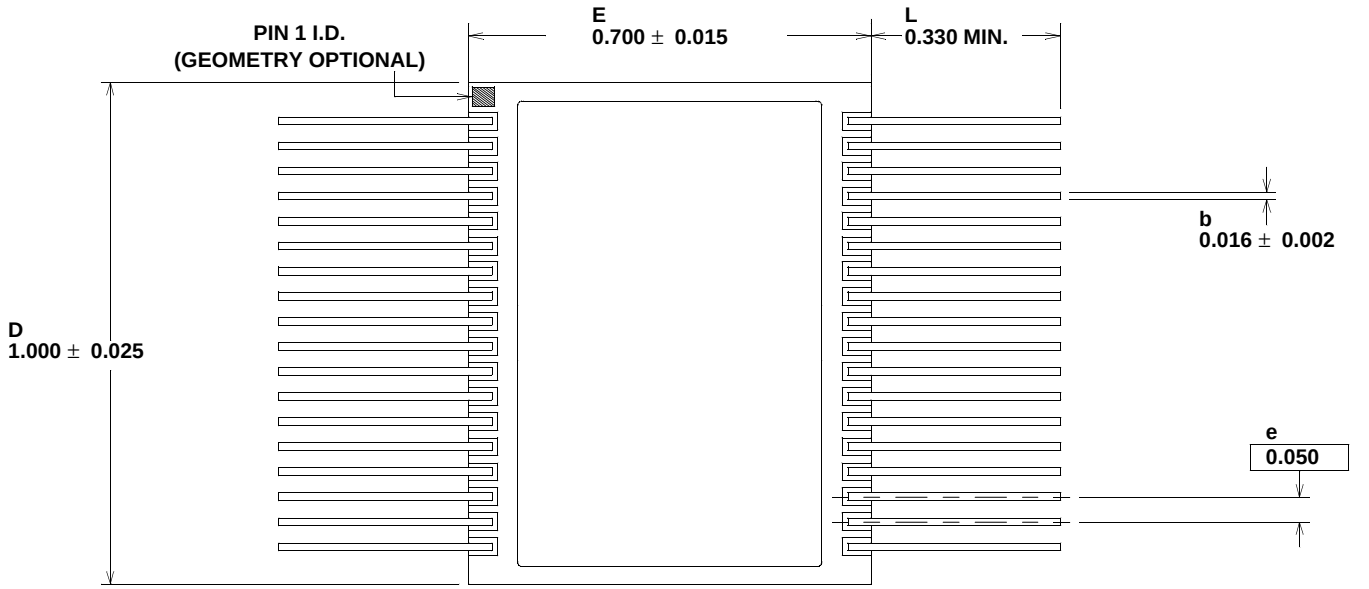


NOTE 1: INTERNAL SYNC, 2 SYNC CHARACTERS, 5 BITS, WITH PARITY

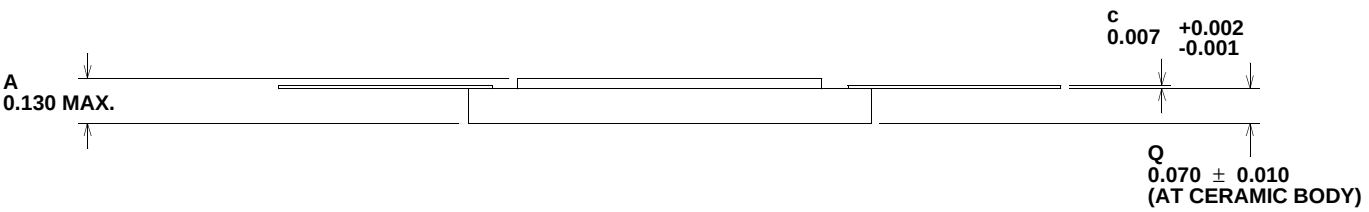
NOTE 2: EXTERNAL SYNC, 5 BITS, WITH PARITY

Figure 30. Rx CONTROL-FLAGS SYNC

PACKAGING



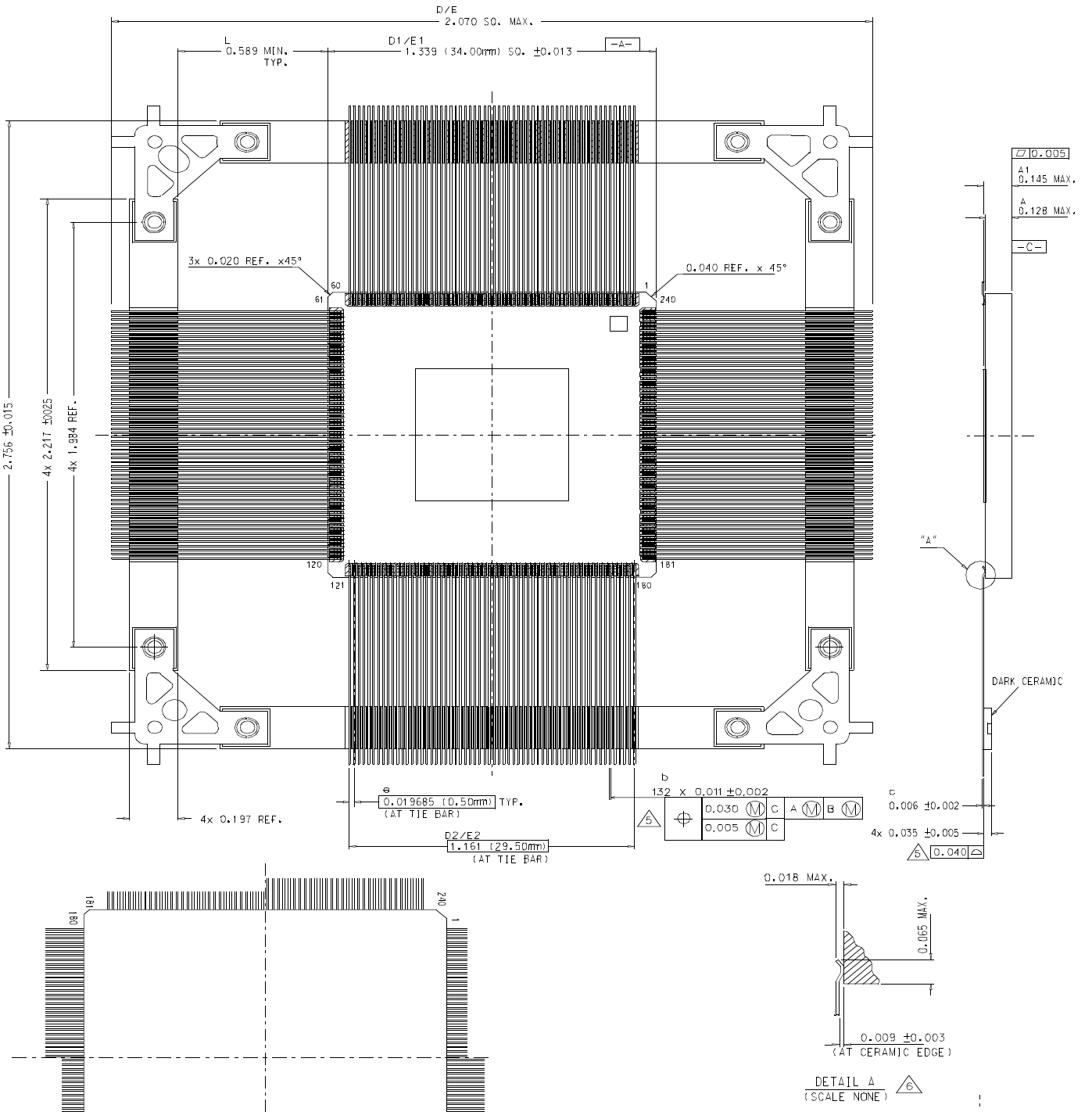
TOP VIEW



END VIEW

Notes:
1. All package finishes are per MIL-PRF-38535.
2. It is recommended that package ceramic be mounted to a heat removal rail located on the printed circuit board. A thermally conductive material such as MERECO XLN-589 or equivalent should be used.
3. Letter designations are for cross-reference to MIL-STD-1835.

Figure 31. 36-pin Ceramic Flatpack



Notes:

1. All exposed metalized area must be gold plated over nickel plating per MIL-PRF-38535.
2. Lead finish is in accordance with MIL-PRF-38535.
3. Lid is electrically connected to VSS.
4. Letter designations are to cross-reference to MIL-STD-1835.
5. Lead true position tolerances and coplanrity are not measured.
6. Dogleg geometries optional within dimensions shown.

Figure 32. 68-pin Ceramic Flatpack