BCD UP/DOWN COUNTER

FEATURES

- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT4510 are high-speed Si-gate CMOS devices and are pin compatible with the "4510" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4510 are edge-triggered synchronous up/down BCD counters with a clock input (CP), an up/down count control input (UP/$\overline{DN}$), an active LOW count enable input ($\overline{CE}$), an asynchronous active HIGH parallel load input (PL), four parallel inputs (D_0 to D_3), four parallel outputs (Q_0 to Q_3), an active LOW terminal count output ($\overline{TC}$), and an overriding asynchronous master reset input (MR).

Information on D_0 to D_3 is loaded into the counter while PL is HIGH, independent of all other input conditions except the MR input, which must be LOW. With PL LOW, the counter changes on the LOW-to-HIGH transition of CP if $\overline{CE}$ is LOW. UP/$\overline{DN}$ determines the direction of the count, HIGH for counting up, LOW for counting down. When counting up, $\overline{TC}$ is LOW when Q_0 and Q_3 are HIGH and $\overline{CE}$ is LOW. When counting down, $\overline{TC}$ is LOW when Q_0 to Q_3 and $\overline{CE}$ are LOW. A HIGH on MR resets the counter (Q_0 to Q_3 = = LOW) independent of all other input conditions.

Logic equation for terminal count:

$$\overline{TC} = \overline{\overline{CE} \cdot \{(UP/\overline{DN}) \cdot Q_0 \cdot Q_3 + (\overline{UP/\overline{DN}}) \cdot \overline{Q}_0 \cdot \overline{Q}_1 \cdot \overline{Q}_2 \cdot \overline{Q}_3\}}$$

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay CP to Q_n	C_L = 15 pF; V_{CC} = 5 V	21	23	ns
f_{max}	maximum clock frequency		57	58	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	50	53	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF
   f_o = output frequency in MHz; V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

16-lead DIL; plastic (SOT38Z).
16-lead mini-pack; plastic (SO16; SOT109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	PL	parallel load input (active HIGH)
4, 12, 13, 3	D_0 to D_3	parallel inputs
5	$\overline{CE}$	count enable input (active LOW)
6, 11, 14, 2	Q_0 to Q_3	parallel outputs
7	$\overline{TC}$	terminal count output (active LOW)
8	GND	ground (0 V)
9	MR	asynchronous master reset input (active HIGH)
10	UP/$\overline{DN}$	up/down control input
15	CP	clock input (LOW-to-HIGH, edge-triggered)
16	V_{CC}	positive supply voltage

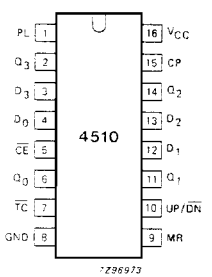


Fig. 1 Pin configuration.

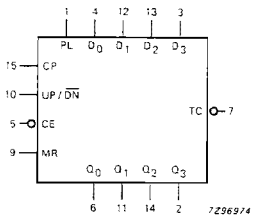


Fig. 2 Logic symbol.

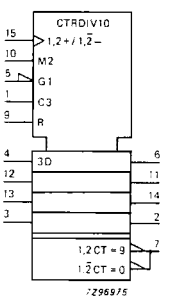


Fig. 3 IEC logic symbol.

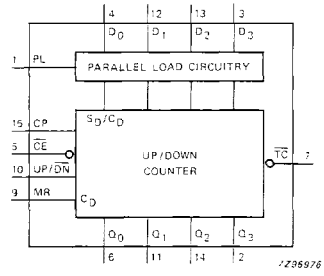


Fig. 4 Functional diagram.

FUNCTION TABLE

MR	PL	UP/$\overline{DN}$	$\overline{CE}$	CP	MODE
L	H	X	X	X	parallel load
L	L	X	H	X	no change
L	L	L	L	↑	count down
L	L	H	L	↑	count up
H	X	X	X	X	reset

H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH clock transition

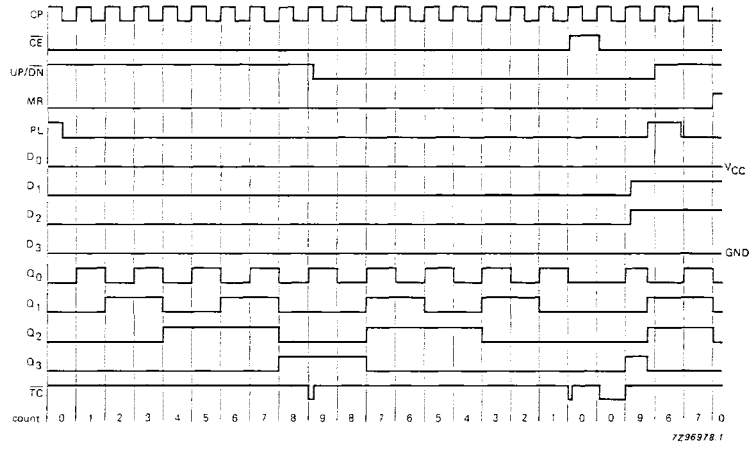


Fig. 5 Timing diagram.

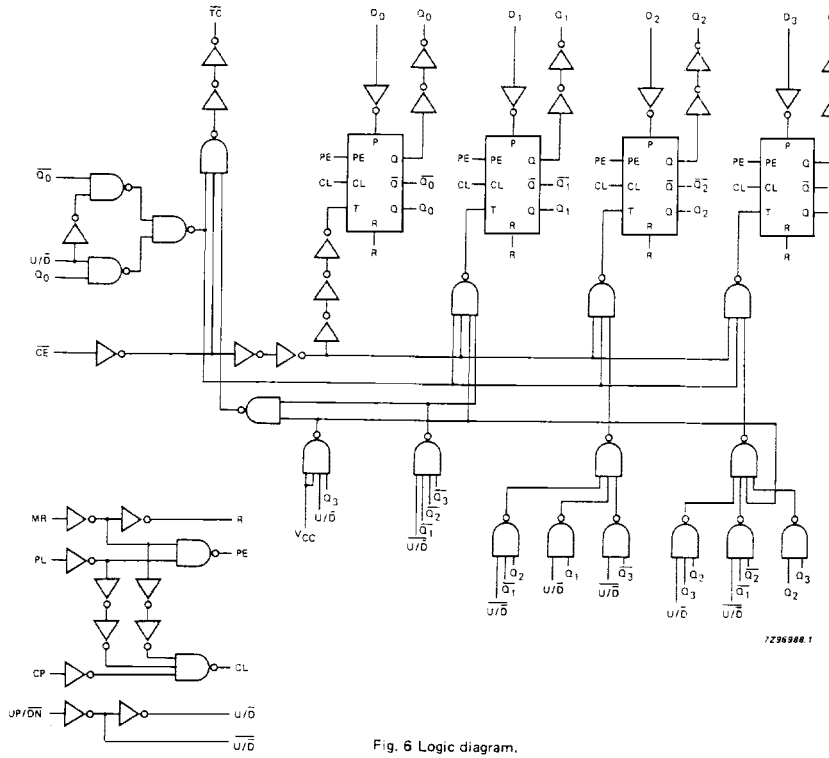


Fig. 6 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_n		69 25 20	220 44 37		275 55 47		330 66 56	ns	2.0 4.5 6.0	Fig. 7
t_{PHL}	propagation delay MR to Q_n		63 23 18	210 42 36		265 53 45		315 63 54	ns	2.0 4.5 6.0	Fig. 10
t_{PLH}/t_{PHL}	propagation delay PL to Q_n		77 28 22	250 50 43		315 63 54		375 75 64	ns	2.0 4.5 6.0	Fig. 9
t_{PHL}/t_{PLH}	propagation delay CP to $\overline{TC}$		74 27 22	260 52 44		325 65 55		395 78 66	ns	2.0 4.5 6.0	Fig. 7
t_{PHL}/t_{PLH}	propagation delay $\overline{CE}$ to $\overline{TC}$		36 13 10	125 25 21		155 31 26		190 38 32	ns	2.0 4.5 6.0	Fig. 8
t_{PLH}	propagation delay MR to $\overline{TC}$		69 25 20	235 47 40		295 59 50		355 71 60	ns	2.0 4.5 6.0	Fig. 10
t_{PHL}/t_{PLH}	propagation delay PL to $\overline{TC}$		91 33 26	300 60 51		375 75 64		450 90 77	ns	2.0 4.5 6.0	Fig. 9
t_{THL}/t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 9
t_W	pulse width CP, $\overline{CE}$ HIGH or LOW	80 16 14	25 9 7		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7
t_W	parallel load pulse width HIGH	80 16 14	22 8 7		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 10
t_W	master reset pulse width HIGH	100 20 17	19 7 6		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 10
t_{rem}	removal time MR to CP	80 16 14	28 10 8		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 10
t_{rem}	removal time PL to CP	80 16 14	14 5 4		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 10

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{su}	set-up time $\overline{UP}/DN$ to CP	100 20 17	30 11 9		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 8
t_{su}	set-up time $\overline{CE}$ to CP	100 20 17	19 7 6		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 8
t_{su}	set-up time D_n to PL	100 20 17	17 6 5		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 11
t_h	hold time $\overline{CE}$ to CP	5 5 5	0 0 0		5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig. 8
t_h	hold time D_n to PL	3 3 3	−6 −2 −2		3 3 3		3 3 3		ns	2.0 4.5 6.0	Fig. 11
t_h	hold time $\overline{UP}/DN$ to CP	0 0 0	−19 −7 −6		0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig. 8
f_{max}	maximum clock pulse frequency	6.0 30 35	17 52 62		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig. 7

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
D_n	0.75
PL, $\overline{CE}$	1.00
$\overline{UP}/DN$	1.00
CP	1.25
MR	1.50

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_n		27	50		63		75	ns	4.5	Fig. 7
t_{PHL}	propagation delay MR to Q_n		25	42		53		63	ns	4.5	Fig. 10
t_{PLH}/t_{PHL}	propagation delay PL to Q_n		28	53		66		80	ns	4.5	Fig. 9
t_{PHL}/t_{PLH}	propagation delay CP to $\overline{TC}$		29	58		73		87	ns	4.5	Fig. 7
t_{PHL}/t_{PLH}	propagation delay $\overline{CE}$ to $\overline{TC}$		17	31		39		47	ns	4.5	Fig. 8
t_{PLH}	propagation delay MR to $\overline{TC}$		31	50		63		75	ns	4.5	Fig. 10
t_{PHL}/t_{PLH}	propagation delay PL to $\overline{TC}$		35	68		85		102	ns	4.5	Fig. 10
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 9
t_W	pulse width CP, $\overline{CE}$ HIGH or LOW	16	9		20		24		ns	4.5	Fig. 7
t_W	parallel load pulse width HIGH	16	6		20		24		ns	4.5	Fig. 10
t_W	master reset pulse width HIGH	20	4		25		30		ns	4.5	Fig. 10
t_{rem}	removal time MR to CP	23	13		29		35		ns	4.5	Fig. 10
t_{rem}	removal time PL to CP	17	10		21		26		ns	4.5	Fig. 10
t_{su}	set-up time UP/$\overline{DN}$ to CP	20	12		25		30		ns	4.5	Fig. 8
t_{su}	set-up time $\overline{CE}$ to CP	20	6		25		30		ns	4.5	Fig. 8
t_{su}	set-up time D_n to PL	20	6		25		30		ns	4.5	Fig. 11
t_h	hold time $\overline{CE}$ to CP	5	0		5		5		ns	4.5	Fig. 8
t_h	hold time D_n to PL	5	0		5		5		ns	4.5	Fig. 11
t_h	hold time UP/$\overline{DN}$ to CP	0	−5		0		0		ns	4.5	Fig. 8
f_{max}	maximum clock pulse frequency	30	53		24		20		MHz	4.5	Fig. 7

AC WAVEFORMS

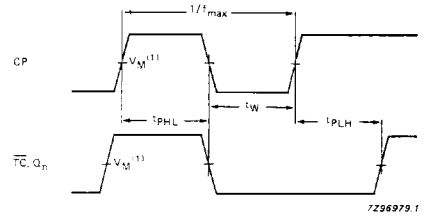


Fig. 7 Waveforms showing the clock (CP) to output (Q_n) and terminal count ($\overline{TC}$) propagation delays, the clock pulse width and the maximum clock pulse frequency.

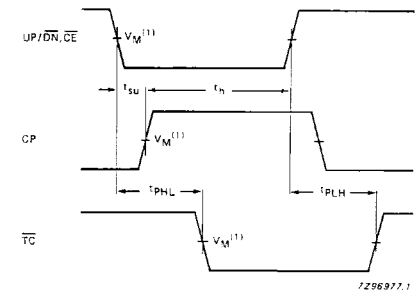


Fig. 8 Waveforms showing the set-up and hold times from count enable ($\overline{CE}$) and up/down (UP/$\overline{DN}$) control inputs to the clock pulse (CP), the propagation delays from UP/$\overline{DN}$, $\overline{CE}$ to $\overline{TC}$.

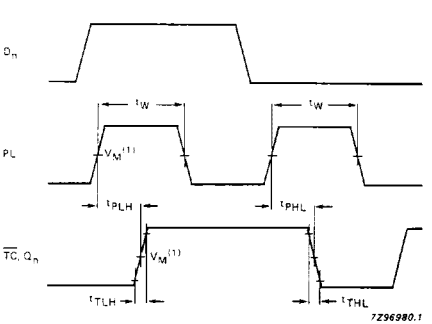


Fig. 9 Waveforms showing the preset enable pulse width, preset enable to output delays and output transition times.

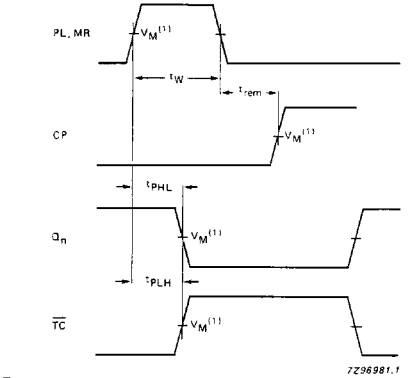


Fig. 10 Waveforms showing the master reset pulse, master reset to terminal count and Q_n delay and master reset to clock removal time.

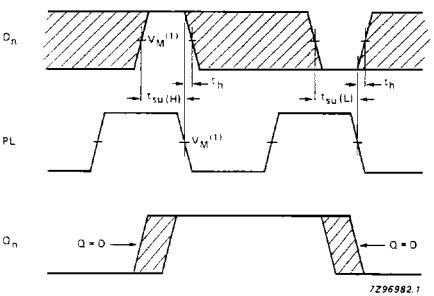


Fig. 11 Waveforms showing the data set-up and hold times to parallel load (PL).

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

APPLICATION INFORMATION

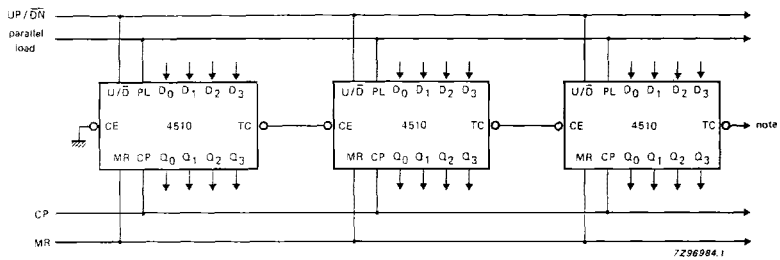


Fig. 12 Cascading counter packages (parallel clocking).

Note to Fig. 12

Terminal count ($\overline{TC}$) lines at the 2nd, 3rd, etc. stages may have a negative-going glitch pulse resulting from differential delays of different 4510s. These negative-going glitches do not affect proper 4510 operation. However, if the terminal count signals are used to trigger other edge sensitive logic devices, such as flip-flops or counters, the terminal count signals should be gated with the clock signal using a 2-input OR gate such as HC/HCT32.

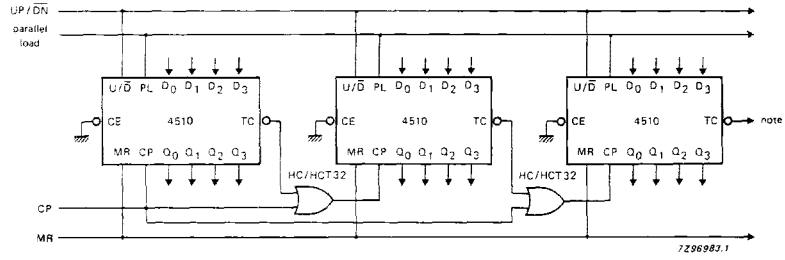
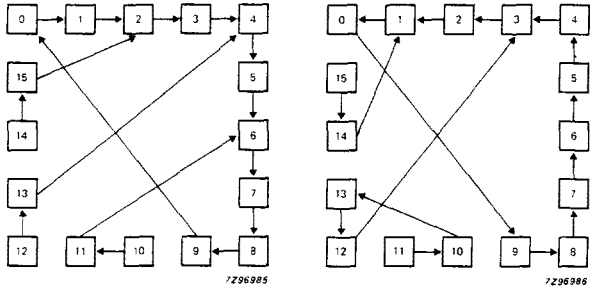


Fig. 13 Cascading counter packages (ripple clocking).

Note to Fig. 13

Ripple clocking mode: the UP/$\overline{DN}$ control can be changed at any count. The only restriction on changing the UP/$\overline{DN}$ control is that the clock input to the first counting stage must be HIGH. For cascading counters operating in a fixed up-count or down-count mode, the OR gates are not required between stages and $\overline{TC}$ is connected directly to the CP input of the next stage with $\overline{CE}$ grounded.



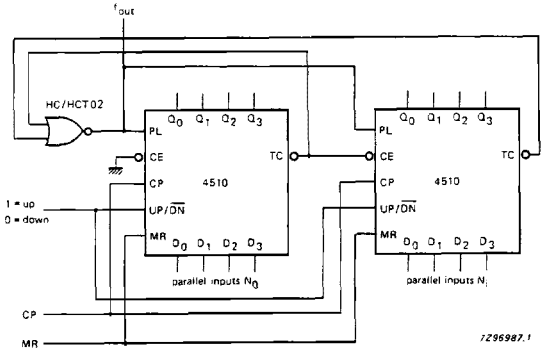
Count-up mode.

Count-down mode.

Notes to Fig. 14

Count-up mode: illegal states in BCD counters corrected in one count.
Count-down mode: illegal states in BCD counters corrected in one or two counts.

Fig. 14 State diagrams.



Note to Fig. 15

Use the following formulae to calculate N_{total}:

$$N_{total} = \left\{ \sum_{1}^{i} \pi(10 \times N_i) \right\} + N_0$$

$$f_{out} = \frac{f_{in}}{N_{total}}$$

Formulae are only applicable if legal data is provided to the parallel inputs.

Fig. 15 Programmable cascaded frequency divider.

parallel inputs				count-up	count-down
D_3	D_2	D_1	D_0	n	n
0	0	0	0	9	*
0	0	0	1	8	1
0	0	1	0	7	2
0	0	1	1	6	3
0	1	0	0	5	4
0	1	0	1	4	5
0	1	1	0	3	6
0	1	1	1	2	7
1	0	0	0	1	8
1	0	0	1	*	9

* no count; f_{out} is HIGH