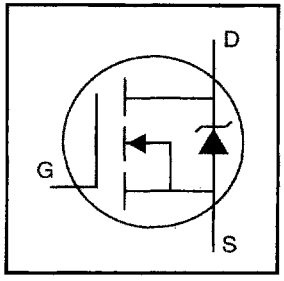
International
IOR Rectifier

PD - 9.1308

IRLZ34NS/L

HEXFET® Power MOSFET

- Logic-Level Gate Drive
- Advanced Process Technology
- Surface Mount (IRLZ34NS)
- Low-profile through-hole (IRLZ34NL)
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated



V_{DSS} = 55V

$R_{DS(on)}$ = 0.035Ω

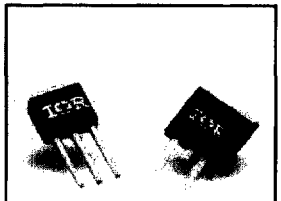
I_D = 30A

Description

Fifth Generation HEXFET® Power MOSFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design for which HEXFET Power MOSFETs are well known, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The D^2Pak is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D^2Pak is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0W in a typical surface mount application.

The through-hole version (IRLZ34NL) is available for low-profile applications.



TO-262 D^2Pak

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V⑤	30	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V⑤	21	
I_{DM}	Pulsed Drain Current ①⑤	110	
P_D @T_A = 25°C	Power Dissipation	3.8	W
P_D @T_C = 25°C	Power Dissipation	68	W
	Linear Derating Factor	0.45	W/°C
V_{GS}	Gate-to-Source Voltage	±16	V
E_{AS}	Single Pulse Avalanche Energy ②⑤	110	mJ
I_{AR}	Avalanche Current ①	16	A
E_{AR}	Repetitive Avalanche Energy ①	6.8	mJ
dv/dt	Peak Diode Recovery dv/dt ③⑤	5.0	V/ns
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

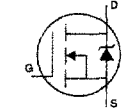
Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	2.2	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mounted,steady-state)**	—	40	

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	55	—	—	V	V_{GS} = 0V, I_D = 250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.065	—	V/°C	Reference to 25°C, I_D = 1mA ⑤
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.035	Ω	V_{GS} = 10V, I_D = 16A ④
		—	—	0.046		V_{GS} = 5.0V, I_D = 16A ④
		—	—	0.060		V_{GS} = 4.0V, I_D = 14A ④
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	2.0	V	V_{DS} = V_{GS}, I_D = 250μA
g_{fs}	Forward Transconductance	11	—	—	S	V_{DS} = 25V, I_D = 16A ⑤
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	A	V_{DS} = 55V, V_{GS} = 0V
		—	—	250		V_{DS} = 44V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS} = 16V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS} = -16V
Q_g	Total Gate Charge	—	—	25	nC	I_D = 16A
Q_{gs}	Gate-to-Source Charge	—	—	5.2		V_{DS} = 44V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	14		V_{GS} = 5.0V, see figure 6 and 13 ④⑤
$t_{d(on)}$	Turn-On Delay Time	—	8.9	—	ns	V_{DD} = 28V
t_r	Rise Time	—	100	—		I_D = 16A
$t_{d(off)}$	Turn-Off Delay Time	—	21	—		R_G = 6.5Ω, V_{GS} = 5.0V
t_f	Fall Time		29			R_D = 1.8Ω, see figure 10 ④⑤
L_S	Internal Source Inductance	—	7.5	—	nH	Between lead, and center of die contact
C_{iss}	Input Capacitance	—	880	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	220	—		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	—	94	—		f = 1.0MHz, see figure 5⑤

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	30	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	110		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	T_J = 25°C, I_S = 16A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	76	110	ns	T_J = 25°C, I_F = 16A
Q_{rr}	Reverse Recovery Charge	—	190	290	nC	di/dt = 100A/μs ④⑤
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (see figure 11)

② V_{DD} = 25V, starting T_J = 25°C, L = 610μH, R_G = 25Ω, I_{AS} = 16A. (see figure 12)

③ I_{SD} ≤ 16A, di/dt ≤ 270A/μs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 175°C

④ Pulse width ≤ 300μs; duty cycle ≤ 2%.

⑤ Uses IRLZ34N data and test conditions

** When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.

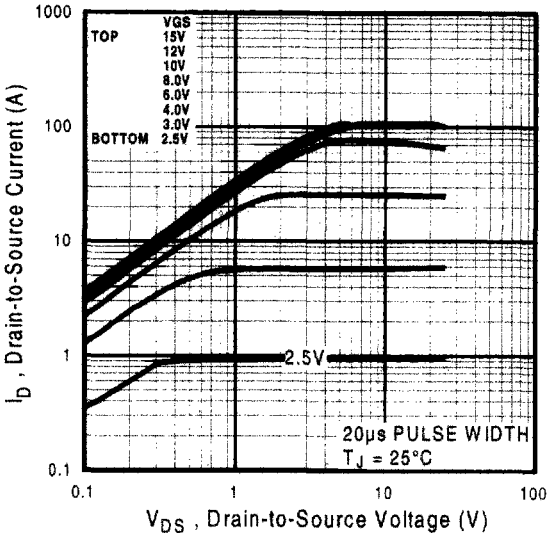


Fig 1. Typical Output Characteristics

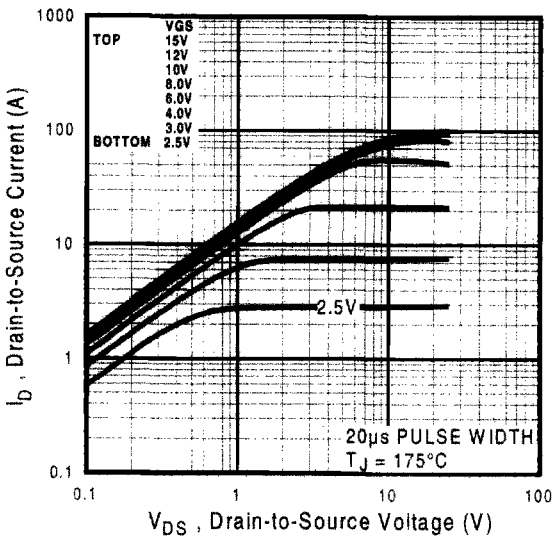


Fig 2. Typical Output Characteristics

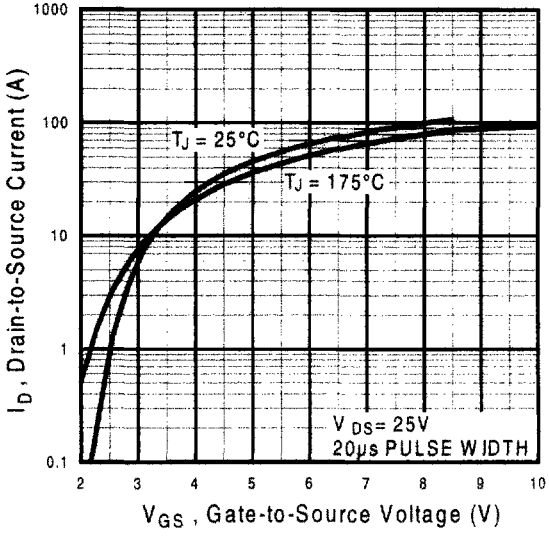


Fig 3. Typical Transfer Characteristics

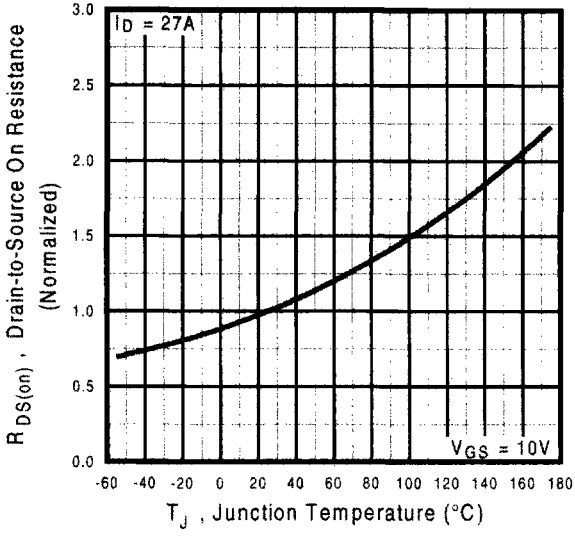


Fig 4. Normalized On-Resistance
Vs. Temperature

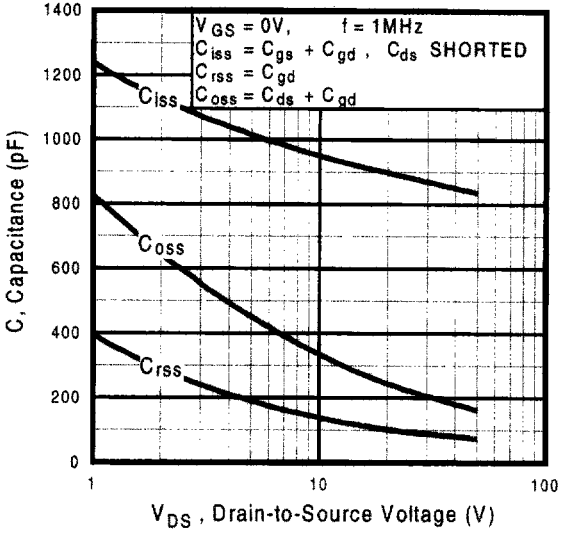


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

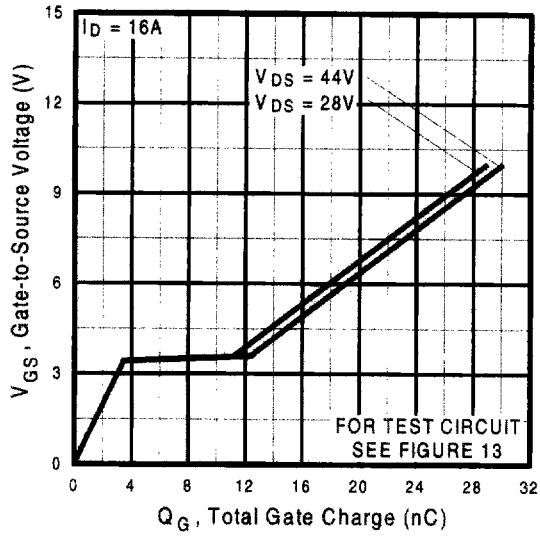


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

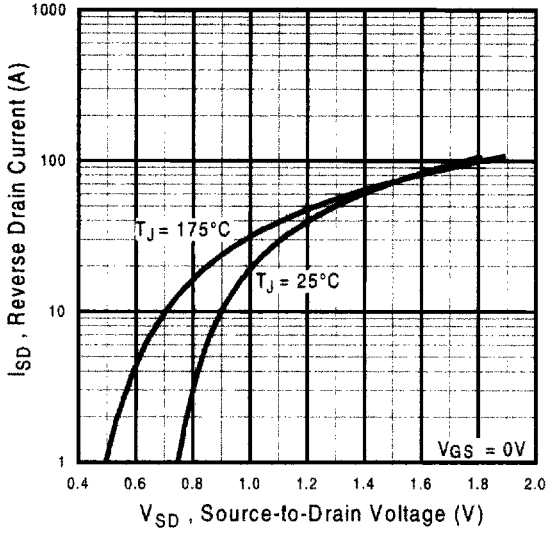


Fig 7. Typical Source-Drain Diode Forward Voltage

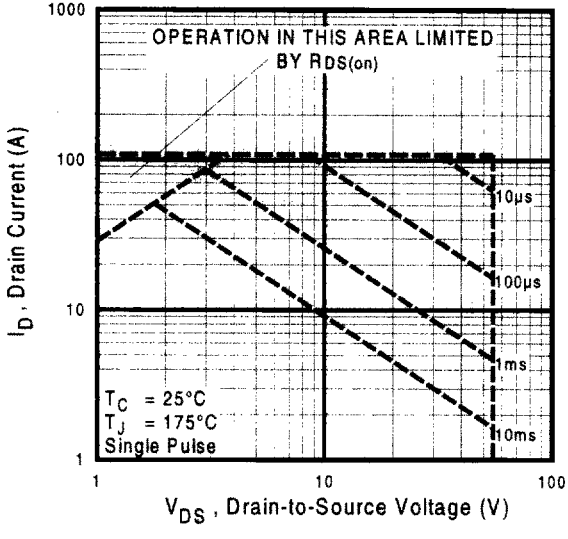


Fig 8. Maximum Safe Operating Area

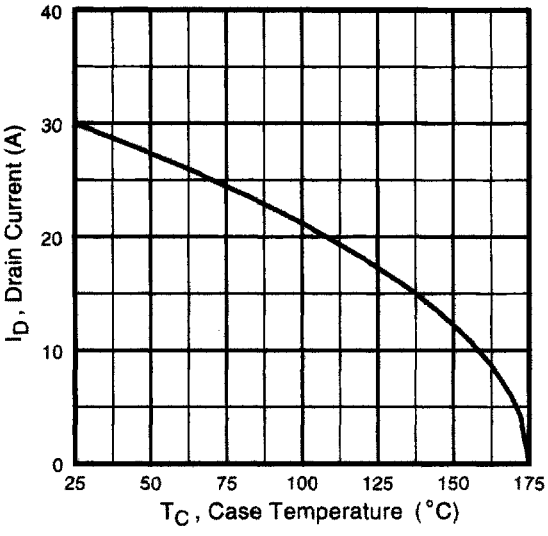


Fig 9. Maximum Drain Current Vs. *Case Temperature*

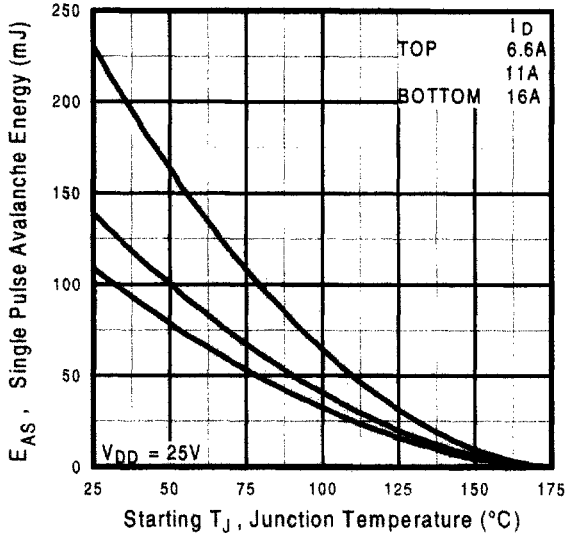


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

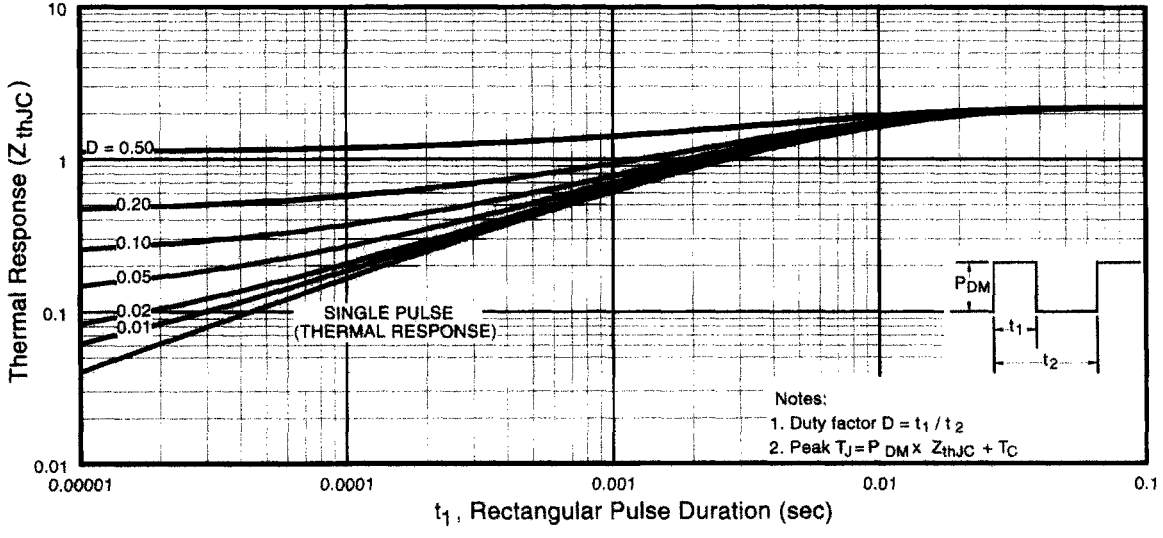


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

Mechanical drawings, Appendix A
Part marking information, Appendix B
Test Circuit diagrams, Appendix C