⋮⋮Lattice®

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ispLSI 2032
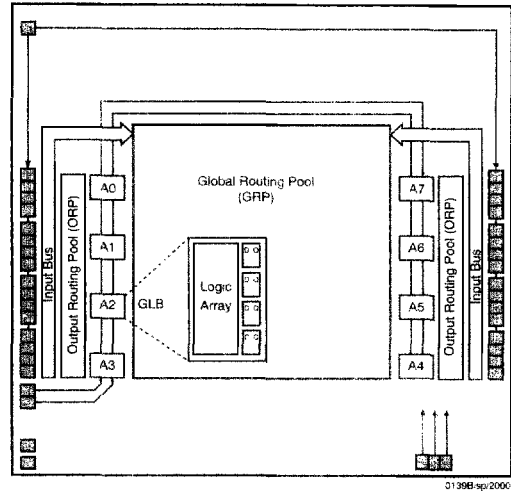
High Density Programmable Logic

Features

• **HIGH DENSITY PROGRAMMABLE LOGIC**

— **1000 PLD Gates**
— **32 I/O Pins, Two Dedicated Inputs**
— **32 Registers**
— **High Speed Global Interconnect**
— **Wide Input Gating for Fast Counters, State Machines, Address Decoders, etc.**
— **Small Logic Block Size for Random Logic**

• **HIGH PERFORMANCE E²CMOS* TECHNOLOGY**

— **$f$max = 180 MHz Maximum Operating Frequency**
— **$t$pd = 5.0 ns Propagation Delay**
— **TTL Compatible Inputs and Outputs**
— **Electrically Erasable and Reprogrammable**
— **Non-Volatile**
— **100% Tested at Time of Manufacture**
— **Unused Product Term Shutdown Saves Power**

• **ispLSI OFFERS THE FOLLOWING ADDED FEATURES**

— **In-System Programmable (ISP™) 5-Volt Only**
— **Increased Manufacturing Yields, Reduced Time-to-Market and Improved Product Quality**
— **Reprogram Soldered Devices for Faster Prototyping**

• **OFFERS THE EASE OF USE AND FAST SYSTEM SPEED OF PLDs WITH THE DENSITY AND FLEXIBILITY OF FIELD PROGRAMMABLE GATE ARRAYS**

— **Complete Programmable Device Can Combine Glue Logic and Structured Designs**
— **Enhanced Pin Locking Capability**
— **Three Dedicated Clock Input Pins**
— **Synchronous and Asynchronous Clocks**
— **Programmable Output Slew Rate Control to Minimize Switching Noise**
— **Flexible Pin Placement**
— *Optimized Global Routing Pool Provides Global Interconnectivity*

• **ispEXPERT™ – LOGIC COMPILER AND COMPLETE ISP DEVICE DESIGN SYSTEMS FROM HDL SYNTHESIS THROUGH IN-SYSTEM PROGRAMMING**

— **Superior Quality of Results**
— **Tightly Integrated with Leading CAE Vendor Tools**
— **Productivity Enhancing Timing Analyzer, Explore Tools, Timing Simulator and ispANALYZER™**
— **PC and UNIX Platforms**

Functional Block Diagram

0139B-sp/2000

Description

The ispLSI 2032 is a High Density Programmable Logic Device. The device contains 32 Registers, 32 Universal I/O pins, two Dedicated Input Pins, three Dedicated Clock Input Pins, one dedicated Global OE input pin and a Global Routing Pool (GRP). The GRP provides complete interconnectivity between all of these elements. The ispLSI 2032 features 5V in-system programmability and in-system diagnostic capabilities. The ispLSI 2032 offers non-volatile reprogrammability of the logic, as well as the interconnect to provide truly reconfigurable systems.

The basic unit of logic on the ispLSI 2032 device is the Generic Logic Block (GLB). The GLBs are labeled A0, A1 .. A7 (see Figure 1). There are a total of eight GLBs in the ispLSI 2032 device. Each GLB is made up of four macrocells. Each GLB has 18 inputs, a programmable AND/OR/Exclusive OR array, and four outputs which can be configured to be either combinatorial or registered. Inputs to the GLB come from the GRP and dedicated inputs. All of the GLB outputs are brought back into the GRP so that they can be connected to the inputs of any GLB on the device.

November 1998

Functional Block Diagram

Figure 1. ispLSI 2032 Functional Block Diagram

Notes:
*Y1 and RESET are multiplexed on the same pin
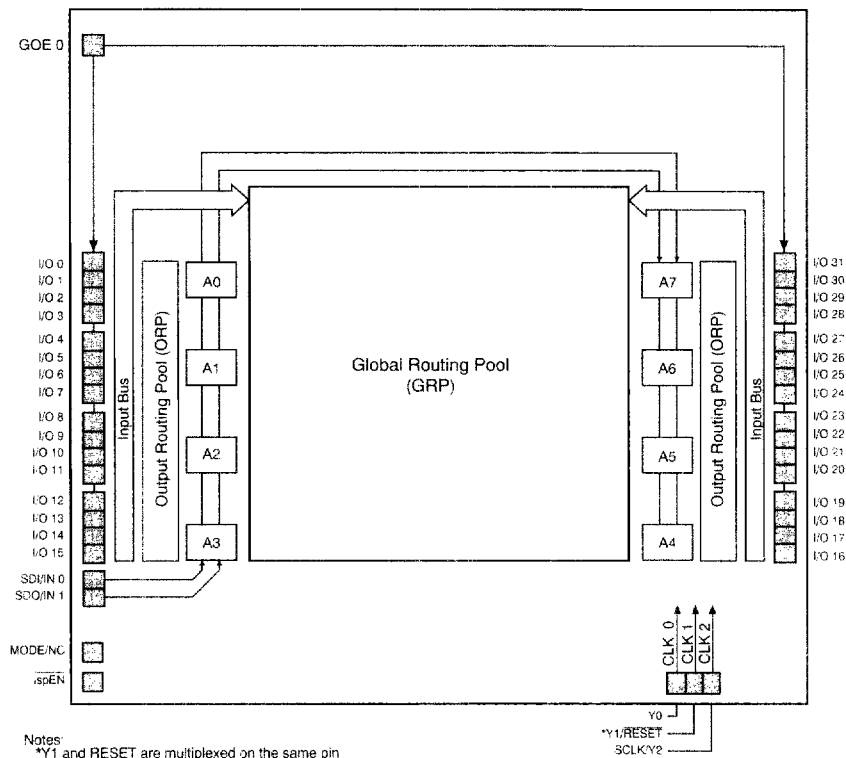
The device also has 32 I/O cells, each of which is directly connected to an I/O pin. Each I/O cell can be individually programmed to be a combinatorial input, output or bi-directional I/O pin with 3-state control. The signal levels are TTL compatible voltages and the output drivers can source 4 mA or sink 8 mA. Each output can be programmed independently for fast or slow output slew rate to minimize overall output switching noise.

Eight GLBs, 32 I/O cells, two dedicated inputs and two ORPs are connected together to make a Megablock (see Figure 1). The outputs of the eight GLBs are connected to a set of 32 universal I/O cells by the ORP. Each ispLSI 2032 device contains one Megablock.

The GRP has as its inputs, the outputs from all of the GLBs and all of the inputs from the bi-directional I/O cells. All of these signals are made available to the inputs of the GLBs. Delays through the GRP have been equalized to minimize timing skew.

Clocks in the ispLSI 2032 device are selected using the dedicated clock pins. Three dedicated clock pins (Y0, Y1, Y2) or an asynchronous clock can be selected on a GLB basis. The asynchronous or Product Term clock can be generated in any GLB for its own clock.

External Timing Parameters

Over Recommended Operating Conditions

PARAMETER	TEST[4] COND.	#[2]	DESCRIPTION[1]	-180 MIN.	-180 MAX.	-150 MIN.	-150 MAX.	-135 MIN.	-135 MAX.	UNITS
t_{pd1}	A	1	Data Prop. Delay, 4PT Bypass, ORP Bypass	–	5.0	–	5.5	–	7.5	ns
t_{pd2}	A	2	Data Prop. Delay	–	7.5	–	8.0	–	10.0	ns
f_{max}	A	3	Clk Frequency with Internal Feedback [3]	180	–	154	–	137	–	MHz
f_{max} (Ext.)	–	4	Clk Frequency with Ext. Feedback $\left(\frac{1}{t_{su2}+t_{co1}}\right)$	125	–	111	–	100	–	MHz
f_{max} (Tog.)	–	5	Clk Frequency, Max. Toggle	200	–	167	–	167	–	MHz
t_{su1}	–	6	GLB Reg Setup Time before Clk, 4 PT Bypass	3.0	–	3.0	–	4.0	–	ns
t_{co1}	A	7	GLB Reg. Clk to Output Delay, ORP Bypass	–	4.0	–	4.5	–	4.5	ns
t_{h1}	–	8	GLB Reg. Hold Time after Clk, 4 PT Bypass	0.0	–	0.0	–	0.0	–	ns
t_{su2}	–	9	GLB Reg. Setup Time before Clk	4.0	–	4.5	–	5.5	–	ns
t_{co2}	–	10	GLB Reg. Clk to Output Delay	–	4.5	–	5.0	–	5.5	ns
t_{h2}	–	11	GLB Reg. Hold Time after Clk	0.0	–	0.0	–	0.0	–	ns
t_{r1}	A	12	Ext. Reset Pin to Output Delay	–	7.0	–	8.0	–	10.0	ns
t_{rw1}	–	13	Ext. Reset Pulse Duration	4.0	–	4.5	–	5.0	–	ns
t_{ptoeen}	B	14	Input to Output Enable	–	10.0	–	11.0	–	12.0	ns
$t_{ptoedis}$	C	15	Input to Output Disable	–	10.0	–	11.0	–	12.0	ns
t_{goeen}	B	16	Global OE Output Enable	–	5.0	–	5.0	–	6.0	ns
t_{goedis}	C	17	Global OE Output Disable	–	5.0	–	5.0	–	6.0	ns
t_{wh}	–	18	Ext. Synchronous Clk Pulse Duration, High	2.5	–	3.0	–	3.0	–	ns
t_{wl}	–	19	Ext. Synchronous Clk Pulse Duration, Low	2.5	–	3.0	–	3.0	–	ns

Table 2-0030B-180/2032

1. Unless noted otherwise, all parameters use the GRP, 20 PTXOR path, ORP and Y0 clock.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-bit counter using GRP feedback.
4. Reference Switching Test Conditions section.

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External Timing Parameters

Over Recommended Operating Conditions

PARAMETER	TEST[4] COND.	#[2]	DESCRIPTION[1]	-110 MIN.	-110 MAX.	-80 MIN.	-80 MAX.	UNITS
t_{pd1}	A	1	Data Propagation Delay, 4PT Bypass, ORP Bypass	–	10.0	–	15.0	ns
t_{pd2}	A	2	Data Propagation Delay	–	13.0	–	18.5	ns
f_{max}	A	3	Clock Frequency with Internal Feedback[3]	111	–	84.0	–	MHz
f_{max} (Ext.)	–	4	Clock Frequency with External Feedback $\left(\frac{1}{t_{su2}+t_{co1}}\right)$	77.0	–	57.0	–	MHz
f_{max} (Tog.)	–	5	Clock Frequency, Max. Toggle	125	–	83.0	–	MHz
t_{su1}	–	6	GLB Reg. Setup Time before Clock, 4 PT Bypass	5.5	–	7.5	–	ns
t_{co1}	A	7	GLB Reg. Clock to Output Delay, ORP Bypass	–	5.5	–	8.0	ns
t_{h1}	–	8	GLB Reg. Hold Time after Clock, 4 PT Bypass	0.0	–	0.0	–	ns
t_{su2}	–	9	GLB Reg. Setup Time before Clock	7.5	–	9.5	–	ns
t_{co2}	–	10	GLB Reg. Clock to Output Delay	–	6.5	–	9.5	ns
t_{h2}	–	11	GLB Reg. Hold Time after Clock	0.0	–	0.0	–	ns
t_{r1}	A	12	Ext. Reset Pin to Output Delay	–	13.5	–	19.5	ns
t_{rw1}	–	13	Ext. Reset Pulse Duration	6.5	–	10.0	–	ns
t_{ptoeen}	B	14	Input to Output Enable	–	14.5	–	24.0	ns
$t_{ptoedis}$	C	15	Input to Output Disable	–	14.5	–	24.0	ns
t_{goeen}	B	16	Global OE Output Enable	–	7.0	–	12.0	ns
t_{goedis}	C	17	Global OE Output Disable	–	7.0	–	12.0	ns
t_{wh}	–	18	External Synchronous Clock Pulse Duration, High	4.0	–	6.0	–	ns
t_{wl}	–	19	External Synchronous Clock Pulse Duration, Low	4.0	–	6.0	–	ns

Table 2-0030B-110/2032

1. Unless noted otherwise, all parameters use the GRP, 20 PTXOR path, ORP and Y0 clock.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-bit counter using GRP feedback.
4. Reference Switching Test Conditions section

ispLSI 2000